Detection and Diagnosis of Sub-Module Faults for Modular Multilevel Converters

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***Abstract*—This paper presents a new fault detection technique for the diagnosis and localization of sub-module faults that are developed due to failures in switching devices inside Modular Multilevel Converters (MMC). Unlike other fault detection strategies that have been proposed in literature, the proposed fault detection technique does not need extra sensors or special power circuits as it depends on an ADAptive LINEar Neuron (ADALINE) capacitor voltage estimation algorithm. The proposed fault detection technique is validated by Hardware In the Loop (HIL) real time simulations through which different case studies are simulated to test the algorithm under different operating conditions.**

Keywords—ADALINE; fault detection; MMC.

I. INTRODUCTION

Faults that could be located inside the sub-modules of the MMC which are due to failures in semi-conductor devices not only affect the quality of the output power but also threatens the safety of the converter. Since MMCs have large number of sub-modules, the probability of having a fault inside certain sub-module is relatively high. As a result, it is highly recommended to detect and localize the fault quickly to give a chance for the MMC inner control system to deal with the fault by either the converter disconnection or applying a suitable fault tolerant technique.

According to the literature, there are different types of sub-module faults that can strike MMCs and affect their operation [1-2]. Since MMCs are used in important applications and at the same time they form a big investment, it is extremely important to detect these fault very quickly to protect the whole system from sudden failures. For this particular purpose, the sub-module faults are investigated in the following sub-sections. Moreover, popular fault detection techniques are discussed to find out the advantages and disadvantages of each method and pointing what is needed in the process of fault detection of MMCs.

This paper presents a new Fault Detection Unit (FDU) which depends on the estimation of sub-module capacitor voltages using ADALINE algorithm. Section II presents a brief analysis of the MMC during faults. The proposed fault detection technique is explained in section III. Section IV shows the simulation results and discussions. Section V shows the conclusion and major findings of the presented work.

II. FAULTS INSIDE MMCS

In order to design a FDU for the detection and diagnosis of sub-module faults, firstly the structure and operation principle of the MMC needs to be investigated, then, mapping for different faults including the MMC behaviour during these faults must be studied.

A. The structure of MMCs

The MMC consists of sub-modules connected in series forming a leg in each phase. The sub-module can be a half-bridge or a full-bridge and each sub-module has a capacitor that buffers the energy from the dc to the ac side and vice versa; thus the dc-link capacitor is not required. A high-speed bypass switch is added to the output port of the sub-module to isolate the sub-module in case of a fault. As shown in Fig. 1, each phase leg is divided into two arms upper and lower. Each arm has identical numbers of sub-modules to generate balanced voltages in the two arms of each phase. Inductors are installed in arms to smooth and filter the currents [3-4].

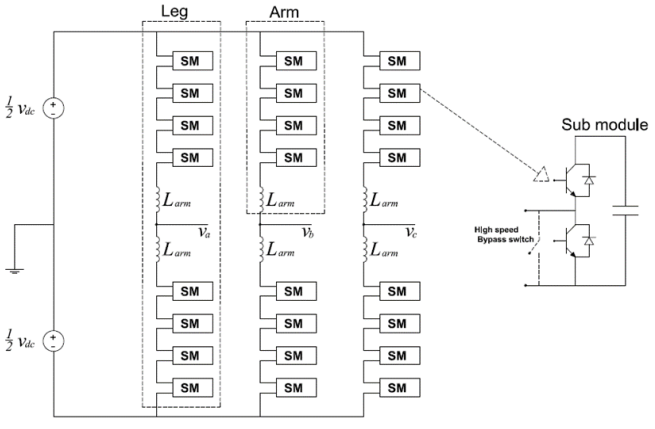

Fig. 1. The structure of the MMC.

B. MMC Operating Modes

The MMC half bridge sub-module has four operation modes during which energy is transferred:

Mode 1: When S1 is closed, S2 is opened, and the arm has positive polarity. The current flows into the capacitor, charging it. The sub-module is then inserted. See Fig. 2(a).

Mode 2: When S1 is opened, S2 is closed, and the arm has positive polarity. The sub-module is bypassed, and the current flows towards the next sub-module, keeping the capacitor charge constant. The sub-module is then bypassed. See Fig. 2(b).

Mode 3: S1 is closed, S2 is opened, and the arm has negative polarity. The capacitor starts to discharge and then the sub-module is inserted. See Fig. 2(c).

Mode 4: When S1 is opened, S2 is closed, and the arm has negative polarity. The current flows towards the next module, keeping the capacitor charge constant, after which and the sub-module is bypassed. See Fig. 2(d).

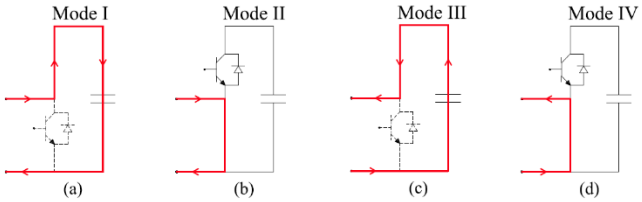

Fig. 2. Different operating modes of MMC sub-modules. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

C. IGBT faults

The IGBT operation is always linked to the presence of freewheeling diodes, this is simply because of the fact that the IGBT cannot function correctly without having a freewheeling diode dissipating the excess power due to the IGBT turn-off action, however this link does not exist in case of fault which means that the IGBT may be exposed to a fault while having a healthy freewheeling diode and vice versa. All of this because the power electronic device faults always depend on the semiconductor physics. Power electronic device faults are either open circuit faults or short circuit faults. Table I shows the main causes of each fault type and their corresponding consequences [5-7].

In case of having an open circuit fault in the upper sub-module switch, the negative capacitor current is blocked. As a result, the only path for this current is the lower freewheeling diode. The same case occurs for the lower switch of the sub-module but the capacitor current is positive. Table II concludes the behavior of arm currents and sub-module voltages in case of having an open circuit fault.

Regarding switch short circuit faults, the behavior is different as the output voltage will equal to the capacitor voltage when the upper switch is short circuited. When the short circuit is applied to the lower switch, the sub-module output voltage is equal to zero. Table III describes the relationship between the arm current and sub-module output voltage during switch short circuit faults.

It is important to mention that in case of open circuit faults, there is no threat on the safety of the converter or the whole system since the consequences are related to the power quality so there is no real need to shut off the converter. On the other hand, if the sub-module is subjected to short circuit fault in the power electronic device, it is a must to disconnect the sub-module immediately [8].

TABLE I
FAULTS IN SUB-MODULE IGBTS

Fault type	Failure mechanism	Consequences
Open circuit	Bond wire rupture	1) Pulsating current 2) Distortion in output current and voltage
	Gate driver failure	
Short circuit	High voltage breakdown	Overheating in few cells at first and then spreads to other cells leading to complete failure
	Static/ dynamic latch up	
	Energy shocks	

TABLE II
RELATIONSHIP BETWEEN SUB-MODULE OUTPUT VOLTAGE AND ARM CURRENTS DURING OPEN CIRCUIT FAULTS

The state of the sub-module	The sign of the arm current	The sub-module output voltage		
		Normal operation	Upper switch open circuit fault	Lower switch open circuit fault
Bypassed	+ve	V_c	V_c	V_c
	-ve	V_c	0	V_c
Inserted	+ve	0	0	V_c
	-ve	0	0	0

TABLE III
RELATIONSHIP BETWEEN SUB-MODULE OUTPUT VOLTAGE AND ARM CURRENTS DURING SHORT CIRCUIT FAULTS

The state of the sub-module	The sign of the arm current	The sub-module output voltage		
		Normal operation	Upper switch open circuit fault	Lower switch open circuit fault
Bypassed	+ve	V_c	V_c	0
	-ve	V_c	V_c	0
Inserted	+ve	0	V_c	0
	-ve	0	V_c	0

D. The MMC behaviour during faults

The main operation concept of the MMC is keeping the upper and lower arm voltages the same. In case of having a fault in any sub-module, the balance between arm voltages will not be kept as the number of healthy modules in the upper and lower arms will be different. This means that the ac voltage will have different notation due to the change of the arm voltage [9]. During sub-module faults, the summation of capacitor voltages for the upper and lower arms can be expressed by:

$$V_{Cu}^{\Sigma} = \frac{1}{C_{eff\,u}} \int \frac{i_u(1-e_v^*)}{2} dt \quad (1)$$

$$V_{Cl}^{\Sigma} = \frac{1}{C_{eff\,l}} \int \frac{i_l(1+e_v^*)}{2} dt \quad (2)$$

Where e_v^* is the reference signal of the desired AC voltage, this signal has a sinusoidal shape that depends on the modulation factor as shown in (3):

$$e_v^* = m_x \cos(\omega t + \theta) \quad (3)$$

The voltage generated across each arm can be expressed as:

$$V_u = \frac{N_u V_{Cu}^{\Sigma} (1-e_v^*)}{2} \quad (4)$$

$$V_l = \frac{N_l V_{Cl}^{\Sigma} (1+e_v^*)}{2} \quad (5)$$

From (1) and (2) and substituting in (4) and (5) respectively, the arm voltages can be rewritten as:

$$V_u = \frac{1-e_v^*}{2\,C_{eff\,u}} \int \frac{i_u(1-e_v^*)}{2} dt \quad (6)$$

$$V_l = \frac{1+e_v^*}{2\,C_{eff\,l}} \int \frac{i_l(1+e_v^*)}{2} dt \quad (7)$$

Regarding the arm currents, each arm current will have its own phase angle instead of having a unified phase angle φ as given below:

$$i_u = i_{dc} + \frac{\widehat{i_{ac}}}{2} \cos(\omega t + \alpha) \quad (8)$$

$$i_l = i_{dc} - \frac{\widehat{i_{ac}}}{2} \cos(\omega t + \beta) \quad (9)$$

Substituting (8) and (9) into (6) and (7) gives the AC components of the upper and lower arm voltages:

$$V_{u\,ac} = \frac{1}{2\,C_{eff\,u}} \left[-\frac{m_u^2+8}{16} \frac{\widehat{i_{ac}}}{2} \cos(\omega t + \beta) + \frac{m_u i_{dc}}{4} \cos(\omega t + \theta) + \frac{3 m_u}{8} \frac{\widehat{i_{ac}}}{2} \cos(2\omega t + \theta + \alpha) - \frac{m_u^2 i_{dc}}{8} \cos(2\omega t + 2\theta) + \frac{m_u^2}{32} cos(3\omega t + 2\theta + \alpha) \right] \quad (10)$$

$$V_{l\,ac} = \frac{1}{2\,C_{eff\,l}} \left[\frac{m_l^2+8}{16} \frac{\widehat{i_{ac}}}{2} \cos(\omega t + \alpha) - \frac{m_l i_{dc}}{4} \cos(\omega t + \theta) + \frac{3 m_l}{8} \frac{\widehat{i_{ac}}}{2} \cos(2\omega t + \theta + \alpha) - \frac{m_l^2 i_{dc}}{8} \cos(2\omega t + 2\theta) - \frac{m_l^2}{32} cos(3\omega t + 2\theta + \alpha) \right] \quad (11)$$

As given in (10) and (11), losing the balance between the upper and lower arm voltages due to sub-module faults has severely affected the quality of the output power. This is because of the super imposed third harmonics generated in the arm voltages which has not been existed during normal operation. Moreover, the distorted arm voltages will be reflected on sub-module voltages as they will either increase or decrease according the type of fault. This has been also proven in Table II and Table III which shows the behavior of capacitor voltages during open circuit and short circuit faults.

III. The Proposed Fault Detection Algorithm

The capacitor voltage estimation is performed using the Adaptive Linear Neuron (ADALINE) algorithm. ADALINE is known for its efficiency and its rapid on-line tracking technique for dynamically changing voltage signals. It has been utilized in many applications because of its robust performance, low calculation burden, and accurate results [10-12]. The ADALINE algorithm is formed by simple calculations that do not consume large computing time, which is very important in the application of capacitor voltage estimation. To estimate the capacitor voltages, the MMC governing equations are written in the vector form as follows:

$$\frac{v_{dc}}{2} - v_o - v_{Lu} = [S_{u1} \quad S_{u2} \quad \dots \quad S_{uN}] \begin{bmatrix} v_{cu1\_est} \\ v_{cu2\_est} \\ \vdots \\ v_{cuN\_est} \end{bmatrix} \quad (12)$$

$$\frac{v_{dc}}{2} + v_o - v_{Ll} = [S_{l1} \quad S_{l2} \quad \dots \quad S_{lN}] \begin{bmatrix} v_{cl1\_est} \\ v_{cl2\_est} \\ \vdots \\ v_{clN\_est} \end{bmatrix} \quad (13)$$

where S_{xi} is the switching state for the i^{th} sub-module, $v_{Lu} = L_{arm} \frac{di_u}{dt}$, and $v_{Ll} = L_{arm} \frac{di_l}{dt}$.

The ADALINE algorithm produces a linear combination of its input vector $X(k)$, which represents the switching state of each sub-module whether it is inserted or by-passed at time *k,* and it is written as follows:

$$X(k) = [S_{x1} \quad S_{x2} \quad \dots \quad S_{xN}]^T \quad (14)$$

where the suffix *T* refers to the transpose operation. As shown in Fig. 3, the input vector is multiplied by the weight vector W, which resembles the estimated capacitor voltages, given in (12) and (13):

$$W(k) = [v_{cx1\_est} \quad v_{cx2\_est} \quad \dots \quad v_{cxN\_est}]. \quad (15)$$

This multiplication is performed to produce the predicted linear output $\hat{y}(k) = X^T W(k)$. The next step is updating the weight vector using an adaptation algorithm called the Widrow-Hoff delta rule given by [17]:

$$W(k+1) = W(k) + \alpha \frac{X(k)(y(k)-\hat{y}(k))}{X(k)^T X(k)} \quad (16)$$

where α is the reduction factor and $y(k) = \frac{v_{dc}}{2} \pm v_o - v_{Lx}$. The adaptation algorithm is responsible for adjusting the weighting vector, which represents the estimated capacitor voltages so that the linear output of the ADALINE, $\hat{y}(k)$ is equal to its target value $y(k)$. When the error between the measured signal $y(k)$and the estimated signal $\hat{y}(k)$ converges to zero, the ADALINE algorithm decomposes the signal and estimates capacitor voltages.

It is observed that increasing the reduction factor α increases the convergence speed on account of losing stability as the prediction error may increase dramatically. This observation is a common behavior of the Widrow-Hoff delta rule for all the study cases. A practical value for the reduction factor α is 0.002 for this application. This value is determined based on minimizing the error to guarantee system stability [13]. It is worth mentioning that the proposed capacitor voltage

estimation unit is based on three voltage sensors per phase to measure the voltage across the arm reactors and the output phase voltage. This action enables the implementation of a low-cost centralized controller for the MMC with large numbers of sub-modules, since voltage measurements of sub-modules and their associated communication links are eliminated. The proposed fault detection algorithm which is based on the percentage reduction of the estimated voltage and the rate of change of the difference between the estimated sub-modules voltages from the RLS and the actual voltages. The proposed FDU calculates the per-unit values $v_{cx\ pu\ i}$ from the estimated sub-module capacitor voltages $v_{cx\ RLS\ est\ i}$ using the RLS algorithm. The instantaneous rate of change of the difference between the RLS estimated capacitor voltages and the actual measured voltages is calculated, $\frac{de_{xi}}{dt}$. A sub-module is considered faulty if its pu voltage reduced below 85% and the rate of change of the difference signal exceeds a predefined threshold value which is tuned to insure the sensitivity of the proposed FDU. Moreover, a counter is used to check the steadiness of the fault conditions for a certain time, 1 ms, before indicating a faulty sub-module.

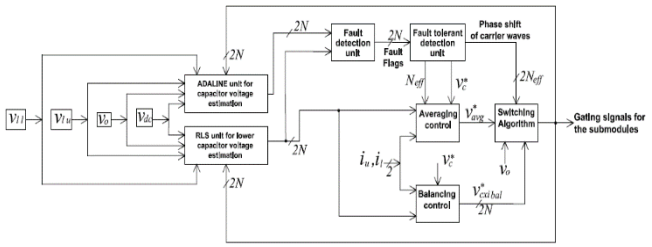

Fig. 3. Block diagram of the proposed capacitors voltages estimation unit based on the ADALINE algorithm.

IV. Simulation Results

The proposed FDU is validated using the hardware in the loop (HIL) concept. The MMC system is simulated using the RT-LAB and downloaded to the OP-4510 real time digital simulator, while the proposed FDU and its associated capacitor voltage estimation units are programmed using the LAB-VIEW software and uploaded to a FPGA physical controller type cRIO-9024 as shown in Fig. 4. The system parameters are shown in Table IV.

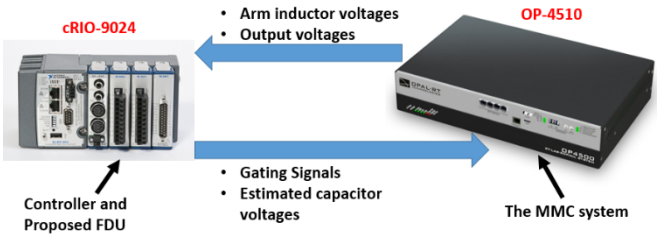

Fig.4: The HIL platform.

TABLE IV
MMC Model Parameters

Parameter	Value
Rated power	1 MW
Sub-module rated voltage	2,250 V
Rated DC voltage	4,500 V
Arm inductance	3 mH
Sub-module capacitance	1,900 µF
Number of sub-modules per leg	8
Load impedance	30 Ω , 6 mH

The applied case is conducted to investigate the capabilities of the proposed FDU under multiple faults in two different arms. An open-circuit fault is applied to the upper switch of the third sub-module in the upper arm of phase *a* at *t= 0.5s* while a short circuit fault is applied to the lower switch in the second sub-module in the lower arm of phase *a* at *t= 0.7s*. As shown in Fig. 4 (a) and 4 (b), the voltage and current of phase *a* are suffering from increased level of harmonics and high DC component just after the event of the open circuit fault. After the moment of applying the short circuit fault, the harmonics are increased affecting the power quality of the voltage and current and lowering it to a very poor level. The sub-module capacitor voltages start to lose their balancing just after the first fault and increases rapidly after the application of the second fault as indicated in Fig. 4(c).

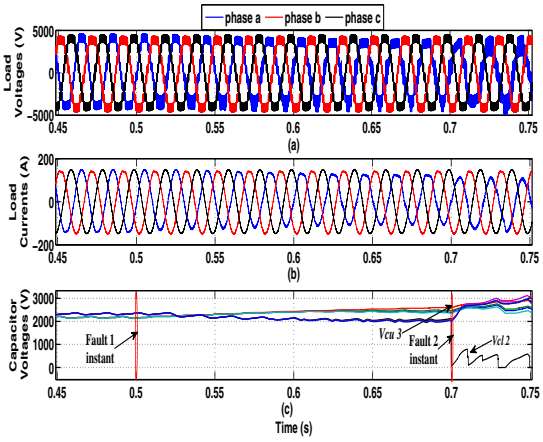

Fig. 4: Operation during multiple faults: a) Three-phase voltages, b) three-phase load currents, c) voltages of leg *a* sub-modules.

The ADALINE estimated voltages of leg *a* are shown in Fig. 5 and 6. These estimated voltages are tracking their actual voltages until the instant of the two faults, after each fault the estimated voltages contain steady-state error. Regarding the estimated voltages of the faulty sub-modules, it is very clear that these signals have been rapidly decreased which make it very easy for the FDU to detect the two faults.

Since the capacitor voltage of the third sub-module cannot be charged and discharged properly due to the first fault, the voltage balancing strategy partially fails to achieve its function. However, after the second fault, the situation gets worse and the balancing control totally fails in balancing the capacitor voltages.

As shown in Fig. 7 (a), the estimated voltage of the two faulty sub-modules has exceeded the FDU voltage threshold for a longer period than the other voltages, this is the first condition for the FDU to detect the fault. While the estimated signals of all other sub-modules are by far higher than the FDU voltage threshold. Also the derivative of the error signal between the RLS and ADALINE estimated voltages for the faulty sub-modules have by far exceeded the pre-defined threshold and this is the second condition which the FDU needs to satisfy to successfully detect the fault. The FDU succeeds to detect and localize the first fault after 5 ms while for the second fault the detection time is lower than 2.2 ms as demonstrated in Fig. 7 (b). This case has proved that the proposed FDU is able to detect multiple faults very quickly, this is needed in MMCs as the high number of sub-modules may lead to several failures at the same time.

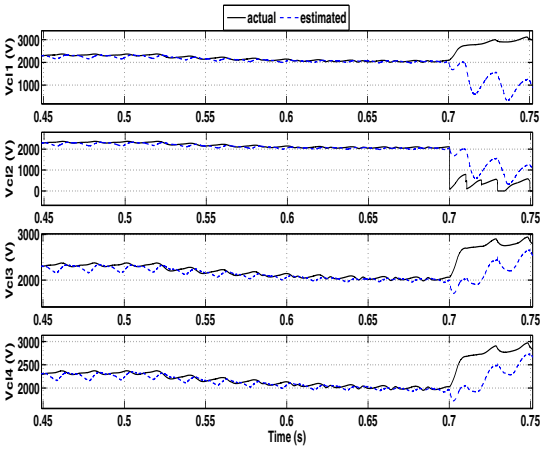

Fig. 5: Actual and estimated voltages of the upper arm sub-modules of phase *a*, under two faults

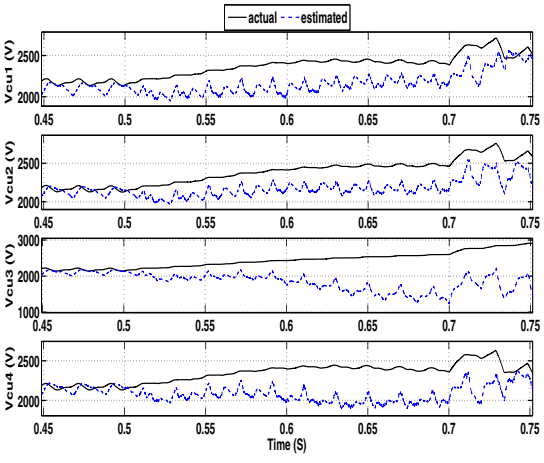

Fig. 6: Actual and estimated voltages of the lower arm sub-modules of phase *a*, under two faults.

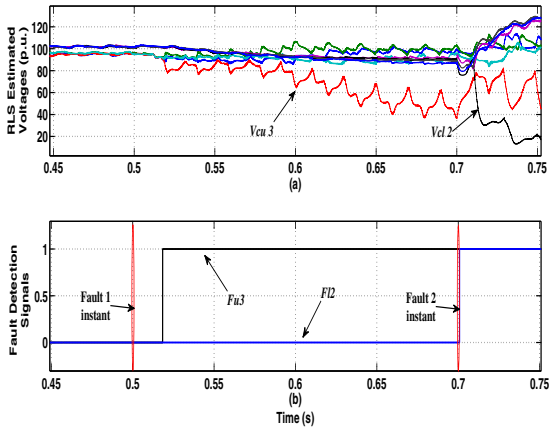

Fig. 7: The performance of the FDU under IGBT multiple faults: a) The pu values of ADALINE estimated voltages of the upper arm of phase *a*, b) the detection times of the two faults.

V. Conclusion

In this paper, a new fault detection technique for the detection and localization of MMC sub-module switch faults has been presented. The proposed FDU is based on an ADALINE capacitor voltage estimation algorithm. The HIL real-time simulations showed an accurate performance for detecting and localizing different faults which results from its processing where the fault decision is not only based on the reduction on the estimated per-unit voltage but also on the rate of change of the difference between the estimated voltages from the proposed ADALINE algorithm. Also the results show the necessity of having a fault tolerant control scheme to protect the MMC during sub-module faults and helps it to continue in a safe operation mode.

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