High Tolerance of Charge Pump Leakage Current in Integer-N PLL Frequency Synthesizer for 5G Networks

Zakia Berber and Samir Kameche
dept. of Telecommunications STIC Lab
University of Tlemcen, Algeria
zakia.berber@gmail.com
samir.kameche@mail.univ-tlemcen.dz

Elhadj Benkhelifa
School of Computing and Digital Technologies
Staffordshire University, UK
e.benkhelifa@staffs.ac.uk

Abstract

One of the most promising solutions for the future fifth generation communication systems is to utilize millimeter wave (mm-W) radio frequencies. There is, however, little works about Phase Locked Loop (PLL) frequency synthesizer designed for mm-W band frequency for 5G applications. This article discusses integer PLL architecture for frequency synthesis; it targets the highest range of 5G mmW [81-86] GHz using ultra-wide channel spacing of 1GHz. This work investigates the design of a third passive loop filter for frequency synthesizer using a *Phase Frequency Detector* and a current switch *Charge Pump* such as analog devices ADF4155. The critical performance for the Charge Pump depends on the leakage current produced by the technology of its transistors. This undesirable current can have a high impact on the loop stability. However, by optimizing PLL filter parameters, the synthesizer was able to tolerate up to 117 nA. With such a high leakage current, a high performance of the system was achieved. As a result, less than −71 dBc reference spur level at 50 MHz offset frequency was ensured and 3.23 µs settling time for a hopping frequency of 5 GHz was achieved.

Keywords

PLL; frequency synthesizer; ADF4155; 5G; mm-Waves; loop filter; loop bandwidth; phase margin; Charge Pump; leakage current; settling time; references spurs, Optimisation

I.   Introduction

Since the 1980s, a new generation of mobile technology has been launched every decade or so, and each has brought new capabilities with new mobile services, which has provided faster speeds, greater capacity and more reliable services. The foreseeable Fifth Generation (5G) is promises to deliver new added benefits over the preceding technologies (Ofcom, 2018), where the wireless access will extend far beyond the capabilities of previous generations mobile communication. Examples of these capabilities include very high data rates (20 Gbit/s peak data rate), very low latency (<1ms), ultra-high-speed availability (up to 500km/h), extreme device densities (1 million connections per km^2), with ultra-high reliability and energy efficiency (Wang and al., 2016), (Borkar and Pande, 2016). However, these new requirements will only be realized by the development of an LTE-advanced, which includes LTE release 10 and LTE-Broadcast and by integrating its licensed and unlicensed bands and in combination with new radio-access technologies as Wi-Fi and cellular Internet of Thing technologies (Habiba and Hossain, 2018) (Huawei, 2016) (Ericsson, 2016). To meet these challenges, 5G networks will leverage multi-layer spectrum. For macro cells, it will use low band, that is below 6 GHz, for instance, the integration of 700 MHz band and C- band, which will interwork and co-exist with 4G systems; but it will also exploits high band that is above 6 GHz for smaller cells (Kawanishi and al., 2018) (Ofcom, 2017) (Huawei, 2017).

Beyond 6 GHz band, World Radio-communication Conference 2015 (WRC-15) has paved the way for the future development of the International Mobile Telecommunication (IMT) on higher frequency bands by identifying several frequencies for the future networks, summarized in the Table I (Huawei, 2017). Recent studies suggest that high frequencies above 20 GHz, commonly known as millimeter Waves (mmW)

frequencies, could be used, thanks to its large width of the bandwidth, which can be ranging from 500 MHz to 2 GHz (Nokia, 2017)(Nokia, 2016). 30 and 40 GHz ranges have been chosen as the most promising candidate frequencies for the early deployment of 5G- mmW systems. On the other hand, a higher allocated band, makes it possible to further diversify the fields of application. For this reason, in this paper, we have chosen to propose and simulate a frequency generation system in the higher unlicensed [81-86] GHz allocation frequency bands for 5G systems.

TABLE 1. FRENQUENCY GROUP

Group 30 GHz	Group 40 GHz	Group 50 GHz	Groups 70/80 GHz
24.25- 27.5 31.8 – 33.4	37 – 40.5 40.5 – 42.5 42.5 – 43.5	45.5 – 47 47 – 47.2 47.2 – 50.2 50.4 – 52.6	66 – 71 71 – 76 **81 - 86**

Thus, Phase locked Loop (PLL) based frequency synthesizer is an important subsystem of any communication systems. It is widely used in wireless transceivers to provide precise and fine tunable local oscillation frequencies. Integration of this circuit in the 5G systems has been addressed in several research projects and several works been published in this context. However, most of the presented PLL synthesizers are proposed to generate the 28GHz and 38GHz frequency bands, whereas, as previously mentioned, higher frequencies can better tackle the 5G data challenges. Also, to generate such high frequencies, the bandwidth must also be broad in frequency. So, in this paper, we propose to design a model of PLL frequency synthesizer, able to generate not only the entire [81-86] GHz band frequency but can also ensure 1 GHz ultra-broadband channel spacing.

Moreover, spectrum and timing specifications of various wireless standards impose a stringent requirement on the synthesizer Phase Noise, spur level and settling time (Gorji and Zakeri, 2012). These characteristics, which depend largely on the loop filter, are determined by a loop bandwidth limited to approximately $1/10^{th}$ of the reference frequency and a phase margin of more than 0 degree and less than 90 degrees (Yiwu Tang and al., 2002) (Zakia and SAMIR, 2015). Also, the loop filter component is used to achieve a desired PLL transfer function and to implement desired poles and zeros for realizing a given open loop transfer function. Furthermore, in combination with the charge pump, it sets the overall open loop gain of the system (Zakia and Samir, 2018). Considering this association, the leakage current produced by the Charge Pump transistors can have a great influence on the performance of the system. For that, this parameter must be less than $1/10^{th}$ of the Charge Pump gain. Otherwise, it can have a significant impact on the loop stability, which will be manifested by a high density of reference spurs.

A number of researchers have attempted to improve PLL characteristics and various architectures of PLL frequency synthesizer have been presented. The proposed models included a new circuit arrangement in the functional PLL diagram that aimed at either reducing leakage current effect or adapting bandwidth parameter in the system. However, to the best of the authors' knowledge, non of these investigations proposed an adjustment technique that allows a good tolerance to the undesirable leakage current. So, the main purpose of this paper is firstly, to use the traditional design of frequency synthesizer in its class (integer-PLL). The designed PLL frequency synthesizer is based on the conditions of stability to generate the highest [81-86] GHz 5G mm-Waves band frequency with 1 GHz broadband channel spacing; Secondly, to mitigate leakage current effect caused by the charge pump, we propose an optimization method of loop bandwidth and other PLL parameters that does not allow compensating or reducing leakage current, but rather offers a large tolerance range to this current which will allow a good analysis of PLL characteristics and therefore good performance of all overall PLL system.

The remainder of the paper is structured as follows: Section II presents a related work and proposed specifications. Section III discusses the simulation work. Section IV presents the simulation results. Finally, the conclusion is drawn in Section V.

II. Related Work and Proposed Specifications

This section presents an overview on PLL (1) PLL frequency synthesizer (2) Linear PLL system and its transfer functions covering the two main components: (3) Concept of Phase Frequency Detector/ Charge Pump and (4) Concept of loop filter design.

A. PLL frequency synthesizer

Frequency synthesizers can be classified into three groups; *Direct Synthesizer, DLL based and Indirect Synthesizer (PLL)*. The latter can be either *Functional-N or Integer-N*. Most of the 28 GHz synthesizers processed for 5G applications are fractional and majority of related works are focused on improving PLL characteristics. Authors (El-Halwagy et al., 2016) leaded their research on design a quadrature Fractional-N Synthesizer model for 26- 32 GHz band to provide low integrated jitter and low Phase Noise. Also, authors (Siriburanon et al., 2015) used a reference and frequency doublers for 27.5-29.6 GHz fractional-N frequency synthesizer to get not only a low in-band and out-of-band phase-noise but also a low gain of reference spurs. furthermore, authors (Kuo et al., 2017), proposed other model of PLL for 28 GHz band which consists of a dual loop offset PLO to improve in-band phase noise for 5G systems. In addition to the proposed works for 28 GHz band, other investigation reported by (Herzel et al., 2017) presented a design of frequency synthesizer for both 28/38 GHz frequency bands. The proposed model achieved a low Phase Noise by combining capacitive tuning and inductor switching in the voltage-controlled oscillator (VCO). For much higher frequencies, authors (Iotti et al., 2017) were interested to the E-band in its lowest [71-76] GHz frequencies. They proposed a circuit which consists of a quadrupler with differential outputs based on transformer-coupled push-push stages that allowed to ensure a low-phase-noise frequency synthesizer for integrated E-Band backhaul transceivers. However, all these research works are focused on fractional frequency synthesizers while the integer ones are less complex, consume less power and have low noise. For this reason, in this paper, we chose to design an integer PLL frequency synthesizer for E-band in its highest [81-86] GHz range frequency. As shown in Figure 1, the general concept consists of six major blocks: *A Phase Frequency Detector (PFD), a Charge Pump (CP) and Programmable Dividers* (*R* and *N*) within a PLL- Chip and a *Reference oscillator (TCXO)*, a *Loop Filter (LF)*, and a *Voltage-Controlled Oscillator (VCO)* outside the PLL- Chip.
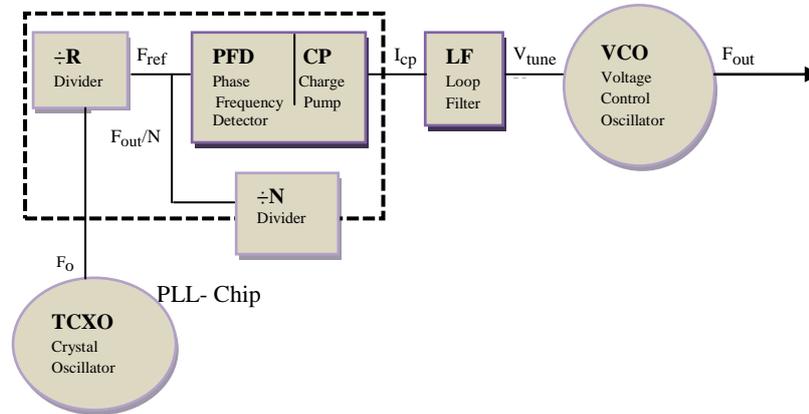

Figure 1: The basic PLL frequency synthesizer

In a PLL synthesizer, the frequency of a reference signal (F_{ref}), which comes from the division report of the frequency (F_0), is generated by the TCXO and divided by R divider. The feedback signal (F_{out} divided by N), are compared in a PFD. The difference between them is converted into a control voltage by a Charge Pump and Loop Filter circuits. The control voltage (Tune voltage 'V_{tune}') in VCO is used to generate various frequency signals. Since the divider R is added to give $F_{ref} = F_o/ R$ and the integer-N divider is added in the feedback path to have F_{out}/ N, the locked condition, F_{ref} and F_{out}/ N must be equal, which means that F_{out} is simply equal to the product of F_{ref} and N.

$$F_{out} = N.F_{ref} = \frac{N}{R} F_0 \tag{1}$$

Linear PLL system and its transfer functions

PLL is a highly nonlinear system. When it is in a locked state, it can be described with a linear approximation (KAMECHE and FEHAM, 2012). As depicted in Figure 2, the linear model of PLL includes a Charge Pump with a gain of $K\varphi$, a Loop Filter with a transfer function of $Z(s)$, and a VCO with a gain of K_{VCO} (Hz/V). In order to model the phase detector, it is important to model the output signals as phases, not frequencies(Zakia and Samir, 2016). When the two input signals into the PFD are almost equal in phase, the error tends to be zero and can be related as:

$$\theta_e = \theta_r - \theta_i \quad \text{When} \quad \theta_e = 0; \; \theta_r = \theta_i \quad \text{hence} \quad \theta_r = \frac{\theta_o}{N} \tag{2}$$
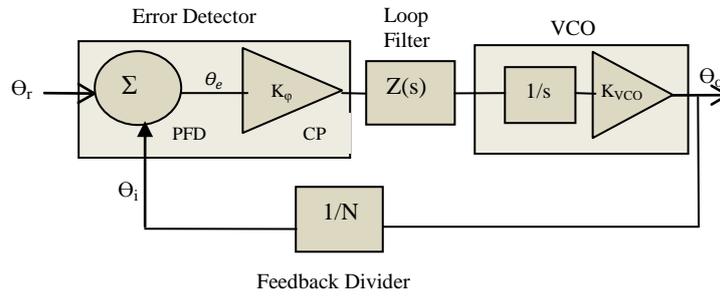
Figure 2: Linear PLL system block diagram

However, when θ_r and θ_i are different, the error detector will output source/sink current pulses to the loop filter. Since, the output of the charge-pump is current, and the oscillator is voltage controlled, the loop filter can transform the current to voltage by its transfer function Z(s), which will be the ratio of the output voltage to input current (Gorji and Zakeri, 2012). This voltage is then applied to1/s integrator, which converts a phase to a frequency in order to adjust its output frequency. Using the PLL block diagram of Figure 2, the PLL system transfer function is calculated as that of the following (SAMIR and al., 2012).

Forward loop gain $\qquad G(s) = \dfrac{\theta_0}{\theta_e} = \dfrac{K_\phi.Z(s).K_{VCO}}{s}$ $\qquad\qquad$ (3)

Reverse loop gain $\qquad H(s) = \dfrac{\theta_i}{\theta_0} = \dfrac{1}{N}$ $\qquad\qquad$ (4)

Open loop gain $\qquad T(s) = \dfrac{\theta_i}{\theta_e} = H(s).G(s) = \dfrac{K_\phi.Z(s).K_{VCO}}{N.s}$ $\qquad\qquad$ (5)

Closed loop gain $\qquad K(s) = \dfrac{\theta_0}{\theta_r} = \dfrac{G(s)}{[1 + H(s).G(s)]}$ $\qquad\qquad$ (6)

C. Phase Frequency Detector (PFD)/ Charge Pump

One of the vital non-linearity issues that exists in modern charge pump circuit is the leakage current, which can influence on all PLL system. The majority of the related work focuses on using nanometer-CMOS technology on the design of the PLL, and a variety of methods/ architectures have been studied for improving the reduction of leakage current for the performance of the system. The proposed investigation carried out on nanoscale CMOS processes in (Chao-Ching Hung and Shen-Iuan Liu, 2009), discussed a leakage current compensation circuit to suppress the leakage current of the PMOS capacitor in the loop filter. Measurement results demonstrate that the root mean-square (RMS) jitter was reduced to 3.10 ps, when the output frequency was 950 MHz. Using the same technology (65-nm CMOS), Zhao Zhang and al. (Liu and al., 2016), proposed another model, which consists on Source-switched charge pump (SSCP) with reverse leakage compensation technique

for spur reduction of wideband PLL. Simulation results show that this method can reduce orders of the magnitude of the reverse leakage and can achieve up to 28 dB spur level reduction for a design of [0.7-1.6] GHz PLL. Authors of (Kim and al., 2007), reported their research on the design of [40-725] MHz PLL based on a 32-nm CMOS technology. This PLL includes a leakage compensator circuit, which consists of two charge pump replicas and current mirrors. By using this technique, experimental results show a great improvement of RMS jitter of 5 ps, while it was 40.9 ps. However, while these investigations relate more specifically to a circuit whereby a compensation of the leakage current can be realized to reduce RMS jitter, other ones focus on improving other PLL characteristics as settling time, Phase Noise and reference spurs caused by a leakage current. According to research reported in (Xiaozhou and al., 2009), the measured results demonstrate a settling time of less than 3 μs, a Phase Noise of –108 dBc/Hz @ 1MHz and a reference spur of –52 dBc. This result is obtained by adding a digital processor block in the PLL frequency synthesizer circuit. Reproaches (Abdul Majeed and Kailath, 2017) proposed a PLL built realized with glitch-free linear PFD and current splitting CP circuits which could offer reference spur of -75.92 dBc @ 20 MHz offset, Phase Noise of -113.5 dBc/Hz @ 100 kHz and lock time of 2.95 μs for 2.56 GHz output frequency. Also, Chun-Yi Kuo and al. (Chun-Yi Kuo and al., 2006) conducted their research on other techniques for 5 GHz frequency synthesizer. They introduced two charge pumps and a dual-control VCO with aid of the smoothed varactors in PLL design. This model has exhibited a Phase Noise of -79 and -113 dBc/Hz at 10-kHz and 1-MHz offset, respectively, a reference spur level of -74 dBc and a total switching time of 110 μs was achieved.

PFD takes inputs from the R and N counters and produces an output θ_e proportional to the phase and frequency difference between them. However, this difference output represents an error voltage, containing a continuous value (V_{tune}) and alternative components. The DC component is ideally linearly proportional to the phase error, as expressed in equation (7) (Pawar and Mane, 2017) .

$$V_{tune} = K_p * \theta_e \qquad\qquad (7)$$

Where:

K_p is the gain of the PFD and θ_e is the time shift between the reference and feedback signals, which will be reflected by Up/Down pulses as a function of the delay or the phase advance between them. However, in the PFD component, a dead zone is one of the noise sources in PLL. It is a phenomenon that occurs when the loop is essentially locked (around zero phase error) and that the phase delay between the input PFD signals becomes very weak. In this situation, the phase error as small as it is, cannot be corrected by the PLL (Pawar and Mane, 2017). To eliminate this dead zone (undetectable phase difference range), delay is inserted in the reset path (DEAN, 1998). As shown in Figure 3. This time delay is chosen so that the Up and Down signals generated last longer than the switching time of the charge pump. Thus, when the signals at the input of the PFD have a low phase delay, the charge pump will have enough time to switch and deliver the appropriate current to the loop filter.
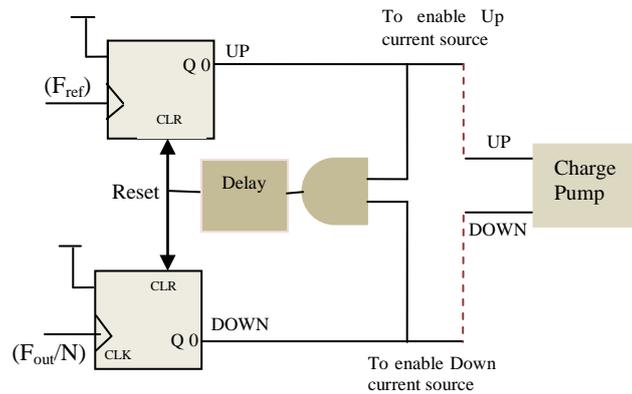

Figure 3: PFD Concept

Figure 4, conceptually, shows the operation of a D flip flop and AND gate integrated on the PFD component The circuit produces Up/ Down outputs and operates as follow: If $\theta_r > \theta_i$, then the Up signal produces a pulse and goes to high state while the Down signal remains in the low (zero) state. Conversely, if $\theta_i > \theta_r$, a positive

pulse appears at the Down output while the Up output remains at zero. On the other hand, if $\emptyset_r = \emptyset_i$, the circuit generates Up or Down pulses with a width equal to the phase difference between the reference and the output signals.

Therefore, the Charge Pump component has to convert the error voltage coming from the PFD into a correction current. At the output of the PFD, the pulses Up and Down are combined into a single signal, which controls the source and sink generators constituting the charge pump. These generators are switched by PMOS (T1) and NMOS (T2) transistorstechnology , as shown in Figure 5.
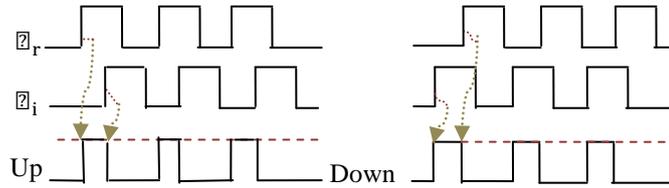
Figur 4. PFD behavior
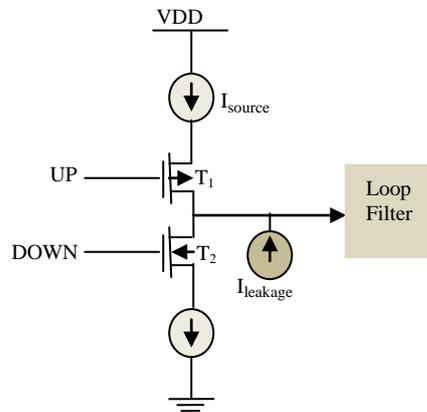
Figure 5: Charge Pump Concept

When the Up signal is high, T_1 turns on, connecting the positive current source to the output ($I_{cp} = I_{source}$). Similarly, if the Down signal goes high, T_2 turns on by connecting the negative current sink to the output ($I_{cp} = -I_{sink}$). Finally, if the two signals Up and Down remain weak, the two switches T_1 and T_2 are blocked and do not let the current flow, which will cancel the current at the output ($I_{cp} = 0$).

However, in the Charge Pump design, some parameters are taken into considerations. The non-ideal effects of the charge leakage current can have an impact on the overall system performance. This undesirable charge current is due to the difference in technology between transistor T_2 (channel-N) and transistor T_1 (channel-P), where the electrons mobility is higher than that of holes. The phase offset, due to the leakage current, is usually negligible but the reference spurs by the leakage current is possibly substantial in frequency synthesizers (Rhee, 1999). The phase offset (φ_ε) due to the leakage current, I_{Leak}, with the charge pump current, I_{cp}, is expressed in (8). In theory, the leakage current must be less than one tenth of charge pump gain as described in (*ADISimPLL 4.30.03 software*, 2017), which is expressed in (9):

$$\varphi_\varepsilon[\text{rad}] = 2\pi * \frac{I_{Leak}}{I_{cp}} \qquad (8)$$

$$I_{Leak} < \frac{I_{cp}}{10} \qquad (9)$$

D. Loop Filter Design

There are many types of filters; compared to an active filter, a passive filter is desirable for its simplicity, low cost and Phase Noise performance (KAMECHE and FEHAM, 2012). In theory, higher order passive filter can suppress spurious better but uses more resistance components, which may lead to Phase Noise degradation and smaller capacitance near the VCO and then cause the VCO output distortion. In this paper, a third order RC loop filter is used. Its topology is given in Figure 6. The loop filter structure is restricted by conditions depending on some parameters. *Loop Bandwidth* and *Phase Margin* are important design parameters in achieving optimum Phase Noise, reference spurs and settling time performance. Many researchers developed works on improving PLL characteristics by adjusting loop bandwidth parameter. An optimization method of PLL loop bandwidth that minimizes the output jitter was proposed in (Kyoohyun Lim and al., 2000) and an RMS jitter of 3.1 ps was obtained. Yan Ge and al. (Yan Ge and al., 2005), employed two charge pumps in PLL topology to define an adaptative bandwidth, which could achieve a fast locking time less than 4 µs. Yiwu Tang and al. (Yiwu Tang and al., 2001) also had used a new adaptation technique by extending a loop bandwidth to achieve a low noise and fast setting time.

Loop bandwidth: it is defined as the frequency at which the magnitude of the open loop transfer function is equal to 1 (which means 0dB). It is given by (DEAN, 2017) and expressed in (10). In order to achieve a high performance PLL synthesizer, the loop bandwidth must be carefuly chosen. According to a well reasoned rule of thumb, the bandwidth should not exceed approximately 1/10 of the reference frequency (F_{ref}) described as the following expression presnted in (Zakia and SAMIR, 2015), and expressed by (11)

$$\| G(j.\omega_{p*} H) \| = 1 \tag{10}$$

$$\omega_p \leq \frac{F_{ref}}{10} \tag{11}$$
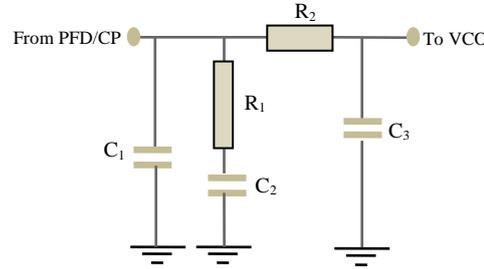
Figure 6. Passive low pass filter

Phase margin: is defined as 180 degrees minus the phase of the open loop transfer function at the loop bandwidth frequency (ω_p), corresponding to 0 dB gain. It is given by (DEAN, 2017) and expressed in (12). The choice of this parameter has a significant impact on the closed loop gain response. Higher phase margins can be decreasing and flatting the peaking around the loop bandwidth but can sacrifice switching speed of the PLL on the other hand. Conversely, if the phase margin is low, this tends to be peaking in the closed loop response and ringing in the PLL transient response (Zakia and Samir, 2018). So, for the loop stability, it would be better to design the synthesizer with a phase margin greater than 0 degree and less than 90 degrees as described in (Zakia and Samir, 2018) and expressed in (13).

$$\Delta\varphi = 180 - \arg G (j * \omega_p) * H \tag{12}$$

$$0° > \Delta\varphi < 90° \tag{13}$$

The generalized loop filter transfer function is defined as the change in voltage at the tuning port of the VCO divided by the current injected by the PLL charge pump. The impedance of the loop filter Z(s) is introduced into the zero and pole in the open loop PLL transfer function, as described in equation (5). So, the zero and pole

directly affect the bandwidth ω_p and the phase margin $\Delta\varphi$ of the PLL. This is shown in the transfer function of the third order loop filter, described in (Dean, 2006) and expressed in (14).

$$Z(s) = A_0 \cdot \frac{1+s.\,T_2}{s.\,A_0.\,(1+s.T_1).(1+s.T_3)} \tag{14}$$

Where $A_0 = C_1 + C_2 + C_3$ is the sum of the capacitors values in the loop filter and the zero $T_2 = C_2 * R_1$ is always necessary for the system stability.

The pole T_1: $T_1 = \frac{C_1*C_2*R_2}{C_1+C_2+C_3}$ \hfill (15)

The pole T_3: $T_3 = R_3 * C_3$ \hfill (16)

III. Simulation

As mentioned before, the leakage current generated by the Charge Pump is one of the major factors, which contributes to the loop stability. Actually, modern PLLs can tolerate up to 1nA (Sotskov and Elesin, 2016). While in theory, this parameter is limited to one tenth of the Charge Pump gain. Therefore, in this paper, the main contribution consists of using ADF4155 as PLL-chip. For this purpose, we propose to design an integer-N-PLL synthesizer able to tolerate more than 1 nA leakage current while maintaining a good performance of the system. This section describes the proposed software implement and the simulation design as well as steps to achieve the proposed contributions of this work.

A. Software implementation

To design and analyze PLL frequency synthesizers, ADIsimPLL software provides an integrated environment using the analog devices ADF series of PLL chips. In this paper, ADF4155 is proposed to be used in conjunction with 5G wireless communication systems. It is used to generate and to control a very stable signal with a low noise in [81-86] GHz mm-wave frequencies with 1GHz bandwidth. From the datasheet (Analog Devices, n.d.), ADF4155 allows implementation of fractional-N or integer-N PLL frequency synthesizers, when used with an external VCO, external loop filter and external reference frequency oscillator. In this work, it is used on integer-N mode with an external prescaler, to select channel spacing. Figure 7 shows a general concept of the adopted synthesizer, while Figure 8 details the functional block diagram of ADF 4155 relating to PLL-chip.
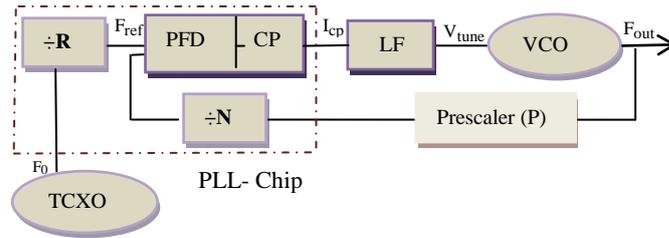
Figure 7. General concept of the adopted synthesizer

B. Design simulation

By using ADIsimPLL 4.30.03 Software tool, ADF4155 is designed for the given specifications:

- Minimum and maximum frequency range (F_{out}) is [81-86] GHz.
- Phase Detector Frequency (F_{ref}), is 50 MHz.
- Channel spacing is specified in the external prescaler (P) with a division ratio of 20.
- Reference frequency (F_0) is 250 MHz.
- Gain of VCO (K_{VCO})is 2 GHz/V.
- -Period of the Anti-Backlash Pulse (delay) introduced in the PFD is 2.90 ns.
- Gain of Charge Pump is 938 µA.

8
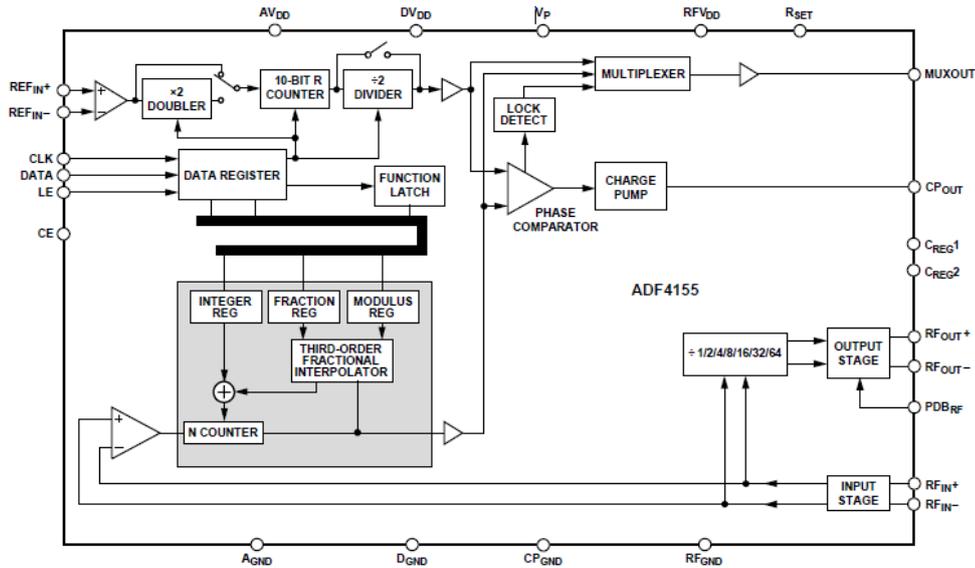
Figure 8. ADF 4155 PLL- chip (Copied from ADF 4155 datasheet)

C. Optimal Parameters for the Synthesizer Design

As mentioned above, the phase margin is one of the most critical of all the design parameters and can impact the settling time. Table 2 presents a summary on how to choose a phase margin for various loop bandwidths. From the formulas (11) and (13), the loop bandwidth is chosen to be $1/100^{th}$, $1/50^{th}$ and $1/10^{th}$ of the reference frequency corresponding to 500 kHz, 1MHz and 5 MHz respectively. The phase margin is chosen to be between [10- 80] degrees. From Table 2, it can be seen that whatever the specified value of the loop bandwidth, there is a specific value (45 degrees) of phase margin that minimizes the lock time. For a phase margin between 70 and 80 degrees, the response time cannot be determined for a bandwidth of 5000 kHz; these phase margin values are, therefore, to be excluded from the outset and the 45 degrees can be considered as 'optimal phase margin' for the design of the loop filter.

TABLE 2. SIMULATED SETTLING TIME FOR VARIOUS PHASE MARGIN AT VARIOUS LOOP BANDWIDTH

Phase Margin (degree)	Settling Time (µs) @ ω_p		
	500 kHz	1000 kHz	5000 kHz
10	35.36	17.57	3.59
15	22.30	11.47	2.30
20	16.23	7.99	1.77
25	12.33	6.03	1.39
30	9.67	4.62	1.14
35	7.79	3.66	0.986
40	6.11	3.08	0.893
45	5.36	2.69	0.936
50	7	3.51	1.15
55	9.09	4.54	1.32
60	11.81	5.86	1.74
65	15.58	7.82	2.36
70	21.42	10.78	∞
75	33.73	16.65	∞
80	73.57	40.03	∞

9

The previous step allowed us to determine the optimal value of the phase margin, but not that of the loop bandwidth. Table 2 shows that 5 MHz (highest bandwidth) responds faster to the locking loop, which suggests to be the most appropriate bandwidth for the design of the loop filter. The subsequent stage, analyses the influence of the leakage current generated by the Charge Pump for 500 kHz, 1 MHZ and 5 MHz loop bandwidths. At this stage, it is important to note that the impact of the leakage current on the loop is manifested by the reference spurs and showed at the multiple of the reference frequency (F_{ref}= 50MHz). Based on the condition expressed in equation (9) we would like to determine the maximum leakage current, tolerated by ADF 4155 in [81-86] GHz 5G band frequency. To recall, the Charge Pump gain introduced in the simulation is 938 µA, where the leakage current should be less than 93.8 µA. The analysis is then done from I_{cp}/1000000 to I_{cp}/10 at $1/100^{th}$, $1/50^{th}$ and $1/10^{th}$ of the reference frequency, corresponding also to the specified values of the loop bandwidth. The obtained results of the settling time and the three first reference spurs are reported in Table 3. from these results, we can conclude that the loop bandwidth is inversely proportional to the response time and directly proportional to the attenuation characteristics of reference spurs. A greater width of the loop bandwidth results in a high level of the reference spurs, which tends to be reduced as much as the loop bandwidth decreases. However, before deciding on the optimal value for the loop bandwidth, in is important to evaluate the intensity of the leakage current tolerated by the system. For this, we examine the reaction of the loop on its stability, in order to draw the maximum undesired current, accepted by the synthesizer.

¶   TABLE 3. SIMULATED SETTLING TIME AND REFERENCE SPURS FOR VARIOUS LEAKAGE CURRENT AT 500 KHZ, 1 MHZ AND 5 MHZ LOOP BANDWIDTH

Leakage Current (µA)	500 kHz Loop Bandwidth				1 MHz Loop Bandwidth				5 MHz Loop Bandwidth			
	Settling Time (µs)	Reference spurs (dBc/Hz)			Settling Time (µs)	Reference spurs (dBc/Hz)			Settling Time (µs)	Reference spurs (dBc/Hz)		
		50	100	150		50	100	150		50	100	150
0.000938	5.36	-131	-149	-159	2.69	-113	-131	-141	0.930	-74	-90	-100
0.00187	5.36	-125	-143	-153	2.69	-107	-125	-135	0.952	-68	-84	-94
0.00938	5.36	-111	-129	-139	2.69	-93	-111	-121	∞	-54	-70	-80
0.0187	5.36	-105	-123	-99	2.69	-87	-105	-115	∞	-48	-64	-74
0.0938	5.36	-91	-109	-119	2.77	-73	-91	-101	∞	-34	-50	-60
0.187	5.42	-85	-103	-113	∞	-67	-85	-95	∞	-28	-44	-54
0.938	6.44	-71	-89	-99	∞	-53	-71	-81	∞	-14	-30	-40
1.87	∞	-65	-83	-93	∞	-47	-65	-75	∞	-7.9	-24	-34
9.38	∞	-51	-69	-79	∞	-33	-51	-61	∞	6.1	-9.7	-20
18.7	∞	-45	-63	-73	∞	-27	-45	-55	∞	12	-3.7	-14
93.7	∞	-31	-49	-59	∞	-13	-31	-41	∞	26	10	278m

In order to determine the maximum tolerated leakage current at the specified loop bandwidth, an analysis is done in the range, where the PLL is in its locked and unlocked state. The obtained results following the settling time and the reference spurs are presented in the Table 4. The results show that using ADF 4155 chip to generate the frequency band [81-86] GHz with 1GHz extra-large channel spacing for the future 5G systems, is able to tolerate more than 1nA leakage current, without compromising the system performance. However, this parameter is limited by the specified loop bandwidth. Making the loop bandwidth too small will result in a design with improved reference spurs rejection and a good tolerable leakage current, but at the expense of the increasing settling time. Conversely, using a wide PLL bandwidth, the system will lock faster, at the expense of higher reference spurs and a much smaller tolerable leakage current. On the other hand, from Table 5, presented below, shows that choosing 45 degrees as an optimum phase margin and 1MHz as an optimum loop bandwidth for the ADF 4155 PLL- chip, it can respond to the trade-off between the settling time and the reference spurs with a very good tolerated leakage current.

10

TABLE 4. ACCURATE PREDICTION OF LEAKAGE CURRENT FOR 500 KHZ, 1MHZ AND 5MHZ LOOP BANDWIDTH

Maximum tolerable Leakage Current (µA)	Settling time (µs)	Reference spurs (dBc/Hz)		
		50	100	150
500 kHz loop bandwidth I_{Leak} Analysis (µA) [0.938-1.87]				
0.938	6.44	-71	-89	-99
1.04	∞	-70	-88	-98
1.17	∞	-69	-87	-97
1.34	∞	-68	-86	-96
1.56	∞	-66	-84	-95
1.87	∞	-65	-83	-93
1 MHz loop bandwidth I_{Leak} Analysis (µA) [0.0938-0.187]				
0.0938	2.77	-73	-91	-101
0.104	2.83	-72	-90	-100
0.117	3.23	-71	-89	-99
0.134	∞	-70	-88	-98
0.156	∞	-68	-86	-97
0.187	∞	-67	-85	-95
5 MHz loop bandwidth I_{Leak} Analysis (µA) [0.00187-0.00938]				
0.00187	0.930	-68	-84	-94
0.00234	1.057	-66	-82	-92
0.00312	∞	-63	-79	-89
0.00469	∞	-60	-76	-86
0.00938	∞	-54	-70	-80

TABLE 5. SUMMARY TABLE OF THE MAXIMUM TOLERABLE LEAKAGE CURRENT FOR EACH LOOP BANDWIDTH VALUE

ω_p (kHz)	Settling time (µs)	Reference spurs (dBc/Hz)			Tolerable Leakage(nA)
		50	100	150	
500	6.44	-71	-89	-99	938
1000	3.23	-71	-89	-99	117
5000	1.05	-66	-82	-92	2.34

IV. Simulation Results

Taking into account 45 degrees as an optimum phase margin and 1 MHz as optimum loop bandwidth, the circuit designed using the ADIsimPLL software is illustrated in Figure 9. Before presenting the impact of 117 nA leakage current on the performance of the system, it should be emphasized that the ADIsimPLL software can also calculate the components' values of the loop filter. Figure 11 shows the resultant components' values of the third passive loop filter used to design the frequency synthesizer in 80 GHz frequency range. In order to see more clearly, this is also presented in Table 6. The obtain results show that the capacitance values C_1, C_2 and C_3 are less than (<) 100 pF and the ones of resistance R_1, R_2 and R_3 are also less than (<) 100 kΩ. Unlike another investigation (Pawar and Mane, 2017) which states that disadvantages of passive filter are hard to integrate when the values of C are larger than> 100 pF and the ones of R > 100kΩ.

TABLE 6. FILTER COMPONENTS' VALUES

ω_p= 1MHz, $\Delta\phi$= 45°				
C_1 (pF)	R_1 (kΩ)	C_2 (pF)	R_2 (kΩ)	C_3 (pF)

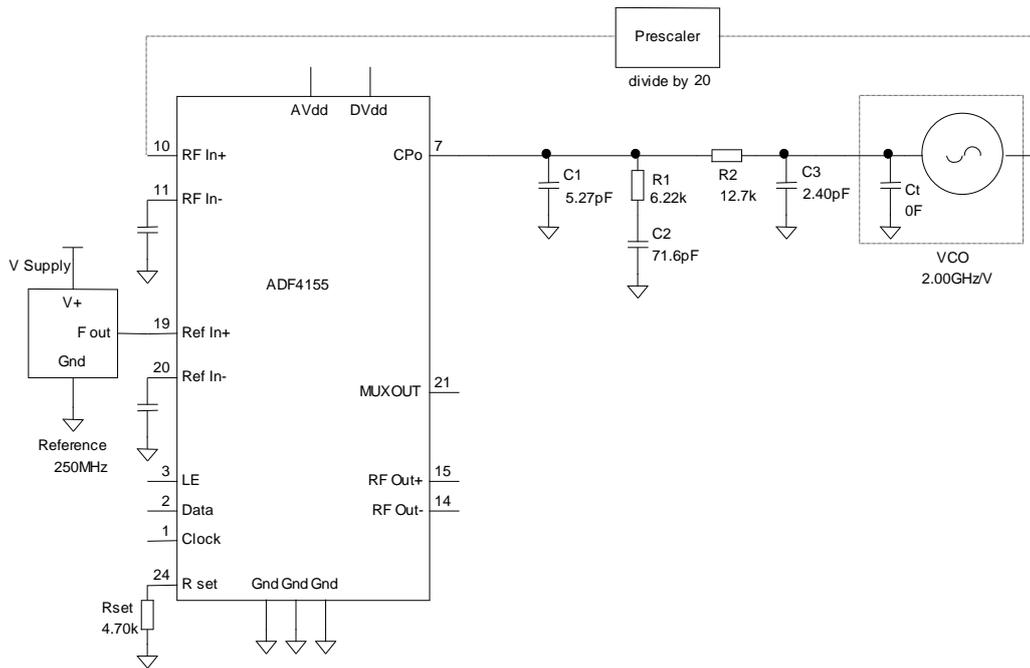| 5.27	6.22	71.6	12.7	2.40

Figure 9. Schematic of the resulting loop filter using ADIsimPLL

Figure 10 shows the VCO frequency output from 81 GHz to 86 GHz during transient conditions. The time required by the frequency synthesizer to lock at 86 GHz is 3.23 µs. The output phase error of the PLL system is given in Figure 11. This plot shows the VCO output phase error during transient conditions. It can be deducted that the phase gets to 76 degrees of the final value within 3.23µs. The output frequency error of PLL during transient condition is given in Figure 12. In the frequency domain, the open and closed loop gain response of the system are presented in Figures 13 and 14 respectively. Figure 13, is useful for analyzing the stability of the system. It can be seen that at the frequency specified of the loop (1MHz), the phase is at its maximum at 0 dB (unity gain) and is about -135degrees, which corresponds to a phase margin of 45 degrees (180-135) degrees. The Closed Loop Gain in Figure 16 has a low pass nature. Within the loop bandwidth, the gain is very large on amplitude thus causing an increased noise level of reference oscillator. When it reaches the loop bandwidth, a low peaking   of the order of 2.34 dB is observed. Then, it drops rapidly. The gain in the loop pass band is largely coming from the N division ratio of the loop. The Phase Noise contribution of each component and the overall Phase Noise of the system are presented in Figure 15. From Figure 15 it can be seen that the noise of the loop filter and the VCO increases within the loop bandwidth. Outside the loop bandwidth, the noise decreases but remains constant for the VCO. Concerning the noise of the reference oscillator, the prescaler and the chip, it decreases slowly and continuously inside and outside the loop bandwidth. Figure 16 shows the reference spurs occured by the charge pump leakage at the multiple of the reference frequency. Figure 17 is obtained by associating the open and closed loop reponses. It shows the response to frequency modulation achieved by modulating the tuning voltage of the VCO in locked condition. The plot has a high-pass response in amplitude as within the loop bandwidth the PLL will try to remove the VCO Phase Noise.
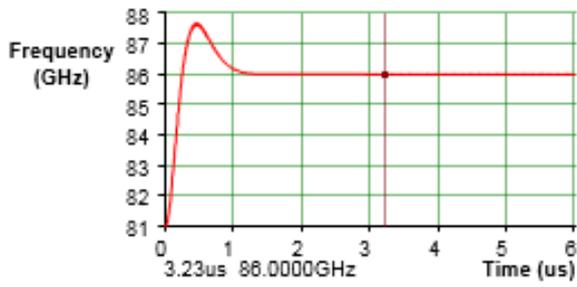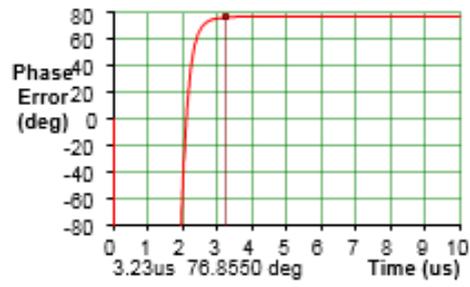
Figure 10. Response time

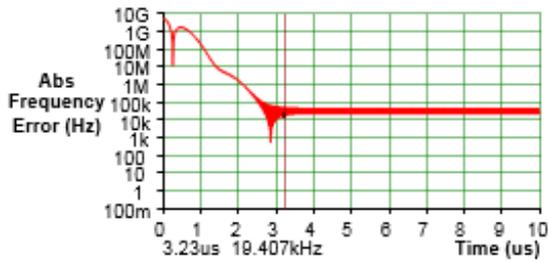Figure 11. Output phase error

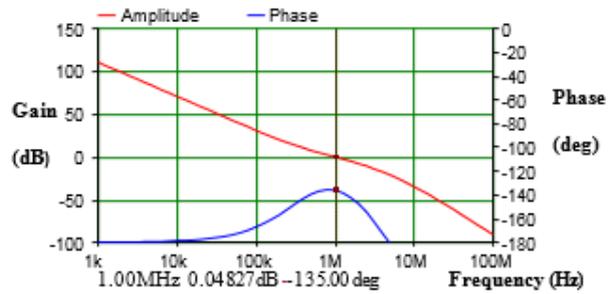Figure 12. PLL output frequency error
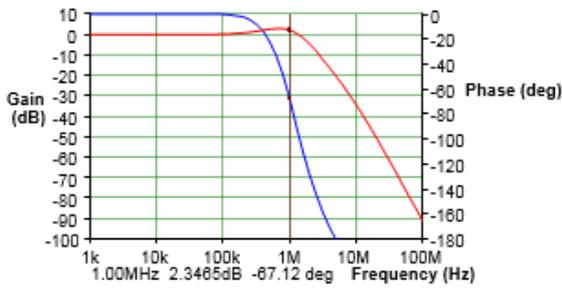

Figure 13. Open loop gain
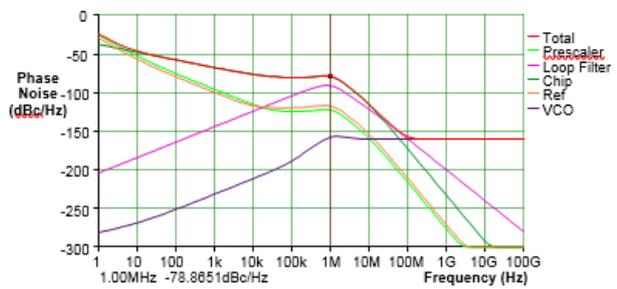

Figure 14. Closed loop gain
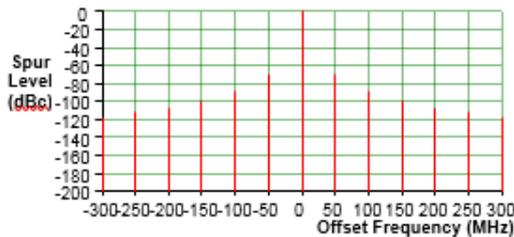

Figure 15. Phase Noise of PLL synthesizer
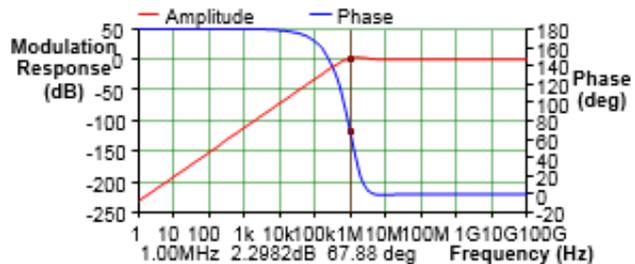

Figure 16. Reference spur levels

Figure 17. Frequency Modulation response

Among the most important characteristics that determine the performance of the PLL system are, *Reference Spurs, Phase Noise, Settling Time* and *RMS Jitter*. Table 7 provides a comparison of the proposed work with a previously published research related to 5G application. It can be observed that the proposed work achieves a better performance in 80 GHz 5G-band frequency compared to the state-of-the-art 28 GHz/ 38 GHz PLL frequency synthesizers, thanks to the use of optimal loop filter parameters. Approach in (El-Halwagy and al., 2016) achieves good *RMS Jitter* but it requires PLL cascade architecture. This work achieves 3.23 μs of settling time and is significantly lower than 1 ms (time latency required by 5G challenges), which makes the proposed synthesizer suitable to be used in future 5G systems.

TABLE 7. COMPARISON BETWEEN THE RESULTS OF THE PROPOSED SOLUTION AND ITS COUNTERPARTS FROM LITERATURE

Ref	Frequency (GHz)	Settling time (μs)	RMS jitter (ps)	Phase Noise (dBc/Hz)	Reference spurs (dBc/Hz)
(Siriburanon and al., 2015)	27.5- 29.6	-	0.51	-78 @100kHz -126 @10MHz	-80 @ 80 MHz
(El-Halwagy and al., 2016)	26.2- 32.4 (Integer mode) (Fractional mode)	-	0.063 0.070	-116.2 @1MHz -112.6 @1MHz	−63.16 @100 MHz −80.91 @ 100 MHz
(Herzel and al., 2017)	28.7-33.7	-	-	-	-63 @ 80 MHz
The proposal approach	81- 86	3.23	0.399	-80.39@100 kHz -78.87@1MHz -114.7@10 MHz	-71 @ 50 MHz -89 @100 MHz -99 @150 MHz

V.   Conclusion

In this paper, we have presented an integer PLL frequency synthesizer for 5G wireless networks. The design method proposed here can be used for the highest 5G mm-Wave frequencies [81-86] GHz by using an extra-large (1GHz) broadband channel spacing. The simulation is performed by using the practical program ADIsimPLL4.30.03. The results demonstrate a high-performance synthesizer in conjunction with ADF 4155 PLL chip. An analysis of a time and frequency domain design technique for passive filter in Charge Pump Phase Locked Loops is done. As a conclusion, it is important to employ the appropriate loop bandwidth and phase margin parameters in favor of a good tolerance of the Charge Pump leakage current. However, depending on the PLL applications, if the fast time is the main criterion to be considered, it is better to use a wide bandwidth but at the expense of the high density of reference spurs and a small tolerated leakage current. Conversely, if the low spurs are the accounted for criterion, it is better to use a small loop bandwidth, since it gives a great tolerated leakage current, but at the expense of a slow acquisition time. To satisfy this trade-off, an optimum value for both the loop bandwidth and the phase margin parameters was chosen. By using 938 μA Charge Pump gain and a third passive loop filter with 45 degree phase margin and 1 MHz loop bandwidth corresponding to one fifty of the reference frequency, ADF4155 PLL synthesizer was able to provide a settling time of 3.23 μs with 5 GHz hopping frequency, an RMS Jitter of 399 fs, a total in-band Phase Noise of -80.39 dBc/Hz at 100 kHz and out-band Phase Noise of -114.7 dBc/Hz at 10 MHz frequency, a density of the reference spur of -71 dBc/Hz at 50 MHz offset frequency and above all, a tolerance of the controlled leakage current of the order of 117 nA.

REFERENCES

Abdul Majeed, K.K., Kailath, B.J., 2017. Low power PLL with reduced reference spur realized with glitch-free linear PFD and current splitting CP. Analog Integrated Circuits and Signal Processing 93, 29–39. https://doi.org/10.1007/s10470-017-1013-4

ADISimPLL 4.30.03 software, 2017.

Analog Devices, n.d. Datasheet ADF4155.

Borkar, S., Pande, H., 2016. Application of 5G next generation network to Internet of Things. Presented at the International Conference on Internet of Things and Applications (IOTA), IEEE, Pune, India, pp. 443–447. https://doi.org/10.1109/IOTA.2016.7562769

Chao-Ching Hung, Shen-Iuan Liu, 2009. A Leakage-Compensated PLL in 65-nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs 56, 525–529. https://doi.org/10.1109/TCSII.2009.2020948

Chun-Yi Kuo, Jung-Yu Chang, Shen-Iuan Liu, 2006. A spur-reduction technique for a 5-GHz frequency synthesizer. IEEE Transactions on Circuits and Systems I: Regular Papers 53, 526–533. https://doi.org/10.1109/TCSI.2005.858322

DEAN, B., 2017. PLL Performance, Simulation, and Design.

Dean, B., 2006. PLL Performance, Simulation, and Design. Dog Ear Publishing.

DEAN, B., 1998. PLL Performance, Simulation, and Design.

El-Halwagy, W., Nag, A., Hisayasu, P., Aryanfar, F., Mousavi, P., Hossain, M., 2016. A 28GHz quadrature fractional-N synthesizer for 5G mobile communication with less than 100fs jitter in 65nm CMOS, in: 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). Presented at the 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), IEEE, San Francisco, CA, USA, pp. 118–121. https://doi.org/10.1109/RFIC.2016.7508265

Ericsson, 2016. 5G Radio Access.

Gorji, S.S., Zakeri, B., 2012. Evaluation of different structures for loop filter on synthesizer specifications. Presented at the 20th Telecommunications Forum (TELFOR), IEEE, Belgrade, Serbia, pp. 1127–1130. https://doi.org/10.1109/TELFOR.2012.6419409

Habiba, U., Hossain, E., 2018. Auction Mechanisms for Virtualization in 5G Cellular Networks: Basics, Trends, and Open Challenges. IEEE Communications Surveys & Tutorials 1–1. https://doi.org/10.1109/COMST.2018.2811395

Herzel, F., Kucharski, M., Ergintav, A., Borngraber, J., Ng, H.J., Domke, J., Kissinger, D., 2017. An integrated frequency synthesizer in 130 nm SiGe BiCMOS technology for 28/38 GHz 5G wireless networks, in: 2017 12th European Microwave Integrated Circuits Conference (EuMIC). Presented at the 2017 12th European Microwave Integrated Circuits Conference (EuMIC), IEEE, Nuremberg, pp. 236–239. https://doi.org/10.23919/EuMIC.2017.8230703

Huawei, 2017. 5G Spectrum, Public Policy Position.

Huawei, 2016. 5G Network Architecture, A High-Level Perspective.

Iotti, L., Bassi, M., Mazzanti, A., Svelto, F., 2017. Design of low-power wideband frequency quadruplers based on transformer-coupled resonators for E-Band backhaul applications. Integration 58, 413–420. https://doi.org/10.1016/j.vlsi.2017.03.003

KAMECHE, S., FEHAM, M., 2012. Perfect A PLL LTE Synthesizer. MicroWave Journal 54–66.

Kawanishi, T., Kanno, A., Freire, H.S.C., 2018. Wired and Wireless Links to Bridge Networks: Seamlessly Connecting Radio and Optical Technologies for 5G Networks. IEEE Microwave Magazine 19, 102–111. https://doi.org/10.1109/MMM.2018.2801638

Kim, K.-K., Kim, Y.-B., Lee, Y.-J., 2007. Phase-Locked Loop with Leakage and Power/Ground Noise Compensation in 32nm Technology. JSTS: Journal of Semiconductor Technology and Science 7, 241–246. https://doi.org/10.5573/JSTS.2007.7.4.241

Kuo, Y.-F., Hsiao, C.-L., Wei, H.-C., 2017. Phase noise analysis of 28GHz phase-locked oscillator for next generation 5G system, in: 2017 IEEE 6th Global Conference on Consumer Electronics (GCCE). Presented at the 2017 IEEE 6th Global Conference on Consumer Electronics (GCCE), IEEE, Nagoya, pp. 1–2. https://doi.org/10.1109/GCCE.2017.8229203

Kyoohyun Lim, Chan-Hong Park, Dal-Soo Kim, Beomsup Kim, 2000. A low-noise phase-locked loop design by loop bandwidth optimization. IEEE Journal of Solid-State Circuits 35, 807–815. https://doi.org/10.1109/4.845184

Liu, L., Wu, N., Yang, J., Liu, J., Zhang, Z., Feng, P., 2016. Source-switched charge pump with reverse leakage compensation technique for spur reduction of wideband PLL. Electronics Letters 52, 1211–1212. https://doi.org/10.1049/el.2016.1036

Nokia, 2017. Beamforming for 4.9G/5G Networks, Exploiting Massive MIMO and Active Antenna Technologies.

Nokia, 2016. The 5G mmWave revolution, Using mmWave spectrum in practical 5G and ultra-dense networks.

Ofcom, 2018. Enabling 5G in the UK.

Ofcom, 2017. 5G spectrum access at 26 GHz and update on bands above 30 GHz.

Pawar, S.N., Mane, P.B., 2017. Wide band PLL frequency synthesizer: A survey. Presented at the International Conference on Advances in Computing, Communication and Control (ICAC3), IEEE, Mumbai, India, pp. 1–6. https://doi.org/10.1109/ICAC3.2017.8318773

Rhee, W., 1999. Design of high-performance CMOS charge pumps in phase-locked loops. Presented at the ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, IEEE, Orlando, FL, USA, pp. 545–548. https://doi.org/10.1109/ISCAS.1999.780807

SAMIR, K., Mohamed, F., Mohamed, K., 2012. Optimizing PLL Performance Levels 54–60.

Siriburanon, T., Liu, H., Nakata, K., Deng, W., Son, J.H., Lee, D.Y., Okada, K., Matsuzawa, A., 2015. A 28-GHz fractional-N frequency synthesizer with reference and frequency doublers for 5G cellular, in: ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC). Presented at the ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference, IEEE, Graz, Austria, pp. 76–79. https://doi.org/10.1109/ESSCIRC.2015.7313832

Sotskov, D.I., Elesin, V.V., 2016. A behavioral model of integer-N PLL frequency synthesizer for reference spur level simulation. Presented at the International Siberian Conference on Control and Communications (SIBCON), IEEE, Moscow, Russia, pp. 1–4. https://doi.org/10.1109/SIBCON.2016.7491738

Wang, S., Zhang, D., He, J., Li, W., Xu, D., Meng, D., Tang, L., 2016. A novel method view to estimate 5G spectrum needs for land mobile service. Presented at the 16th International Symposium on Communications and Information Technologies (ISCIT), IEEE, Qingdao, China, pp. 402–406. https://doi.org/10.1109/ISCIT.2016.7751660

Xiaozhou, Y., Xiaofei, K., Nanjian, W., 2009. A fast-settling frequency-presetting PLL frequency synthesizer with process variation compensation and spur reduction. Journal of Semiconductors 30, 045007. https://doi.org/10.1088/1674-4926/30/4/045007

Yan Ge, Wennan Feng, Zhongjian Chen, Song Jia, Lijiu Ji, 2005. A Fast Locking Charge-Pump PLL with Adaptive Bandwidth, in: 2005 6th International Conference on ASIC. Presented at the 2005 6th International Conference on ASIC, IEEE, Shanghai, China, pp. 431–434. https://doi.org/10.1109/ICASIC.2005.1611343

Yiwu Tang, Ismail, M., Bibyk, S., 2002. A new fast-settling gearshift adaptive PLL to extend loop bandwidth enhancement in frequency synthesizers. Presented at the IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353), IEEE, Phoenix-Scottsdale, AZ, USA, USA, pp. IV-787-IV–790. https://doi.org/10.1109/ISCAS.2002.1010575

Yiwu Tang, Yingiie Zhou, Bibykl, S., Ismail, M., 2001. A low-noise fast-settling PLL with extended loop bandwidth enhancement by new adaptation technique, in: Proceedings 14th Annual IEEE International ASIC/SOC Conference (IEEE Cat. No.01TH8558). Presented at the 14th Annual IEEE International ASIC/SOC Conference, IEEE, Arlington, VA, USA, pp. 93–97. https://doi.org/10.1109/ASIC.2001.954679

Zakia, B., Samir, K., 2018. Optimal choice for phase margin on mm-Wave PLL frequency synthesizer for 5G wireless communications systems. Presented at the Fifth International Conference on Software Defined Systems (SDS), IEEE, Barcelona, Spain, pp. 223–228. https://doi.org/10.1109/SDS.2018.8370447

Zakia, B., Samir, K., 2016. Design and simulation of PLL frequency synthesizer for LTE mobile communications. Presented at the 5th International Conference on Multimedia Computing and Systems (ICMCS), IEEE, Marrakech, Morocco, pp. 745–748. https://doi.org/10.1109/ICMCS.2016.7905521

Zakia, B., SAMIR, K., 2015. The impact of PLL loop bandwidth on Frequency Synthesizer'S performances for LTE/ LTE-Advanced mobile communications. Presented at the 4th International Conference on Electrical Engineering (ICEE), IEEE, Boumerdes, Algeria, pp. 1–4. https://doi.org/10.1109/INTEE.2015.7416708