CAPACITOR VOLTAGE BALANCING, FAULT DETECTION, AND FAULT TOLERANT CONTROL TECHNIQUES OF MODULAR MULTI-LEVEL CONVERTERS

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Abstract

Modular Multilevel Converters (MMCs) are distinguished by their modular nature that makes them suitable for wide range of high power and high voltage applications. However, they are vulnerable to internal faults because of the large number of series connected Sub-Modules. Additionally, it is highly recommended not to block the converter even if it is subjected to internal faults to secure the supply, to increase the reliability of the system and prevent unscheduled maintenance. This thesis introduces a fault tolerant control system for controlling the MMC in normal as well as abnormal operating conditions. This is done through developing a new adaptive voltage balancing strategy based on capacitor voltage estimation utilizing ADAptive LInear NEuron (ADALINE) and Recursive Least Squares (RLS) algorithms. The capacitor voltage balancing techniques that have been proposed in literature are based on measuring the capacitor voltage of each sub-module. On contrary, the proposed strategy eliminates the need of these measurements and associated communication links with the central controller.

Furthermore, the thesis presents a novel fault diagnosis algorithm using the estimated capacitor voltages which are utilized to detect and localize different types of sub-module faults. The proposed fault diagnosis algorithm surpasses the methods presented in literature by its fast fault detection capability without the need of any extra sensing elements or special power circuit.

Finally, a new Fault Tolerant Control Unit (FTCU) is proposed to tolerate the faults located inside the MMC submodules. The proposed FTCU is based on a sorting algorithm which modifies the parameters of the voltage balancing technique in an adaptive manner to overcome the reduction of the active submodules and secure the MMC operation without the need of full shut-down. Most of fault tolerant strategies that have been proposed by other researchers are based on using redundant components, while the proposed FTCU does not need any extra components.

The dynamic performance of the proposed strategy is investigated, using PSCAD/EMTDC simulations and hardware in the loop (HIL) real-time simulations, under different normal and faulty operating conditions. The accuracy and the time response of the proposed fault detection and tolerant control units result in stabilizing

the operation of the MMC under different types of faults. Consequently, the proposed integrated control strategy improves the reliability of the MMC.

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List of Abbreviations

ADALINE	Adaptive linear neuron.
ANN	Artificial neural network.
CSC	Current source converter.
DFIG	Doubly fed induction generator.
ESR	Equivalent series resistance.
FACTS	Flexible alternating current transmission systems.
FDU	Fault detection unit.
FPGA	Field programmable gate array.
FTC	Fault tolerant control.
FCU	Fault tolerant control unit.
HIL	Hardware in the loop.
HVAC	High voltage AC.
HVDC	High voltage direct current.
IGBT	Insulated gate bipolar transistor.
LCC	Line commutated converter.
LS-PWM	Level shifted pulse-width modulation.
LUT	Look-up table.
MMC	Modular multilevel converter.
MTTF	Mean time to failure.
NLM	Nearest level modulation.
PID	Proportional integral derivative.
PMSG	permanent magnet synchronous generator.
PS-PWM	Phase shifted pulse-width modulation.
PWM	Pulse-width modulation.
RLS	Recursive least squares.
SMO	Sliding mode observer.
SVM	Space vector modulation.
THD	Total harmonic distortion.
VSC	Voltage source converter.

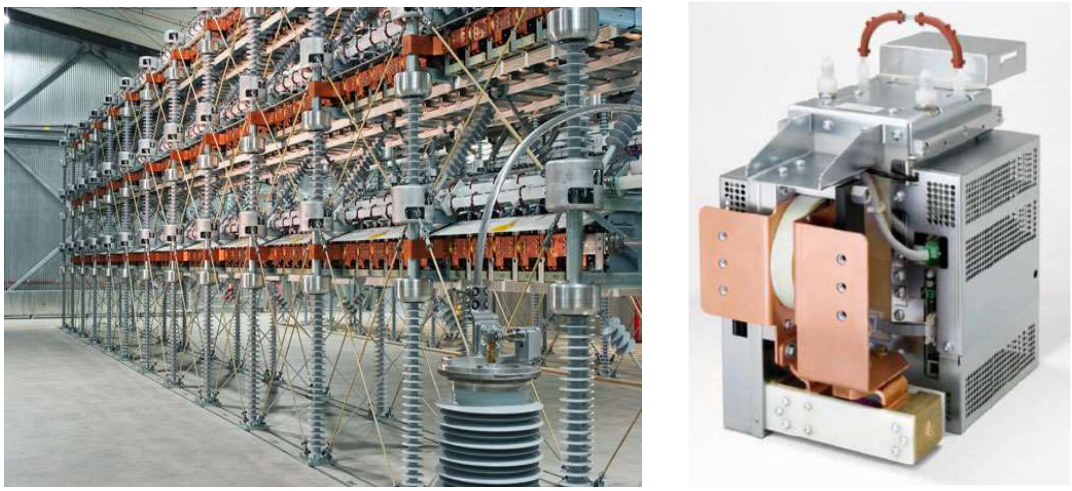
Chapter 1

Introduction

1.1 Background

Voltage source converters (VSC) are increasingly being used in the transmission and distribution of bulk power, due to their advantages over the line commutated converters (LCC). This includes the ability to control active and reactive power independently, supply weak or passive networks, and lower the footprint [1]. Although VSCs have many topologies, the modular multilevel converter (MMC) is considered to be the most suitable converter to be used in high voltage circuits. This is due to their features, including the ability to transmit electric power over high voltage levels directly, the improved quality of output power, and the high efficiency when compared to other multilevel converters [2]. Figure 1.1, which shows a 401-level MMC made by Siemens, illustrates another special feature of MMCs, which is the compact size. This gives a unique advantage for MMCs over other converter topologies when the space allowed for construction is limited.

The MMC is basically formed from a series connection of submodules, which can be either half bridge or full bridge. This is the main reason for calling it modular. Increasing the number of submodules means that the number of voltage levels are increased, which is directly translated into lower harmonic content and enhances the ability to generate higher voltages.



(a) (b)

Figure 1.1: A 401-level MMC made by Siemens [3]*: a) a picture of the MMC, b) a picture for the submodule.*

As illustrated in Figure 1.2, the applications of MMCs have covered most high and medium voltage applications that need the utilisation of power converters. The applications of the MMC include high voltage direct current (HVDC) transmission, MV drives, flexible AC transmission systems (FACTS), and dynamic braking choppers [4]. Furthermore, some research has been recently conducted to utilise the MMC in special applications, such as railway electric traction systems, in which the MMC works as a medium voltage transformer-less converter, which is used to supply the traction motors [5], [6]. In addition, the MMC can applied be in the propulsion systems of electric ships [7], [8].

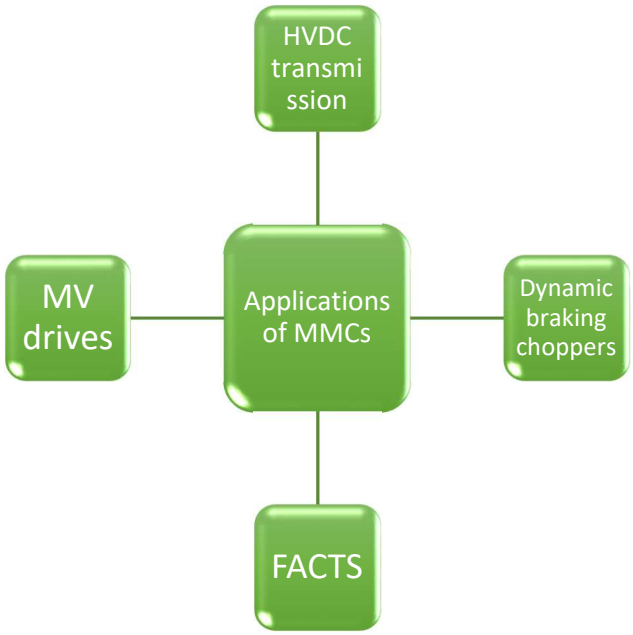


Figure 1.2: Applications of MMCs.

1.2 Motivation and Research Objectives

Today, DC to AC conversions are found in many applications in modern power systems, particularly in the transmission and distribution of electrical energy. Recently, DC/AC converters play an essential role in the interface of offshore wind energy with the utility grid. This is simply because the transmission along HVDC lines is much more efficient compared with the high voltage alternating current (HVAC) transmission over long distances [9].

The current source converter (CSC) was the first converter invented for this particular purpose. The CSC is formed from six thyristors connected in the form of a three-phase bridge connected to the DC supply. Although the CSC is considered very old technology, it is still used in the connection of the renewable energies to the grid in various modern projects [10]. This is simply because of the many advantages, such as the ability to convert high amounts of power, the low manufacturing price, and the high reliability [11]. However, it has some disadvantages and limitations that make it unsuitable for some applications [12], [13]. The main disadvantages are the necessity to have filtering components because of the low order harmonics, the impossibility of changing the current direction, and the inability to independently control reactive power. These limitations have motivated the researchers to invent VSC [13].

The two-level VSC has a simple configuration, which is similar to the CSC but with IGBT instead of the thyristors. This construction has changed the philosophy of switching since the IGBT is fully controllable during turning on and off. On some occasions, the switching device is formed from series-connected IGBTs to withstand high voltage stress [14]. One of the important advantages of the VSC is its ability to control active and reactive powers independently. Moreover, it can supply weak and passive networks. It also has a relatively low footprint compared to the CSC [15]. Despite having all of these advantages, the two-level VSC suffers from some drawbacks that can make it unsuitable for the application of grid interconnection. For example, having series-connected IGBTs increases the switching losses and makes it difficult to predict the transient response of the

switching device. It also is necessary to incorporate DC-link capacitors, which are very big and have a short life expectancy [16]. Moreover, the two-level VSC has no immunity against DC faults, as it fails to support the AC grid with active power [17]. Adding to these drawbacks, the two-level VSCs cannot exchange electricity over high voltage levels directly without using step-up transformers [18].

Due to the problems associated with LCC and VSC, researchers have been directed to multilevel converters (particularly MMCs). The modularity of the MMC offers a generous advantage, which is the ability to generate high voltage levels using a sufficient number of submodules. Although having a series connection of submodules with floating capacitor voltages brings the advantages of a staircase output waveform with low switching frequencies, it increases the level of complexity of the system from the control point of view, as all submodules must be charged to the same voltage level to assure the accurate and stable operation of the converter [19]. Moreover, in order to maintain the output voltage level of the converter, the capacitor voltages must be kept at a reference value [20], [21]. The process of keeping the capacitor voltages within a pre-defined reference is called capacitor voltage balancing control, which is achieved by a dedicated controller called the MMC inner controller [21]. The MMC inner controller should perform some tasks in parallel with the balancing of the voltages across the submodule capacitors. One of the important tasks is protecting the MMC from internal submodule faults, such as power electronic device faults and submodule capacitor faults. As demonstrated in Figure 1.3, which shows the general probability of occurrence for these faults in power converters, power semiconductor devices and capacitors have the highest probability of fault in the MMC with a percentage of 51% [22], [23]. Since the MMC normally works in critical applications, which always require high levels of reliability and supply security, its inner control system should be able to operate with a sustained fault (e.g., insulated gate bipolar transistors (IGBT) failure) until the next maintenance event [24], which means that the inner control system should have fault tolerant control (FTC) capability. This concept increases the reliability of the MMC, as it increases the availability of the converter, even in the case of having an internal fault in order to operate the converter under fail-safe operation conditions. It is important to mention that the process of FTC must be accompanied with a fault detection facility for the purpose

of maintaining safe management of MMC faults. This process not only detects the fault but also localises it to enable the FTC algorithm to isolate the faulty submodule.

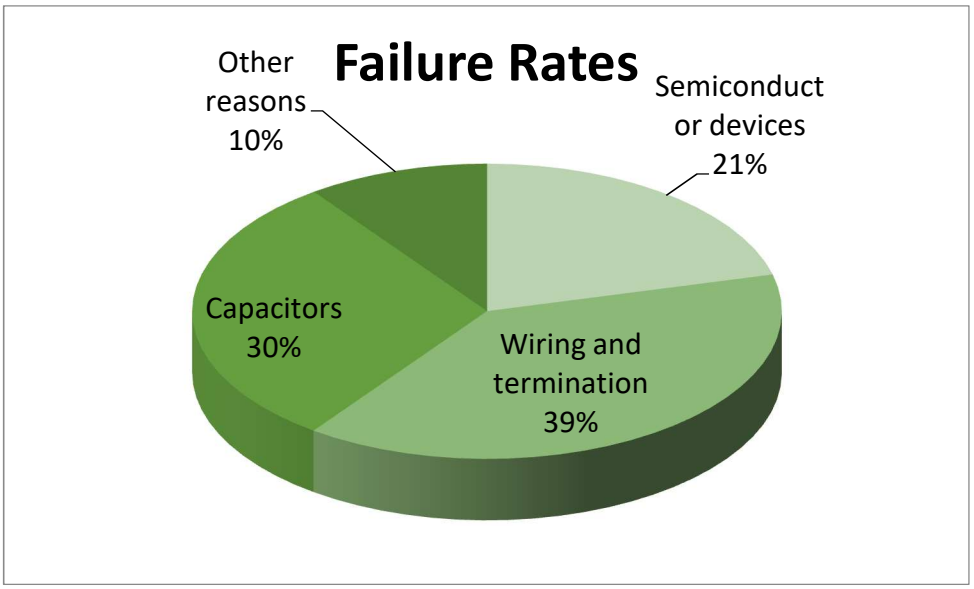


Figure 1.3: Faults probabilities in power converters.

Additionally, the fault diagnosis process has a real challenge to detect the internal DC fault very quickly because, in DC systems, the DC fault current rises to its peak value in a few milliseconds [25].

The volume of the research on fault detection and FTC systems for MMCs is insignificant when compared with the huge challenges surrounding this research area. Moreover, most of the fault detection and tolerant control techniques presented in literature are considered to be expensive, as they require either redundant components or extra sensors [26].

The aim of this thesis is to develop an improved MMC inner controller, which is responsible for balancing the voltages of the submodule capacitors with integrating an ultra-fast fault diagnosis and FTC capability against submodule faults, enabling the MMC to be safely operated in normal conditions as well as abnormal conditions. Furthermore, the developed technique should not need any extra sensors, special power circuits, or even redundant components to make it competitive in cost as well as in performance.

The objectives of the thesis are the following:

- To carry out an intensive literature review in the area of capacitor voltage balancing, fault diagnosis, and tolerant control in MMC systems. This review should index the different faults that can affect the MMC submodules, showing the root cause for each fault and linking it with different techniques proposed in the past.
- To implement a new MMC inner controller, which contains the following subsystems:
    - Voltage balancing of submodule capacitors without the need to measure the actual voltages so that there is no more need for capacitor voltage sensors.
    - Fault diagnostic scheme, which is able to detect and localise submodule faults with effective performance in terms of accuracy and time without adding any extra sensing elements or special power circuits.
    - A FTC scheme, which controls the MMC in abnormal operating conditions when a submodule fault occurs. This scheme should achieve a fail-safe operation until the next shut down for maintenance with increased power quality without incorporating any redundant components.
- To test the developed fault diagnosis and tolerant control techniques on the MMC model to study the effectiveness of these methods by means of PSCAD simulation tool and hardware in the loop (HIL) testing techniques, incorporating a physical controller and a real-time digital simulator to prove the effectiveness of the proposed techniques physically as well as theoretically.

1.3 Thesis Outline

Chapter 2 investigates the structure, theory of operation, mathematical representation, and modulation of MMCs. Furthermore, the design considerations that should be met while selecting the ratings of MMC components are also investigated.

Chapter 3 presents a literature review over the main topics covered in the thesis. First, common capacitor voltage balancing techniques are investigated to characterise the advantages and disadvantages of each technique, aiming to determine the real problems associated with the process of capacitor voltage balancing. Then, the MMC submodule faults are mapped with the root cause and consequences associated with each fault. Finally, popular fault diagnosis and tolerant control strategies that are proposed in literature are also discussed.

In Chapter 4, a new capacitor voltage balancing strategy based on capacitor voltage estimation techniques is presented. Two capacitor voltage estimation techniques based on the adaptive linear neuron (ADALINE) and recursive least square (RLS) algorithms are introduced, and a comparison between the two techniques is also conducted to select the most suitable one to be incorporated into the proposed capacitor voltage balancing technique. Moreover, two simulation models are introduced for the purpose of testing the proposed capacitor voltage balancing techniques under several operation conditions.

Chapter 5 introduces a new fault detection technique based on capacitor voltage estimation algorithms, which is able to detect faults associated with MMC submodules. In addition, the chapter shows some simulation results that show the behaviour and performance of the proposed technique under different faulty conditions.

Chapter 6 presents the proposed FTC technique, which is based on a special sorting algorithm. Moreover, the reliability of the MMC is studied before and after the application of the proposed technique to assess the amount of reliability enhancement. Finally, simulation results of the entire control system are discussed.

Chapter 7 shows the validation of the proposed methods mentioned in Chapters 4, 5, and 6 by means of HIL of simulation through connecting a real-time digital simulator to a real-time controller. It also presents the practical assessment of the proposed MMC inner control when applied in a real application. The assessment mainly focuses on the amount of computational burden of the proposed techniques.

Chapter 8 shows the conclusion of the thesis, focusing on the main contributions to the knowledge. Furthermore, it also presents some recommendations for future research.

1.4 List of Publications

1.4.1 Journal publications

- M. Abdelsalam, M. Marei, S. Tennakoon, and A. Griffiths, 'Capacitor voltage balancing strategy based on submodule capacitor voltage estimation for modular multilevel converters'. *CSEE Journal of Power and Energy Systems*, *2*(1), pp. 65-73, 2016.
- M. Abdelsalam, M. Marei, and S. Tennakoon, 'An Integrated Control Strategy with Fault Detection and Tolerant Control Capability Based on Capacitor Voltage Estimation for Modular Multi-level'. *IEEE Transactions on Industry Applications*, Early access.
- M. Abdelsalam, M. Marei, S. Tennakoon and H. Diab 'A Fault Tolerant Based Control Strategy for Modular Multi-Level Converters'. *PLOS ONE Journal.* – Under review.
- M. Abdelsalam, M. Marei, and S. Tennakoon, 'A Centralized Control Strategy for Hybrid Modular Multi-Level Converters with Fault Detection and Tolerant Control Capabilities', *Journal of Power Electronics* – Under review.

1.4.2 Conference publications

- M. Abdelsalam, S. Tennakoon, A. L. Griffiths, and M. Marei, 'Investigation of submodule fault types of modular multi-level converters in HVDC networks'. *50th International Universities Power Engineering Conference (UPEC)*, (pp. 1-6), IEEE, 2015.
- M. Abdelsalam, S. Tennakoon, A. L. Griffiths, and M. Marei, 'Fault detection, diagnosis and tolerant control of MMCs for HVDC Networks'. *The 5th IET International Conference on Renewable Power Generation*.
- M. Abdelsalam, M. Marei, H. Diab, S. Tennakoon, and A. L. Griffiths, 'Detection and Diagnosis of Submodule Faults for Modular Multilevel

Converters'. *51st International Universities Power Engineering Conference (UPEC)*.

- M. Abdelsalam, S. Tennakoon, H. Diab, and M. Marei, 'An ADALINE Based Capacitor Voltage Estimation Algorithm for MMCs', *The XIXth International Symposium on Electrical Apparatus and Technologies (SIELA 2016)*.
- M. Moussa, M. Abdelsalam, and H. Diab, 'Enhanced Approach for Modelling and Simulation of Modular Multilevel Converter Based Multi-terminal DC Grids', *UKSim-AMSS 18th International Conference on Modelling & Simulation*.

1.4.3 Co-authored conference publications

- H. Diab, M. Marei, M. Abdelsalam, S. Tennakoon, and C. Gould, 'Real Time Simulation of a Current Flow Controller for High Voltage DC Grids Applications', *51st International Universities Power Engineering Conference (UPEC)*.
- H. Diab, S. Tennakoon, M. Abdelsalam, and M. Marei, 'A Current Flow Control Apparatus for Meshed Multi-Terminal DC Grids', *The XIXth International Symposium on Electrical Apparatus and Technologies (SIELA 2016)*.

Chapter 2

Modular Multilevel Converters: Structure, Operation, and Modulation

2.1 Introduction

This chapter presents a literature review on the structure, operation, and modulation techniques of MMCs. First, a brief introduction about multilevel converters is presented. Then, an intensive investigation on the MMC is conducted focusing on its structure, principles of operation, and mathematical model. In addition, a review of the different modulation techniques used for MMCs is also conducted. Finally, the design considerations of MMCs are presented, showing the selection procedure of arm inductors and submodule capacitors.

2.2 Multilevel Converters

The limitations of LCC and VSC (mentioned in Chapter 1) have directed researchers to invent multilevel converters, which are considered very promising for the application of transmission and distribution systems [27]. Unlike two-level VSCs, multilevel converters have advantages, such as the following [28]:

- The ability to transfer high power levels directly without the incorporation of interface power transformers.

- Improved efficiency due to the low switching frequency, which decreases the switching losses.
- Improved quality of output voltage due to the high number of voltage levels requiring no harmonic filters.

Features such as these have motivated researchers to implement a wide range of configurations for multilevel converters, as demonstrated in Figure 2.1. These are explained in the following subsections.

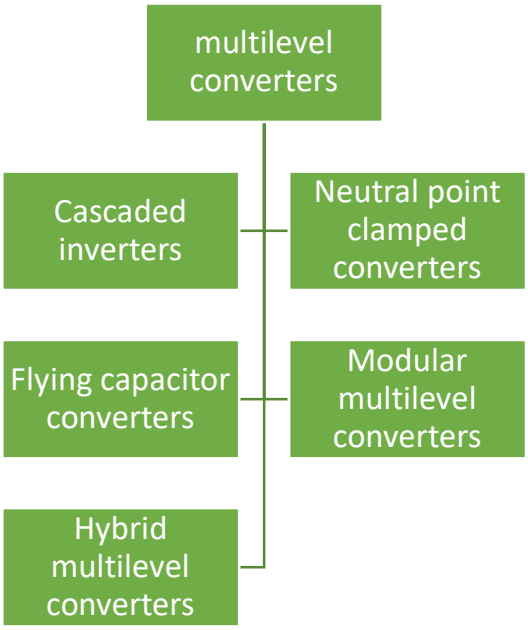
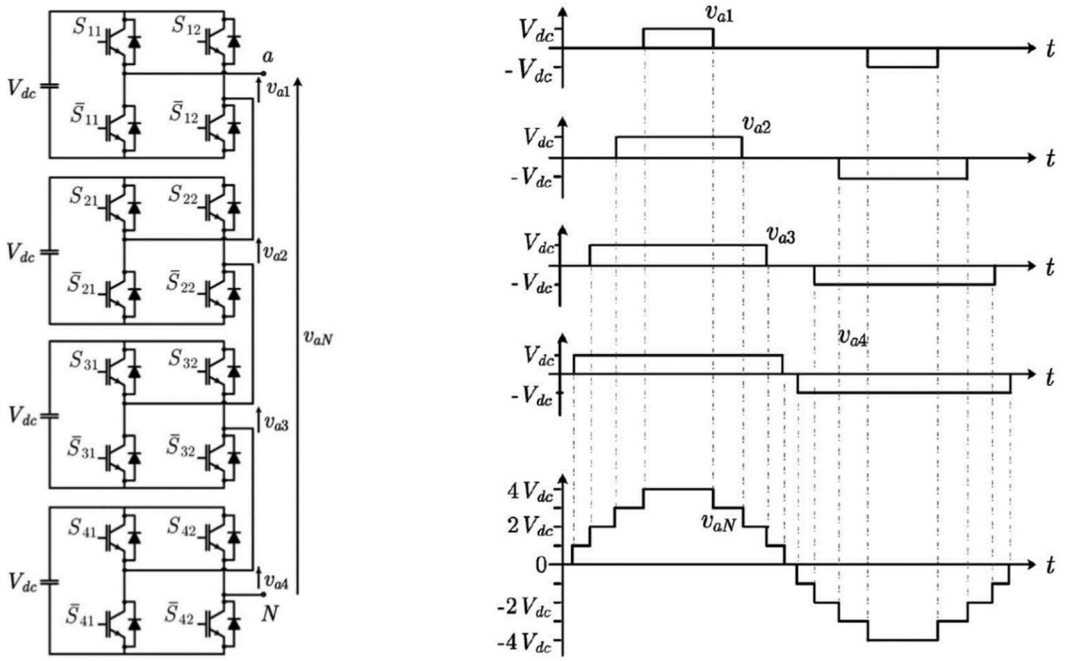


Figure 2.1: Types of multilevel converters.

2.2.1 Cascaded H-Bridge converter

A cascaded multilevel inverter is formed from a series connection of H-bridge submodules. As shown in Figure 2.2(a), the cascaded H-bridge converter is formed from the series connection of full bridges. Each full bridge is connected to a dedicated DC source [29]. The output voltage of each submodule can have three levels: $+V_{dc}$, $-V_{dc}$, or 0. The desired output voltage is achieved by the insertion and bypass of these bridges; thus, the output voltage is built up, as shown in Figure 2.2(b).



(a) (b)

Figure 2.2: Cascaded H-Bridge converter: a) the structure, b) the waveform of output voltage [27].

This topology has a number of advantages, such as its ability to control the zero-sequence component of the current [27], [29]. Moreover, there is no need for balancing algorithms, as it is supplied from multi-phase secondary winding transformers [30]. However, it suffers from many drawbacks, such as the following [31]:

- They usually need a relatively high number of full bridges and isolated DC sources.
- It is not easy to have bi-directional operation of the cascaded inverter because of the usage of isolated DC sources.

2.2.2 Neutral-point clamped multilevel converters

The neutral-point clamped converter is formed from four switches per arm instead of two switches in the two-level converters. As shown in Figure 2.3, the midpoint of the switches is connected to two clamping diodes [32]–[35]. The operation concept is similar to that of the two-level VSC, however, instead of generating two voltages, the neutral-point clamped multilevel converter is able to generate several voltage levels according to the number of capacitors or zero [36].

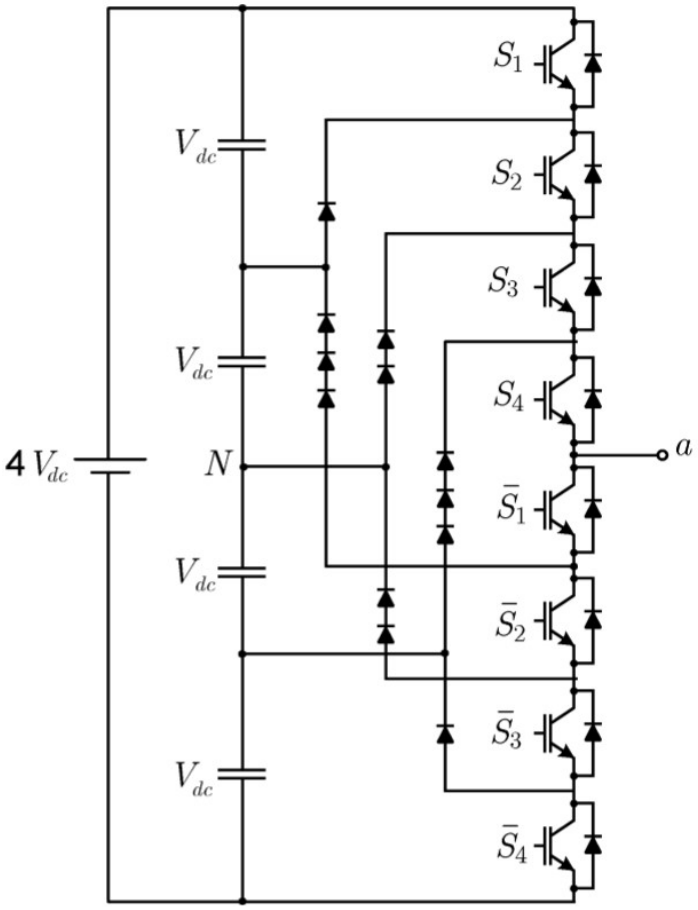


Figure 2.3: Structure of neutral-point clamped multilevel converter [27].

This converter offers some advantages, such as the improved quality of output power, decrease in ratings of the power switches due to the use of the clamping diodes, and elimination of the need for isolated DC sources (which was a main drawback in cascaded H-bridge converters) [37]–[40].

However, this topology has some operating limitations, especially when the DC-link capacitor voltages are not balanced, as this will cause an elevated potential between the neutral and the ground, causing distortion in the output voltage. It is also not scalable. Moreover, clamping diodes are stressed with high voltages. Adding to all of this, the number of components in this converter is relatively high, which affects its reliability [41].

2.2.3 Flying capacitor multilevel converters

The flying capacitor converter has the same structure as the neutral-point clamped converter, where the clamping diodes are replaced with capacitors. Further,

another important difference is that the flying capacitor converter has a modular structure; this has solved the scalability problem of neutral-point clamped multilevel converters. As shown in Figure 2.4, every set of two switches connected to a capacitor forms a module [42].

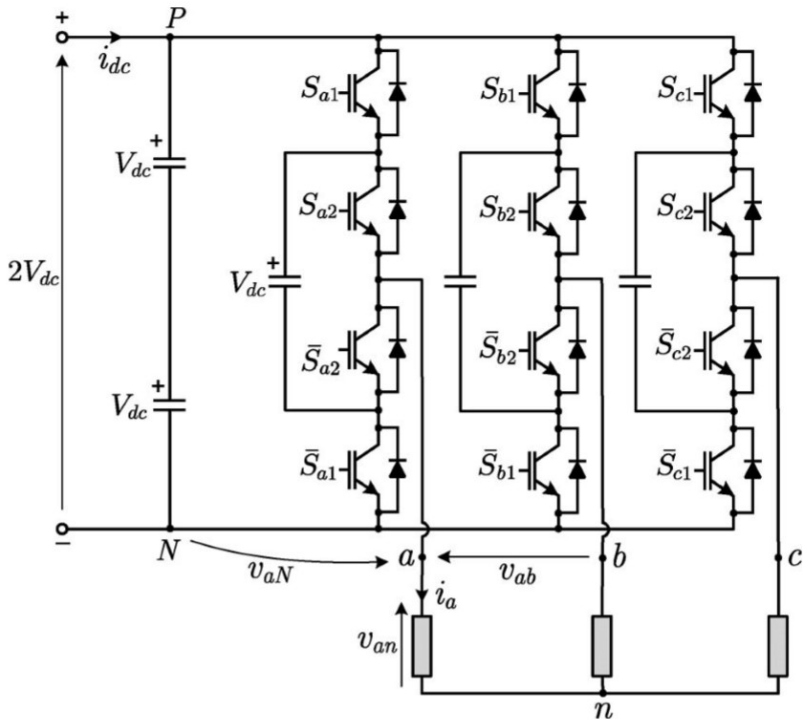


Figure 2.4: The structure of flying capacitor multilevel converters [27].

This gives an advantage of having redundant switching states, which helps in the regulation of capacitor voltages. Moreover, the flying capacitors provide the converter with energy storage, which helps in the ride-through of faults and voltage sags [43], [44]. However, this topology suffers from two main drawbacks [45]:

- It is not possible to have a black start capability, as the capacitors need to be pre-charged.
- There is no equal distribution between the IGBT loading.

2.2.4 Hybrid multilevel converters

The idea of hybrid converters has been recently formed to overcome the limitations and disadvantages of the standard multilevel converters. Although hybrid converters have many topologies, the basic concept of them is employing a two level

conversion stage as a phase controller to change the voltage polarity. On the other hand, the arm links are used to enhance the quality of the output power. This combination offers a reduced number of components which is translated into lower footprint. However, they have some limitations and challenges that are due to the non-standard topologies. One important disadvantage is the complexity of balancing the voltage of dc link capacitors or sub-module capacitors[46]–[51].

2.3 Modular Multilevel Converters

Although multilevel converters have many topologies that have been particularly made for DC/AC transmission, the MMC is considered the most suitable topology for high voltage applications, especially for power transmission and distribution, as it was particularly made to solve all problems associated with other topologies. Their advantages include the potential to eliminate harmonic filters with a sufficient number of voltage levels, DC-link capacitors, and low switching losses [4], [52].

The MMC consists of submodules connected in series forming a leg in each phase. The submodule can be a half bridge or a full bridge, and each submodule has a capacitor that buffers the energy from the DC to the AC side and vice versa; thus, the DC-link capacitor is not required. A high-speed bypass switch is added to the output port of the submodule to isolate the submodule in case of a fault.

As shown in Figure 2.5, each phase leg is divided into two arms, the upper and lower [4], [52]. Each arm has identical numbers of submodules to generate balanced voltages in the two arms of each phase. Inductors are installed in the arms to smooth and filter the currents.

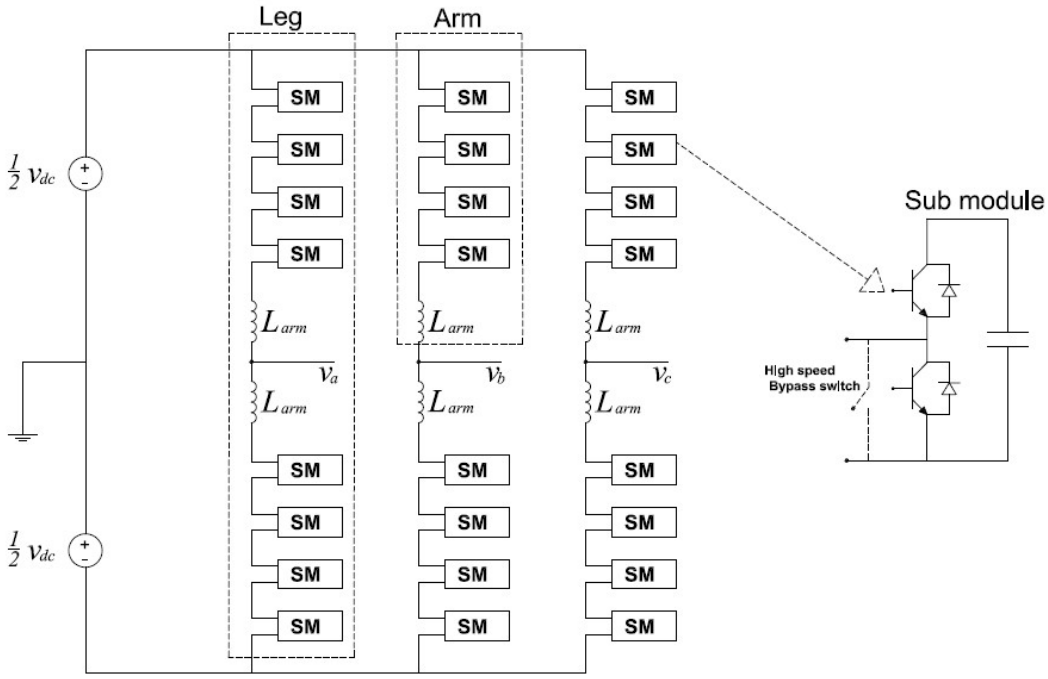


Figure 2.5: Three-phase MMC topology and internal submodule.

2.3.1 MMC modes of operation

To understand the operation of the MMC, it is important to understand the operation of the submodule. The MMC half-bridge submodule has the four following operating modes, and the energy is transferred through them [53], [54]:

- Mode 1: S1 is closed; S2 is opened, and the arm has positive polarity. The current flows into the capacitor charging it, and the submodule capacitor is in circuit (Figure 2.6(a)).
- Mode 2: S1 is opened; S2 is closed, and the arm has positive polarity. The submodule capacitor is bypassed, and the current flows towards the next submodule, keeping the capacitor charge constant and then the submodule is bypassed (Figure 2.6(b)).
- Mode 3: S1 is closed; S2 is opened, and the arm has negative polarity. The capacitor starts to discharge and then the submodule is in circuit (Figure 2.6(c)).
- Mode 4: S1 is opened; S2 is closed, and the arm has negative polarity. The current flows towards the next module, keeping the capacitor charge constant and then the submodule is bypassed (Figure 2.6(d)).

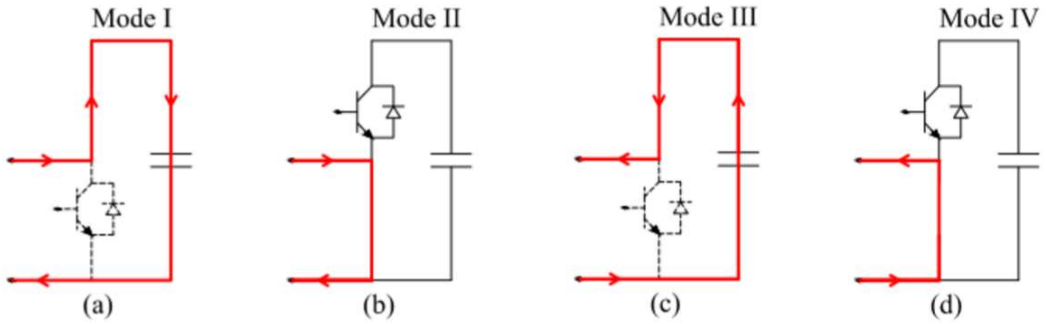


Figure.2.6: Different operating modes of MMC submodules.

2.3.2 MMC mathematical model

The converter arms are represented by variable capacitors as shown in Figure 2.7, which are connected in series with the arm resistance and inductance. The following has been assumed:

1. The number of submodules per arm is infinite.
2. The switching frequency is infinite.

These assumptions will help in simplifying the analysis and in obtaining insight into the fundamental behaviour of the circuit, as the output voltage can be considered to be sinusoidal and to be the ideal voltage balance between the arms.

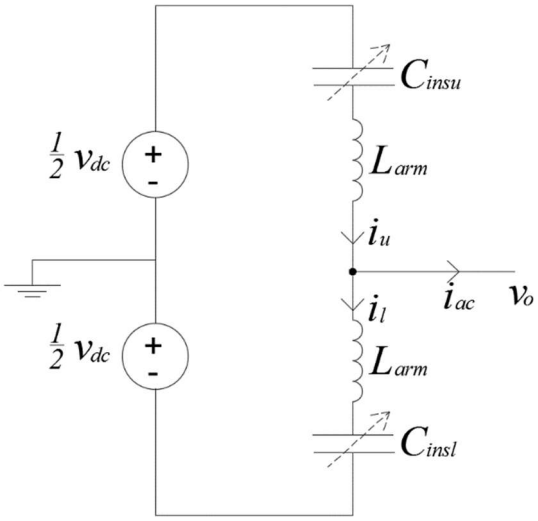


Figure 2.7: MMC average circuit diagram.

The arm capacitance insertion is represented with a modulation value m_u for the upper arm and m_l for the lower arm, while m_x is varied from 0 to 1. When $m_x = 0$, this indicates that all submodules are bypassed, and when $m_x = 1$, this indicates that all submodules are inserted. The value $\sum_{i=1}^{N} v_{cxi}$ is the sum of arm capacitor voltages [55]–[58]. The arm voltages are given by:

$$v_u(t) = m_u . \sum_{i=1}^{N} v_{cui}, \tag{2.1}$$

$$v_l(t) = m_l . \sum_{i=1}^{N} v_{cli}. \tag{2.2}$$

The effective arm capacitance is given by:

$$C_{effu} = \frac{C_{SM}}{N.m_u(t)}, \tag{2.3}$$

$$C_{effl} = \frac{C_{SM}}{N.m_l(t)}, \tag{2.4}$$

where C_{SM} is the capacitance of one submodule and N is the number of submodules per arm.

If the arm currents are $i_u(t)$ and $i_l(t)$ for the upper and lower arms, respectively, the governing differential equation is:

$$\frac{d\sum_{i=1}^{N} v_{cui}}{dt} = \frac{i_u(t)}{C_{effu}}, \tag{2.5}$$

$$\frac{d\sum_{i=1}^{N} v_{cli}}{dt} = \frac{i_l(t)}{C_{effl}}. \tag{2.6}$$

The output ac current i_{ac} is given by:

$$i_{ac} = i_u - i_l. \tag{2.7}$$

The current i_{diff} is the differential current that flows in the phase leg; this current receives an equal contribution from the upper and lower arms because it is assumed that the arm voltages are balanced. In terms of this current, the currents of the upper and lower arms are expressed by:

$$i_u = i_{diff} + \frac{i_{ac}}{2}, \tag{2.8}$$

$$i_l = i_{diff} - \frac{i_{ac}}{2}. \tag{2.9}$$

Adding (2.5) and (2.6) gives:

$$i_{diff} = \frac{i_u + i_l}{2}. \tag{2.10}$$

It is important to mention that the differential current does not contribute to the AC output current. However, it circulates inside the converter, increasing its losses and affecting its performance [4], [59].

The capacitor voltage dynamics can be expressed for the upper and lower arms by:

$$\frac{d\sum_{i=1}^{N} v_{cui}}{dt} = \frac{N.m_u.i_u}{C_{SM}}, \tag{2.11}$$

$$\frac{d\sum_{i=1}^{N} v_{cli}}{dt} = \frac{N.m_l.i_l}{C_{SM}}. \tag{2.12}$$

Applying the Kirchhoff voltage law to the circuit shown in Figure 2.7, the output AC voltage can be expressed as:

$$v_o = \frac{V_{dc}}{2} - R_{arm} i_u - L_{arm} \frac{di_u}{dt} - m_u \sum_{i=1}^{N} v_{cui,} \tag{2.13}$$

$$v_o = -\frac{V_{dc}}{2} + R_{arm} i_l + L_{arm} \frac{di_l}{dt} + m_l \sum_{i=1}^{N} v_{cli.} \tag{2.14}$$

Subtracting (2.13) from (2.14), the differential of i_{diff} can be expressed as:

$$\frac{di_{diff}}{dt} = \frac{V_{dc} - R_{arm} i_{diff} - m_l \sum_{i=1}^{N} v_{cli} - m_u \sum_{i=1}^{N} v_{cui}}{2L_{arm}}. \tag{2.15}$$

From (2.13) and (2.14) and substituting for the currents from (2.7) in (2.15), the differential equations for the phase leg are given by:

$$\frac{d}{dt}\begin{bmatrix} i_{diff} \\ \sum_{i=1}^{N} v_{cui} \\ \sum_{i=1}^{N} v_{cli} \end{bmatrix} = \begin{bmatrix} -\frac{R_{arm}}{2L_{arm}} & -\frac{m_u}{2L_{arm}} & -\frac{m_l}{2L_{arm}} \\ \frac{Nm_u}{C_{SM}} & 0 & 0 \\ +\frac{Nm_l}{C_{SM}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{diff} \\ \sum_{i=1}^{N} v_{cui} \\ \sum_{i=1}^{N} v_{cli} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{2L_{arm}} \\ \frac{Nm_u i_{ac}}{2C_{SM}} \\ -\frac{Nm_l i_{ac}}{2C_{SM}} \end{bmatrix} \tag{2.16}$$

As shown in (2.13) and (2.14), the output voltage, e_v does not depend on the differential current, i_{diff}. Moreover, the value of the differential current depends only on the voltage of the inserted submodules, as given in (2.16). This means that this current can be decreased without affecting the output power.

2.4 Modulation Techniques of the MMC

The modulation techniques used for MMCs are considered extremely important since they are responsible for inserting and bypassing submodules, which means that they control the whole performance of the MMC. Many researchers have developed various types of switching algorithms for MMCs; however, MMC modulation techniques can be divided into three main categories: reference signal-based, carrier-based, and nearest level modulation. The following subsections illustrate the main idea behind each technique. Then, they show the selected technique to be used in the modelled MMC, explaining the reasons for this selection.

2.4.1 Space vector modulation

Space vector modulation (SVM) is commonly used in two-level VSCs. However, some researchers have proposed it for the switching of MMCs due to its attractive advantages, such as [60], [61] the following:

i) ability to be implemented digitally,

ii) reduction of the total harmonic distortion (THD) of output voltage and current waveforms,

iii) optimisation of switching sequences.

Moreover, SVM for two-level VSC is extended to suit the *N* level MMC [61]. As shown in Figure 2.8, the possible switching states for an *N* level MMC is 2^{N-1}. These states are represented in a *3 x N* matrix called H_{abc}:

$$H_{abc} = \begin{bmatrix} h_{a1} & h_{a2} & \dots & h_{aN} \\ h_{b1} & h_{b2} & \dots & h_{bN} \\ h_{c1} & h_{c2} & \dots & h_{cN} \end{bmatrix} \tag{2.17}$$

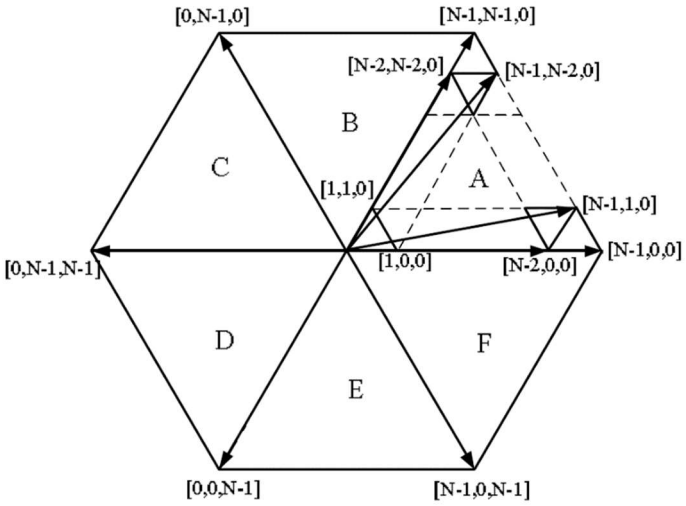


Figure 2.8: Switching plan of space vector for an N level MMC [61].

The reference voltage is generated by multiplying the switching-state matrix, H_{abc} by the submodule capacitor voltages:

$$V_{ref,abc} = H_{abc} x [v_{c1} \quad v_{c2} \quad \dots \quad v_{cN}] \tag{2.18}$$

Similar to the two-level converters, the reference vector is obtained from the nearest stationary vectors, which form a triangle, as shown in Figure 2.9. The dwell times of the stationary vectors are calculated from equations (2.19) and (2.20):

$$\overrightarrow{V_{ref}}\, T_s = \overrightarrow{V_{1,N}}\, t_{1,N} + \overrightarrow{V_{2,N}}\, t_{2,N} + \overrightarrow{V_{3,N}}\, t_{3,N}, \tag{2.19}$$

$$T_s = t_{1,N} + t_{2,N} + t_{3,N}. \tag{2.20}$$

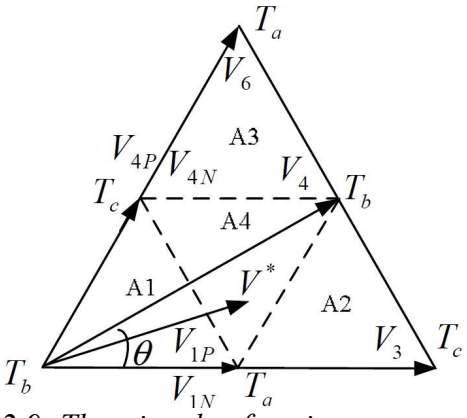


Figure 2.9: The triangle of stationary vectors [61].

It is obvious that the implementation process of the SVM technique is very complex due to the high number of switching states. For example, for a 401-level MMC, the algorithm needs to select from $5\ x\ 10^{120}$. This makes it not recommended for many MMC applications, especially those that have a high number of voltage levels.

2.4.2 Nearest level modulation

The nearest level modulation (NLM) is a simple technique for the direct switching of submodules based on their capacitor voltages and their closeness to the reference signal. First, the required number of voltage levels to be included is determined according to equation (2.21):

$$n_{ON\,x} = round\left[N\left(\frac{1}{2} \pm \frac{V_{ref}(t)}{V_{dc}}\right)\right]. \tag{2.21}$$

The number of bypassed modules is calculated from equation (2.22):

$$n_{OFF\,x} = N - n_{ON\,x} + 1. \tag{2.22}$$

The average value of the capacitor voltages of the inserted submodules will equal the desired reference of the output voltage, as demonstrated in Figure 2.10 [57], [58].

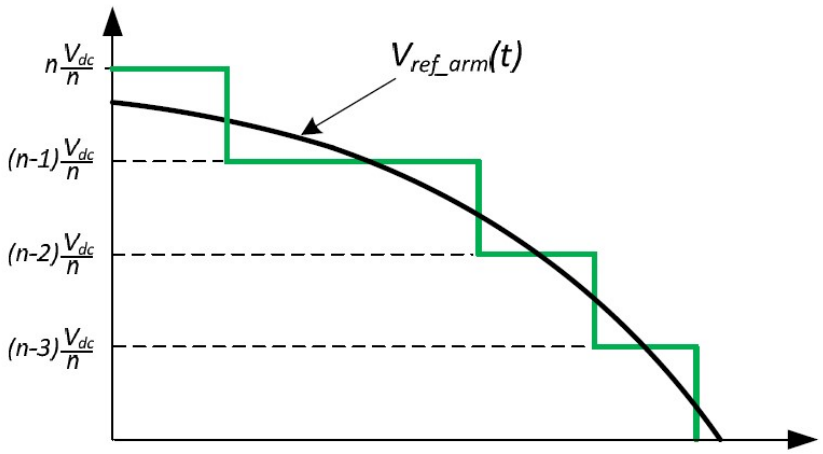


Figure 2.10: The NLM technique [45].

The main advantage of this method is its simplicity, as it can be implemented easily on industrial computers due to the small number of calculations. However, this switching algorithm suffers from a main drawback, which is its relatively high harmonic content that makes it unsuitable for MMCs with a low or medium number of voltage levels [57].

2.4.3 Carrier-based pulse-width modulation

Many carrier-based pulse-width modulation (PWM) based switching algorithms have been proposed in literature [62], [63]. However, there are two major techniques that are commonly used for switching MMCs. The first is the level shifted PWM (LS-PWM). In this technique, each level has a dedicated triangular waveform, as shown in Figure 2.11. The triangular waveforms are displaced from each other by a pre-defined time interval. A sinusoidal reference voltage is compared with the carrier waves to generate the firing signals for the submodules.

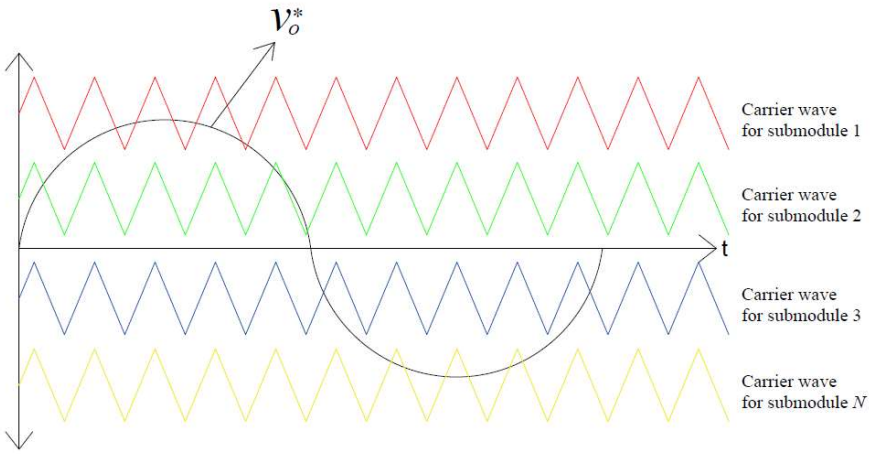


Figure 2.11: The LS-PWM technique.

The second technique is the phase-shifted pulse-width modulation (PS-PWM), which is one of the well-known carrier-based techniques. As illustrated in Figure 2.12, each submodule has a dedicated triangular carrier waveform with the same magnitude but with a different phase shift.

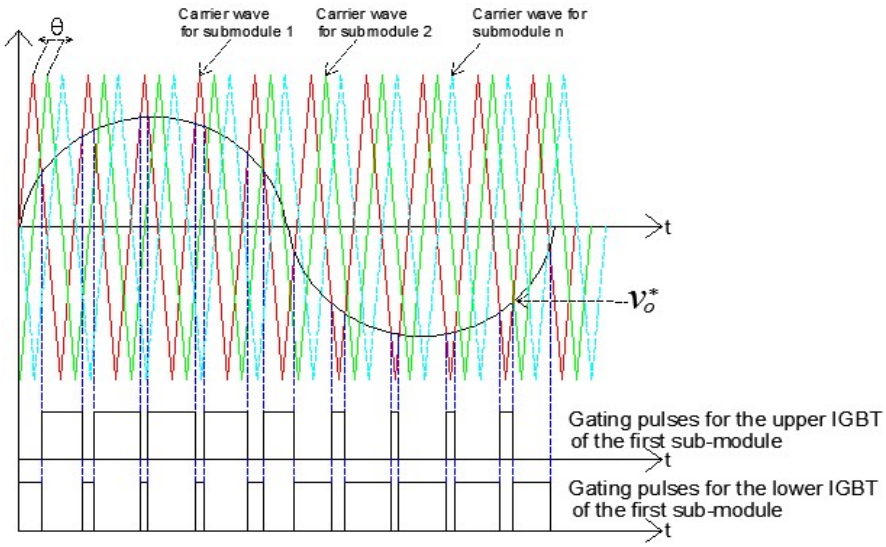


Figure 2.12: The PS-PWM technique.

The switching signals for a submodule result from comparing its corresponding carrier wave with the sinusoidal voltage reference signal v_o^*. The phase shift between each consecutive carrier signals is given by:

$$\theta = \frac{360}{N-1}. \tag{2.23}$$

Table 2.1 presents a comparison between the above mentioned techniques from the point of view of complexity, output power quality and the natural balancing of capacitor voltages.

Table 2.1: Comparison between different switching algorithms used for MMCs.

Switching algorithm	Ease of implementation	Quality of output power	Natural balancing
Space vector modulation	Very complex	High	Good
Nearest level modulation	Simple	Low (particularly for low number of levels)	Bad
Level shifted PWM	Moderate	Moderate	Worst
Phase shifted PWM	Moderate	Moderate	Acceptable

According to the table, the PS-PWM method is selected to be used in the MMC model in this thesis due to the numerous advantages, such as the ease of implementation, the reduced losses due to the reduced switching frequency, and the stable performance during dynamic changes.

2.5 Design Considerations of MMCs

The following subsections show the design considerations of the MMC and the selection process of its parameters, particularly the procedure of selecting the submodule capacitor and arm inductor. It is important to mention that the sizing of these elements is very important for proper operation of the MMC.

2.5.1 Submodule capacitance

The capacitance is calculated based on the energy variation inside the capacitor. Assume that the current passes through the capacitor is i_c and that the voltage across it is v_c. Then, the energy variation inside one capacitor during a period between t_1 and t_2 is:

$$\int_{t_1}^{t_2} v_c \, i_c \, dt = \frac{C\,(V_2^2 - V_1^2)}{2}. \tag{2.24}$$

The capacitor voltage change is from V_1 and V_2. Since the MMC is formed from a series connection of submodules, (2.24) can be applied for the whole arm instead of one submodule. The energy variation inside the upper arm (since both arms are identical) is:

$$\Delta e_u = \int v_u \; i_u \, dt. \tag{2.25}$$

Ignoring the power losses and the arm inductor voltages and assuming that output voltage v_o has a pure sinusoidal waveform, the voltage of the upper arm given in (2.26) can be rewritten as:

$$v_u = \frac{V_{dc}}{2} - v_o. \tag{2.26}$$

The steady state representation of the output voltage and output current is given by:

$$v_o = \widehat{V_o} \cos(\omega t), \tag{2.27}$$

$$i_o = \widehat{I_o} \cos(\omega t - \varphi), \tag{2.28}$$

where $\widehat{V_o}$ and $\widehat{I_o}$ are the maximum values of the output voltage and output current, respectively. Since the power losses are ignored, the active output power can be expressed as:

$$P = \frac{\widehat{V_o}\widehat{I_o} \cos(\varphi)}{2}. \tag{2.29}$$

With the aid of (2.25) and (2.29), the energy variation of the arm as a function of the output active power can be expressed as [64]:

$$\Delta e_u = \frac{P\,(sin(\omega t - \varphi))}{\omega \cos(\varphi)} - \frac{sin(2\omega t - \varphi)}{4} - \frac{\cos(\varphi) sin(\omega t)}{2}. \tag{2.30}$$

Assuming that the allowable percentage of ripple is $k_{ripple\ max}$, according to (2.30), the voltage will vary between V_c and (1+$k_{ripple\ max}$) V_c. The cell capacitance must be chosen such that the maximum value of the energy variation, $\Delta e_{p\ max}$, is smaller than this variation as per (2.31) [64]:

$$\Delta e_{p\ max} < \frac{N\, C_{SM}\, V_c^2 \left(\left(1 + k_{ripple\ max}\right)^2 - 1 \right)}{2}. \tag{2.31}$$

After rearranging (2.31), the value of the capacitor, C_{SM}, must satisfy the following:

$$C_{SM} > \frac{2\, \Delta e_{p\ max}}{N\, V_c^2 \left(1 + k_{ripple\ max}\right)^2}. \tag{2.32}$$

2.5.2 Arm inductance

As mentioned before, arm inductors play a valuable role in the MMC, as they are responsible for limiting the differential and transient currents that may develop during DC faults [65]. They also help in the correction of the total reactance of the system. Thus, the size of arm inductors should be carefully selected to limit DC fault currents to a value that is by far lower than the rating of the MMC IGBT switches [66]. To facilitate the estimation of differential current ripples, the maximum voltage across the arm is assumed to be equal to the submodule capacitor voltage. Additionally, the average value for changing the switching states is assumed to be $\frac{T_s}{2\ N}$ where T_s is the switching cycle of the IGBT. In this case, the peak-to-peak ripples imposed in the differential current can be calculated according to:

$$\Delta i_{diff} = \frac{v_c T_s}{4\ N L_{arm}}. \tag{2.33}$$

Each arm inductor is subjected to half of the peak-to-peak ripples. In this case, after rearranging (2.33), the arm inductor should be selected according to [66]:

$$L_{arm} > \frac{V_c T_s}{8\ N \Delta i_{diff}}. \tag{2.34}$$

2.6 Chapter Summary

This chapter has presented a detailed review of different types of multilevel converters used for DC/AC conversion with particular focus on the MMC, including its structure, operation, and control concepts. Furthermore, it presented the popular switching algorithms used for the firing of MMC submodules, mentioning the selected switching algorithm used in the simulation. Then, the design considerations of the MMC were presented, focusing on the procedure of selecting the size of submodule capacitors and arm inductors.

Chapter 3

Review of Capacitor Voltage Balancing, Fault Detection, and Fault Tolerant Control Techniques of Modular Multilevel Converters

3.1 Introduction

This chapter presents a literature review on the main topics of the thesis. First, a review of the different techniques of capacitor voltage balancing in MMCs is presented. Then, the MMC submodule faults are investigated, explaining the root cause of each fault consequence. In addition, the concepts of fault detection and tolerant control are discussed with a comprehensive investigation of common MMC fault diagnosis and tolerant control strategies.

3.2 Capacitor Voltage Balancing of MMC Submodules

Having series-connected submodules with unequal floating capacitor voltages cannot be accepted, as this condition will increase the differential current and thus, increasing the ripple content in the submodule capacitor voltages which means that the harmonics inside the DC-link voltage will be increased [19]. Thus,

capacitor voltages should follow a pre-defined reference signal. Moreover, these voltages should be balanced to lower the differential current and converter losses [20]. Many strategies have been proposed in order to balance the voltages of the submodule capacitors by forcing the capacitor voltages to follow a desired value for the purpose of reducing ripples in these voltages, eliminating the AC components that are found in the differential current and enhancing the quality of the output power [67]. The following subsections show the most popular control strategies that are used in the industry.

3.2.1 Capacitor voltage balancing based on energy control

In this method, the capacitor voltages are balanced by controlling the total energy stored in the leg and the differential energy between the upper and lower arms [68]. As shown in Figure 3.1, the first step in this method is the measurement of submodule capacitor voltages, and then the energy stored in each arm is calculated with the aid of these voltages.

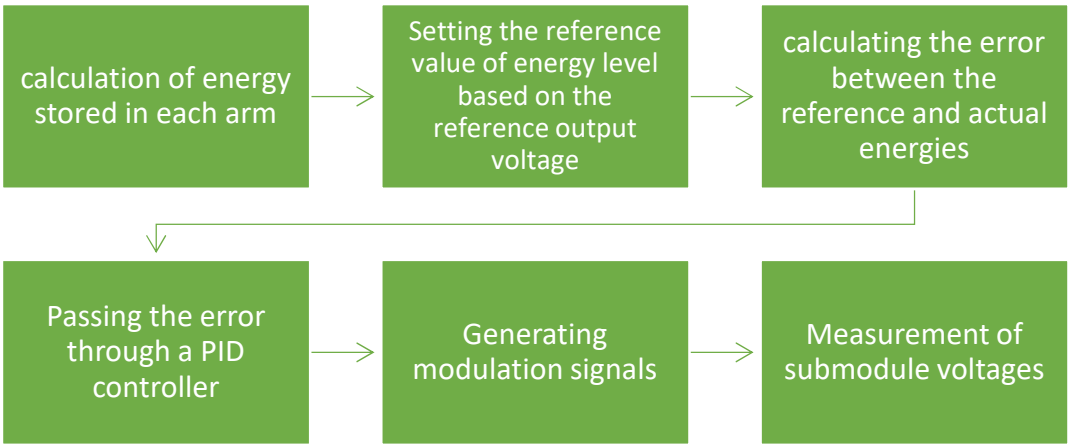


Figure 3.1: Block diagram of capacitor voltage balancing based on energy control.

A reference signal for the desired energy level is received as input to the controller. This reference is calculated based on the reference value of the output voltage, v_o^*. By knowing the energy stored in the arms and the reference value of the energy, the modulating signals (m_u and m_l) for the upper and lower arms are

generated. These modulating signals are then passed through a suitable switching algorithm to insert or bypass different submodules [68].

The performance of this method is good, as it always succeeds in balancing the voltages, even in fast dynamic actions; however, it suffers from some drawbacks, such as a distortion in the output current because of the continuous inserting and bypassing of submodules [68]. Moreover, this method is complex due to the large number of calculations and high number of control loops. It also needs continuous measurements of a large number of signals, such as submodule capacitor voltages and arm currents.

3.2.2 Capacitor voltage balancing based on distributed control

This method was particularly developed to solve some of the problems associated with the energy balancing control, particularly the distorted output power and the complex calculations and control loops [20]. As illustrated in Figure 3.2, the distributed control technique consists of two main parts.

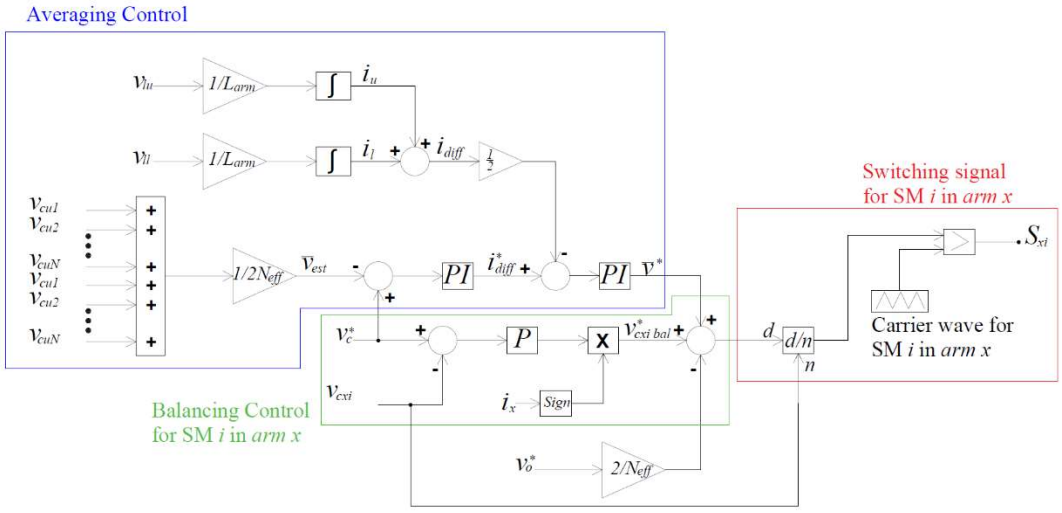


Figure 3.2: Block diagram of capacitor voltage balancing on based distributed control.

The first is the average control of the submodule capacitors, while the second is the balancing control. The average control uses a proportional-integral-derivative (PID) controller to make the average voltage of the whole leg reach the desired reference voltage, v_c^*. The balancing control has N control loops; each loop utilises a P controller for each submodule to enable its capacitor voltage to reach the desired

voltage. Both averaging and balancing control loops need the measurement of the submodule capacitors. The performance of this method is more attractive compared to the energy control, as it is very fast in tracking the reference voltages and thus balancing the voltages, and simultaneously, the distortion in the output power has significantly enhanced [20]. The main drawback of this method is the high content of differential current, as it remains at 70% of its original value. Moreover, it is considered complex when applied to MMC with a high number of voltage levels since each leg must be equipped by ($2N$ + 1) P/PI control loops [69]. This method will be explained in detail later, as it is a part of the proposed control.

3.2.3 Capacitor voltage balancing based on reduced switching frequency modulation

This technique was developed to provide a simple method for balancing the capacitor voltages instead of depending on complex techniques, as illustrated in the two previous methods.

In this method, first, the arm current is observed to determine whether it is charging or discharging the submodules. In the case of charging the capacitors, the algorithm calculates the number of submodules that need to be inserted on N_{new} based on the measured capacitor voltages. Then, it calculates the difference between this number and the old number of submodules that is already inserted ($\Delta N_{on} = N_{on} - N_{on_{old}}$). If the ΔN_{on} is zero, then the switching is kept as it is and nothing changes. However, if the ΔN_{on} is greater than zero, the arm current is checked to determine whether it is charging or recharging the arm capacitors. If the arm current i_{arm} is higher than zero, the algorithm inserts ΔN_{on} submodules that have the lowest voltages, while the algorithm bypasses ΔN_{on} submodules that have the highest voltage if the i_{arm} is less than zero. Finally, if the ΔN_{on} is lower than zero and the arm current i_{arm} is higher than zero, the algorithm inserts ΔN_{on} submodules that have the highest voltages, while the algorithm bypasses ΔN_{on} submodules that have lowest voltages if the i_{arm} is less than zero [70]. Figure 3.3 shows the flow chart of the reduced switching frequency technique.

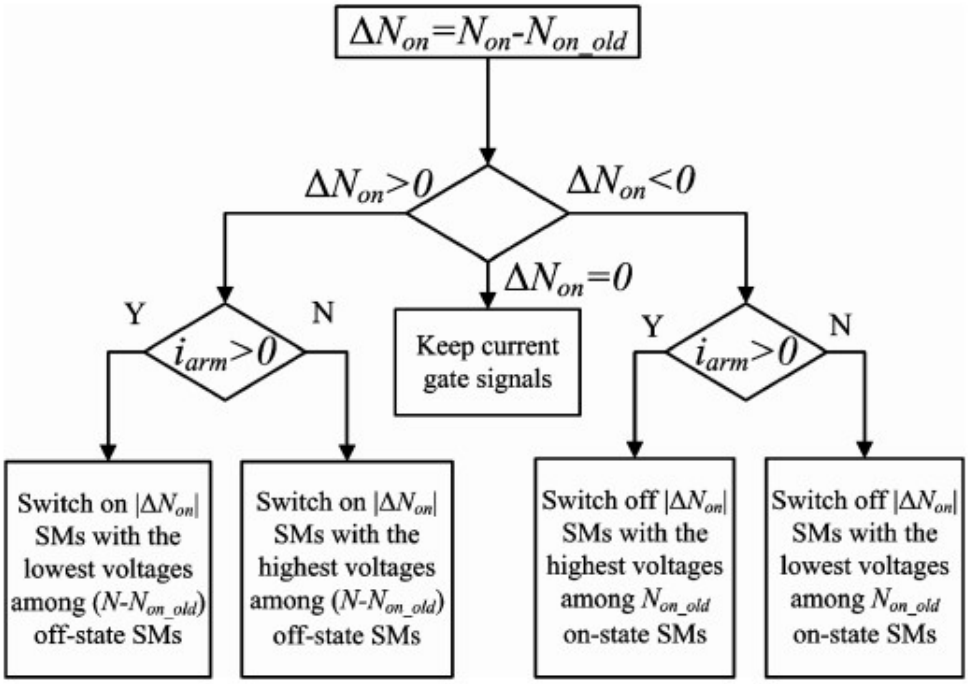


Figure 3.3: Block diagram of capacitor voltage balancing based on reduced switching frequency [70].

It is clear that this method enhances the performance of the MMC since the converter losses are lowered due to the relatively low switching frequency. Moreover, there are no complex calculations or sophisticated PID control loops, which makes it simpler than other techniques. However, the ripples of capacitor voltages are increased due to the increased voltage bandwidth, which means that the differential current will be increased. Another drawback is that it still needs the measurement of each capacitor voltage.

3.2.4 Capacitor voltage balancing based on sorting algorithms

Like the previous method, this method aims to reduce the switching frequency of the submodule IGBTs through applying a simple sorting algorithm while considering reducing the ripple content. The algorithm depends on two sorting structures and a comparator that selects the submodules that need to be inserted. The first stage of applying the algorithm is the sorting stage. From its name, as shown in Figure 3.4, the role of this stage is to sort the submodules in a pre-defined order to be ready for either insertion or disconnection [71].

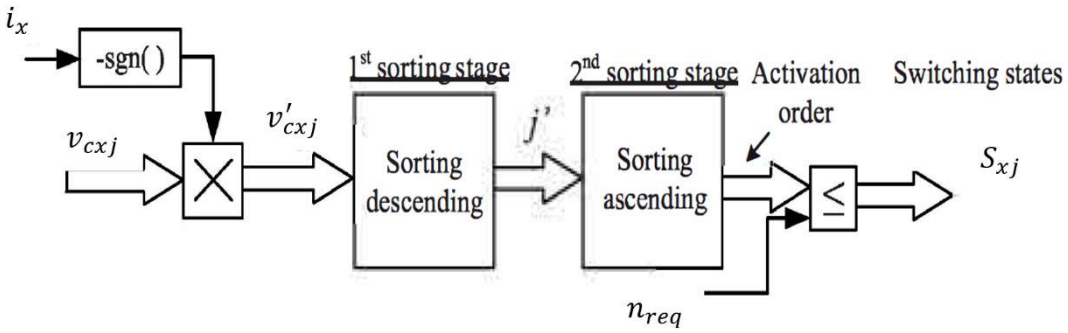


Figure 3.4: Block diagram of the *conventional sorting algorithm based capacitor voltage balancing algorithm* [71].

First, the capacitor voltages are multiplied by the sign of the arm current. The modified submodule capacitor voltage is given by:

$$v'_{cxj} = (-sign\, i_x)\, v_{cxj}, \tag{3.1}$$

where x denotes the location of the arm, whether it is upper or lower, and j is the number of submodules. The modified capacitor voltages, v'_{cxj}, are then sorted in descending order. The algorithm scans the sorted list of the submodules to prepare them for activation. Submodules that will be activated are those with an activation order below or equal to the number of required submodules, n_{req}.

The direct application of this algorithm fails to reduce the switching losses, as it creates many additional switching states, which increase the switching frequency. Thus, a modification to this algorithm has to be made to restrict the number of connected submodules. This restriction is achieved by multiplying the switching states by a factor, ΔK, which is varied between 0 and 1, to enable the sorting algorithm to distinguish between the voltages of the inserted and bypassed submodules [71].

The block diagram of the modified algorithm is shown in Figure 3.5. In this case, the sorting stage will see a virtual voltage with a value of:

$$v''_{cxj} = v'_{cxj} + \Delta K.\, S_{xj}. \tag{3.2}$$

This means that, when submodules are connected, the virtual voltage will be:

$$v''_{cxj} = v'_{cxj} + \Delta K, \tag{3.3}$$

while, for bypassed submodules, the virtual voltage will be:

$$v''_{cxj} = v'_{cxj}. \tag{3.4}$$

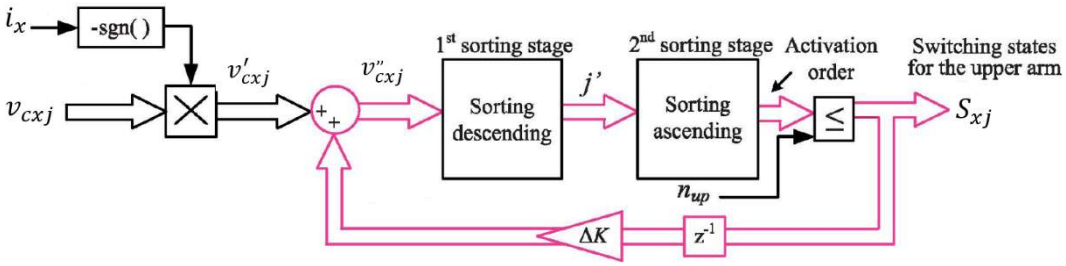


Figure 3.5: Block diagram of the *modified sorting algorithm based capacitor voltage balancing algorithm* [71].

The selection of the ΔK should be carefully chosen for the necessary separation gap between the inserted and bypassed capacitor voltages. This method has a robust performance in terms of balancing the capacitor voltages, reducing the switching losses, and lowering the ripple content. However, it requires the measurements of all submodule capacitor voltages and the arm current, which increases the cost of the strategy. Moreover, applying the submodule restriction concept adds some complexity to the algorithm.

All capacitor voltage balancing techniques discussed in this chapter have a common drawback, which is their need for capacitor voltage measurements. These measurements not only add a large number of sensors but also require a high number of communication channels to transmit these signals. This has prompted the author to develop a new capacitor voltage balancing technique (presented in Chapter 4) that does not depend on the measurement of submodule capacitor voltages.

3.3 The MMC Submodule Faults

According to the literature, there are different types of submodule faults that can strike MMCs and affect their operation [26]. Since MMCs are used in important applications and are a big investment, it is extremely important to detect these faults very quickly to protect the whole system from sudden failures. For this particular purpose, the submodule faults are investigated in the following subsections. Moreover, popular fault detection techniques are discussed to discover the advantages and disadvantages of each method and to highlight what is needed in the process of fault detection of MMCs.

3.3.1 Faults in power electronic devices

The IGBT operation is always linked to the presence of freewheeling diodes. This is simply because the IGBT cannot function correctly without having a freewheeling diode dissipating the excess power due to the IGBT turn-off action. All of faults inside the power electronic device faults always depend on the semiconductor physics. Power electronic device faults are either open circuit faults or short circuit faults.

Table 3.1 shows the main causes of each fault type and their corresponding consequences [72]–[74].

Table 3.1: Faults in submodule IGBTs.

Fault Type	Failure Mechanism	Consequences
Open circuit	Bond wire rupture	1) Pulsating current 2) Distortion in output current and voltage
	Gate driver failure	
Short circuit	High voltage breakdown	Overheating in a few cells at first, spreading to other cells and leading to complete failure
	Static/ dynamic latch up (a low impedance path between the two regions)	
	Energy shocks	

In case of having an open circuit fault in the upper submodule switch, the negative capacitor current is blocked. As a result, the only path for this current is the lower freewheeling diode.

The same case occurs for the lower switch of the submodule, but the capacitor current is positive. Table 3.2 illustrates the behaviour of arm currents and submodule voltages in case an open circuit fault.

Table 3.2: Relationship between submodule output voltage and arm currents during open circuit faults.

The state of the submodule	The sign of the arm current	The submodule output voltage		
		Normal operation	Upper switch open circuit fault	Lower switch open circuit fault
Bypassed	+ve	V_c	V_c	V_c
	-ve	V_c	0	V_c
Inserted	+ve	0	0	V_c
	-ve	0	0	0

Regarding switch short circuit faults, the behaviour is different, as the output voltage will equal the capacitor voltage when the upper switch is short circuited. When the short circuit is applied to the lower switch, the submodule output voltage is equal to zero. Table 3.3 describes the relationship between the arm current and submodule output voltage during switch short circuit faults.

Table 3.3: Relationship between submodule output voltage and arm currents during short circuit faults.

The state of the submodule	The sign of the arm current	The submodule output voltage		
		Normal operation	Upper switch open circuit fault	Lower switch open circuit fault
Bypassed	+ve	V_c	V_c	0
	-ve	V_c	V_c	0
Inserted	+ve	0	V_c	0
	-ve	0	V_c	0

It is important to mention that in case of open circuit faults, there is no threat on the safety of the converter or the whole system since the consequences are related to the power quality so there is no real need to shut off the converter. On the other hand, if the submodule is subjected to a short circuit fault in the power electronic device, it is a must to disconnect the submodule immediately [26].

3.3.2 Faults in submodule capacitors

The submodule capacitor plays an essential role in the operation of the MMC; however, it may suffer from a lot of problems that can severely affect their operation, such as sensitivity to temperature and frequency. One of the most critical problems is the wear-out degradation failure. The main consequence of this failure is the increased equivalent series resistance (ESR). This ESR increase affects the rate of charge and discharge and then the whole operation of the capacitor [75]–[77]. In addition to the wear-out failure, the submodule capacitor may be exposed to open circuit and short circuit failures, as shown in Table 3.4.

Table 3.4: Faults in submodule capacitors.

Fault Type	Failure Mechanism	Consequences
Open circuit	Leakage of electrolyte dielectric material	1) Increase in the capacitor voltage, current, and temperature. 2) Mechanical vibration
	Loose connections of terminals	
Short circuit	Dielectric breakdown	Increase in the capacitor voltage, current, and temperature
Fault in capacitor structure	Change in the electrolytic capacitor structure and capacitance value	Increase in the capacitor voltage, current, and temperature

The capacitor short circuit fault is the only fault type that needs the converter to be shut off, while, in all other fault types, it is not required to shut off the converter [75]. The detection of capacitor faults is not considered in this thesis, as it is a different topic that depends on the monitoring of the capacitor life time.

3.4 The Concept of Fault Detection

The electric fault is defined by any failure associated with a device or with components inside the electric system [78], [79]. The fault detection scheme is responsible for continuous monitoring of the system for the purpose of detecting different types of faults, locating the fault, and diagnosing the cause of the fault. As per Figure 3.6, fault detection strategies can be divided into two main types.

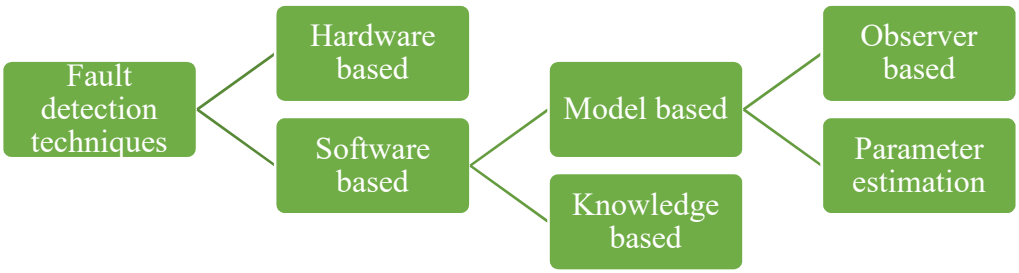


Figure 3.6: Types of fault detection techniques.

The first is the hardware-based fault detection and the second is the software-based fault detection.

3.4.1 Hardware-based fault detection

Hardware-based fault detection strategies depend on adding extra sensors or special power circuits that are dedicated to monitoring the whole system. They can easily detect the fault by comparing the measured signals with pre-defined thresholds. When the measured signals exceed these thresholds, the fault detection unit (FDU) considers this a fault incident; thus, this fault can be easily located [23], [26]. Hardware-based FDUs are commonly used in many applications, and they are famous for their accuracy. However, they have some disadvantages that can be summarised in the following points:

- Adding extra system components for the system will increase the cost.
- The system will be more complicated, and more space will be consumed.
- The increased number of components will reduce the reliability of the entire system.

3.4.2 Software-based fault detection

The software-based FDUs depend on figuring out the different states of the system through the estimate of these states, comparing it with their corresponding actual states [80], [81]. The system states can be identified from the mathematical model of the system. In this case, the FDU will be a model-based unit or can be obtained from the analysis of historical fault data, in which case, the FDU will be knowledge based [80].

Regarding the model-based fault detection strategies, the first step in the design of such techniques is building the mathematical model of the system that needs to be protected. Then, there are two main directions. The first is to utilise an observer and compare actual measured signals with their corresponding observed signals. A fault is detected when a large error between the actual signals and their observation is created. The second route is estimating some signals and comparing them with the actual signals. If there is an inconsistency between the estimation and the actual signals, this is considered to be a fault event [81]. These methods are very attractive for researchers since they are accurate and do not need any extra sensors or additional circuits. However, there is a real challenge in these methods, which is the guarantee of the accuracy of the estimation or observation methods to achieve the selectivity of the FDU and at the same time prevent false fault detection.

Regarding the knowledge-based methods, these methods are attractive in very limited cases where there is a real difficulty in emphasising the mathematical model of the system. Thus, the FDU is designed based on historical fault data, and then a suitable artificial intelligent technique is trained using this data to be able to detect similar faults in the future [26], [82], [83]. The main problems associated with the knowledge-based methods are:

- They require a large number of training points, which consume a lot of effort.
- Their accuracy is not guaranteed if some of the system inputs are changed.

3.5 Fault Detection Techniques in MMCs

There has not been much research conducted in the area of fault detection in MMCs. Most of the proposed methods in literature are classified as hardware techniques. The following subsections present the popular fault detection methods proposed in the past.

3.5.1 IGBT fault detection using the rate of change of the collector current

This method is a hardware-based technique that is dedicated to detecting faults inside IGBTs. It depends on measuring the rate of change of the collector current $\frac{di_c}{dt}$ using the circuit shown in Figure 3.7. This value is compared with a pre-defined threshold, and if it exceeds this threshold, the FDU sends a signal indicating a fault incident [84].

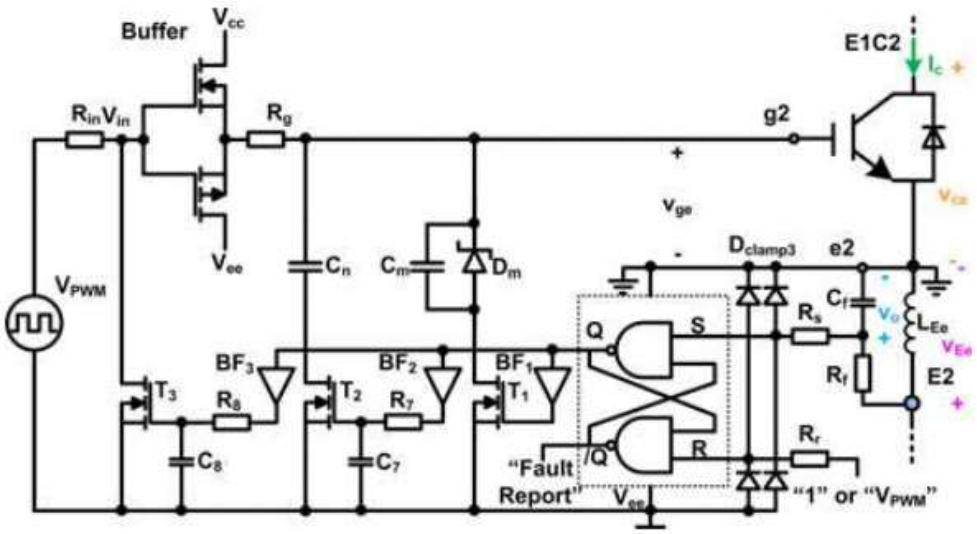


Figure 3.7: The $\frac{di_c}{dt}$ measuring circuit [84].

This method is very accurate, as each IGBT has its own monitoring circuit. However, the cost of this method is extremely high since each IGBT has a sophisticated monitoring circuit [84]. Moreover, it is not capable of differentiating between open circuit and short circuit faults.

3.5.2 IGBT fault detection using the behaviour of the gate voltage

This method is also a hardware-based technique that depends on the charge rate of the gate voltage. As shown in Figure 3.8, the energy of the gate voltage is determined based on the value of the gate voltage and on monitoring the turn-on period. The calculated value of the energy is compared with different thresholds to classify whether the IGBT is healthy or in a fault condition [85].

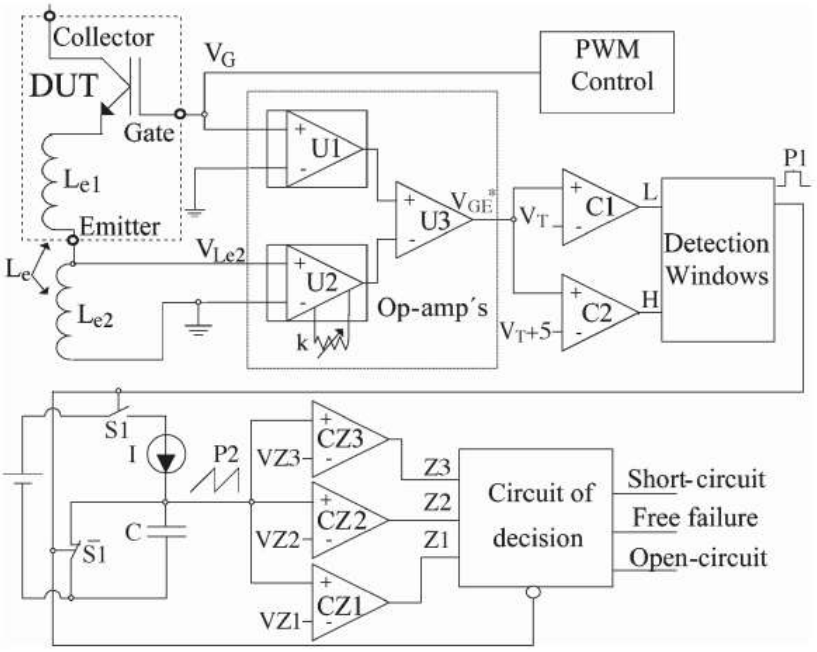


Figure 3.8: Gate voltage-based fault detection circuit [85].

The important advantage of this method over the previously mentioned method is its ability to differentiate between open circuit and short circuit faults, as each fault has its dedicated threshold. However, this method still increases the cost of the FDU because of the need to have a dedicated measured signal for each IGBT [85]. Moreover, the fault detection circuit is very complex, and it is difficult to be integrated inside the IGBT.

3.5.3 Submodule fault detection using the measurements of submodule output voltage

All abovementioned fault detection techniques suffer from a common disadvantage, which is the complexity of the hardware circuit. This method, which is classified as a hardware method, was designed to eliminate this drawback through the implementation of a simple hardware circuit. The fault detection technique depends on a new measurement location. Instead of measuring the capacitor voltage, this fault detection strategy depends on the measurement of submodule output voltage [86]. Additionally, to avoid adding extra measurements, the submodule capacitor voltage is derived from the submodule output voltage, as demonstrated in Figure 3.9.

The capacitor voltage can be estimated by checking whether the state of the submodule is inserted or bypassed. If the submodule is inserted, then the capacitor voltage is equal to the submodule output voltage. However, if the cell is bypassed, the capacitor voltage will remain as it is.

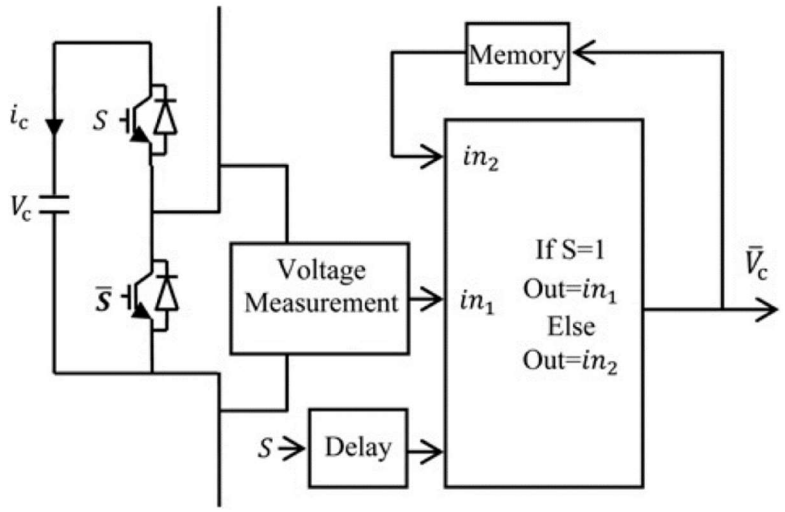


Figure 3.9: Block diagram of the submodule output voltage and derivation of capacitor voltage [86].

As shown in Figure 3.10, the fault detection strategy depends on the continuous comparison between the submodule output voltage, V_{om} and V_{min}, which is a value lower than all other capacitor voltages. The output of this comparison and the submodule switching signal are passed through an exclusive disjunction or 'exclusive or' (XOR). In normal operation, the submodule output voltage, V_{om}, should have 0 V, providing that the submodule is bypassed, and in this case, the output of the XOR should be low.

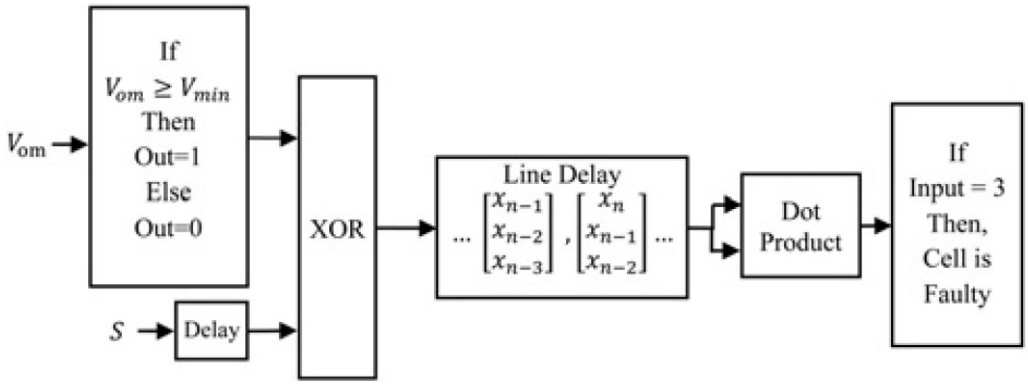


Figure 3.10: Flowchart of submodule output voltage-based fault detection [86].

While in the case of a fault, the output of the XOR will be high, as the voltage across the lower IGBT will no longer remain zero. Thus, the fault condition can be easily detected. This method has many advantages; it can detect both open circuit and short circuit faults and is very sensitive and fast. Nonetheless, it suffers from many drawbacks, which can be summarised in the following points [86]:

- This method needs the continuous measurement of submodule output voltage instead of capacitor voltage, which is not standard and requires extra measurement circuits.
- The capacitor voltages, which are mandatory for the control of the MMC, are derived from the submodule output voltage; this is not accurate and can form a threat for the MMC operation.
- The high sensitivity of this method can lead to malfunction since the decision is based on one factor, which is the submodule output voltage.

3.5.4 IGBT fault detection using artificial neural networks

This method is a knowledge-based software technique, which depends on the historical data of the MMC output voltage and current because they can be affected if any IGBT has either an open circuit or short circuit. If one of the IGBTs has an open circuit fault, the output voltage of the MMC is then distorted and decreased by a considerable value. On the other hand, if any IGBT has a short circuit fault, then the output current is increased by about 1.5 its normal value. As shown in Figure 3.11, an artificial neural network (ANN) is trained with the aid of an output voltage and output current histogram through which its elements have been captured in many normal and abnormal operating conditions [26], [82].

This technique also can provide the control system with the fault location as well. Although this method is a software-based method and does not need any extra physical components, it suffers from some critical disadvantages as mentioned before, such as the accuracy is not guaranteed if the voltage and current levels are changed due to a change in the application. Moreover, the training of the ANN consumes a lot of effort and does not cover all cases [82].

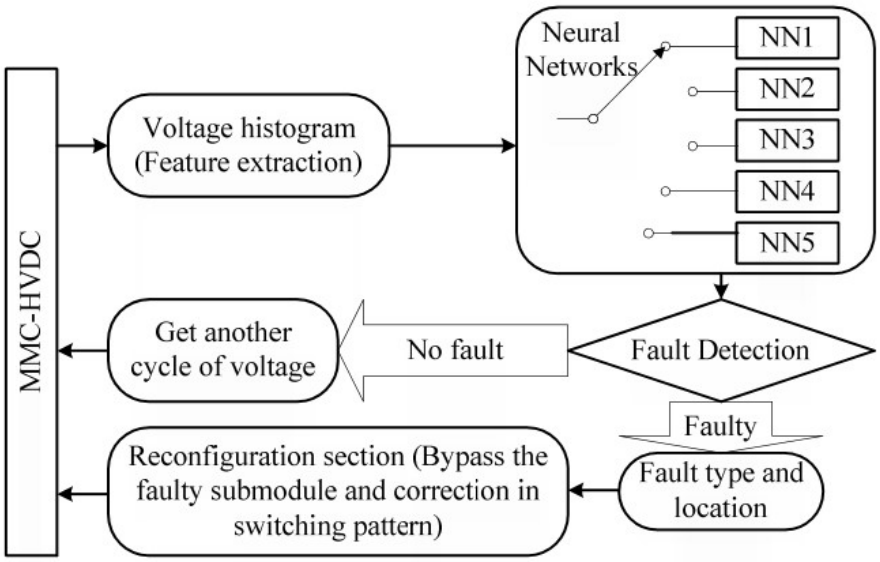


Figure 3.11: The block diagram of the ANN IGBT fault detection method [26].

3.5.5 Submodule fault detection using sliding mode observation

This method is classified as model-based software technique; it fully depends on observing the arm currents and capacitor voltages of the MMC. As shown in Figure 3.12, it has two operation modes. The first mode is the monitoring mode; in this mode the arm currents are observed using the sliding mode observer (SMO).

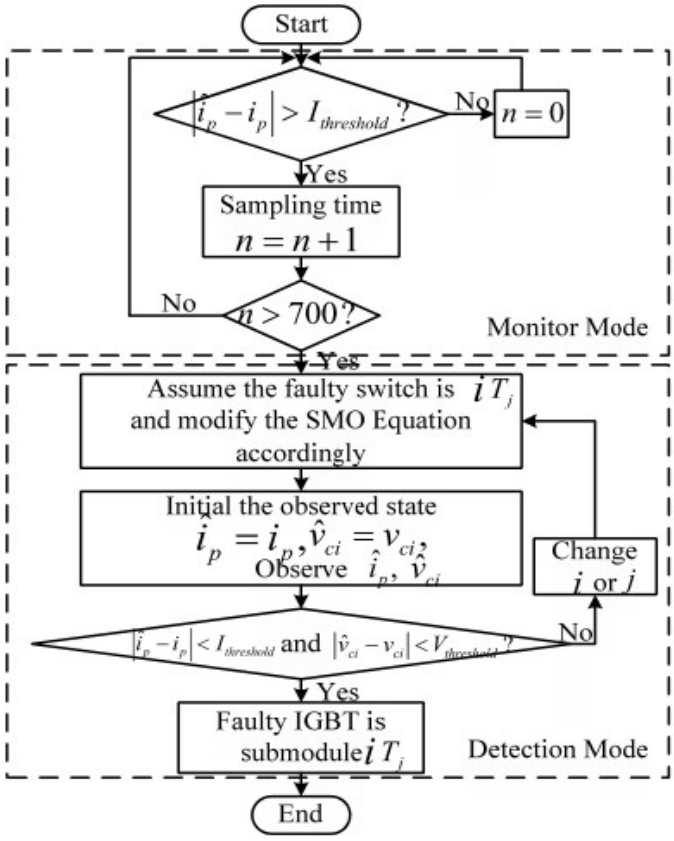


Figure 3.12: Flowchart of the SMO submodule fault detection technique [78].

If there is an error between any arm current and its observed state, then this arm is considered to have a fault, and the algorithm starts the second mode, which is the detection mode. In the detection mode, all of the arm submodules are exchanged with redundant submodules one by one. Then, the voltage of each submodule and the arm current are observed. If the observed capacitor voltage and arm current start to follow their actual value after replacing the submodule with a redundant one, then this submodule is considered to be faulty [78].

This method is considered to be very accurate and has a very robust performance compared to other techniques. However, it has some disadvantages that are summarised in the following points [78]:

- This method requires the measurement of each capacitor voltage, which requires a large number of voltage transducers and a sophisticated communication network to transmit their signals, which not only increases the cost but also complicates the whole control system.
- It requires the incorporation of redundant submodules, which will be used if and only if there is a fault; this also adds extra cost to the system.
- The process time of the algorithm is not small since it scans the observed signals of all arm currents and capacitor voltages. Moreover, exchanging the fault arm submodules with redundant submodules one by one consumes a lot of time because some MMCs can have about 400 submodules per arm. This makes it impossible to detect short circuit faults since the required detection time should be less than a few milliseconds.

Table 3.5 shows a comparison of all fault detection techniques presented in this chapter. It is clear that hardware techniques have higher accuracy than software-based techniques; however, their costs are much higher.

Table 3.5: Comparison between common MMC fault detection techniques proposed in literature.

Fault Detection Method	Classification	Cost	Complexity	Accuracy
Rate of change of the collector current	Hardware	High	High	High
Behaviour of the gate voltage	Hardware	High	High	High
Measurements of submodule output voltage	Software	Moderate	Moderate	Moderate
Artificial neural networks	Software	Low	High	Low
Sliding mode observation	Software	Moderate	High	High

This has motivated the author to implement a new method for fault detection that does not need hardware circuits and simultaneously improves accuracy when compared with other software strategies.

3.6 The Concept of Fault Tolerant Control

The FTC system is the system that is able to perform its desired control functions at a high level of stability and security during the occurrence of a certain fault. The FTC systems are gaining the interest of many researchers in different research fields because of their ability to enhance the overall reliability of systems. The FTC systems are classified into two main types: passive and active [87]–[89].

3.6.1 Active fault tolerant control

As shown in Figure 3.13, active FTC systems receive continuous fault status from the FDU. Then, at the fault condition, it reconfigures the control system to a new system, which isolates the faulty part of the system and maintains the stability of the plant. It is important to mention that the redesign process of the system is performed online, which normally may allow some changes to the desired control functions or degradation in the performance [90], [91].

The main disadvantage of active FTC techniques is their slow response due to the time consumed on the fault detection and controller redesign. However, the

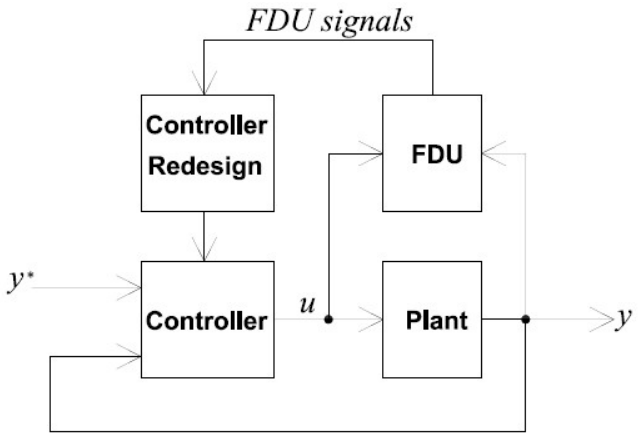


Figure 3.13: Structure of active FTC.

main advantage of these techniques is their ability to detect a wide range of faults [91].

3.6.2 Passive fault tolerant control

In passive FTC, the controller is designed in the offline mode and then it operates with fixed behaviour during normal and abnormal conditions. Therefore, it should be designed such that it can tolerate the faults [92], [93]. The main advantages of passive FTC techniques can be summarised in the following points:

- There is no need for the fault detection process, as the system is working with the same parameters during normal as well as fault conditions.
- Their response is very fast due to the elimination of FDU and the control redesign processes.

However, it is very difficult for one passive FTC system to detect different types of faults since they are designed in the offline mode [94].

3.7 Fault Tolerant Control of MMCs

As mentioned in the previous subsections, the MMC is very weak to certain types of faults. At the same time, MMCs should work at a high level of reliability, as they usually work in critical applications that do not have the luxury of losing the power transfer. Based on this, it is highly recommended to provide the control of the MMC with fault tolerance capability to enable the MMC able to deliver the desired

power during faulty conditions without the need to block the converter [26], [95]. The following subsections investigate popular methods used for tolerating the fault in MMCs.

3.7.1 Fault tolerant control using redundant submodules

Regarding tolerating the fault using redundant submodules, the idea depends on disconnecting the faulty submodule and inserting a new redundant submodule without the disconnection of the MMC, as shown in Figure 3.14 [26], [95], [96].

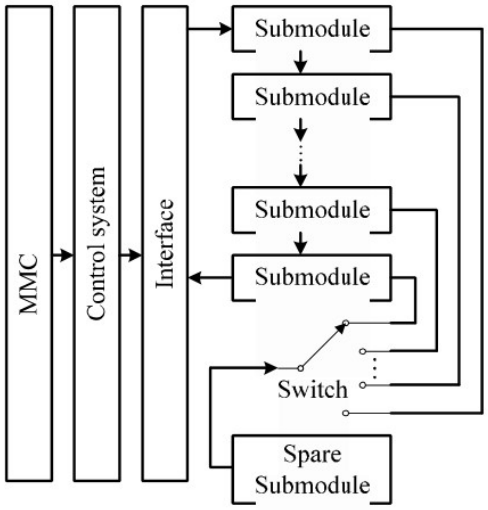


Figure 3.14: Structure of MMC with redundant submodules [26].

The process of insertion of the redundant submodules is done using a strict control. At each trigger time, the control system identifies the state of each submodule with the aid of a suitable fault detection algorithm. If any submodule is subjected to high switching commutations or a fault, the control system bypasses the faulty submodule and replaces it with a redundant submodule, as shown in Figure 3.15 [96].

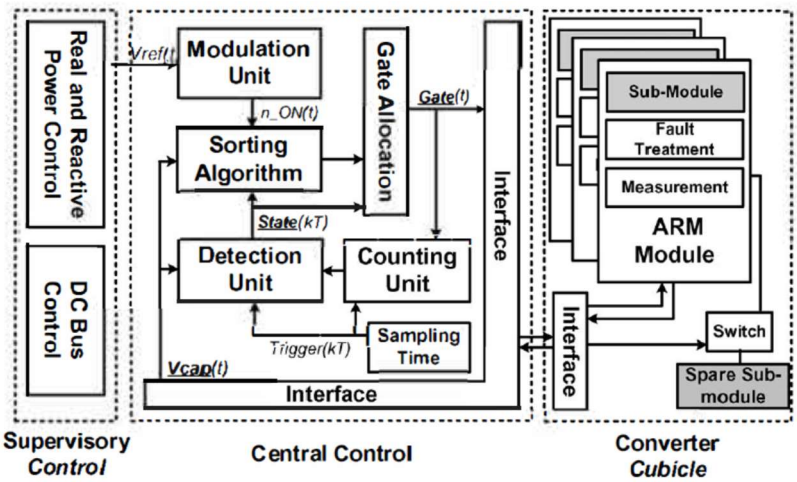
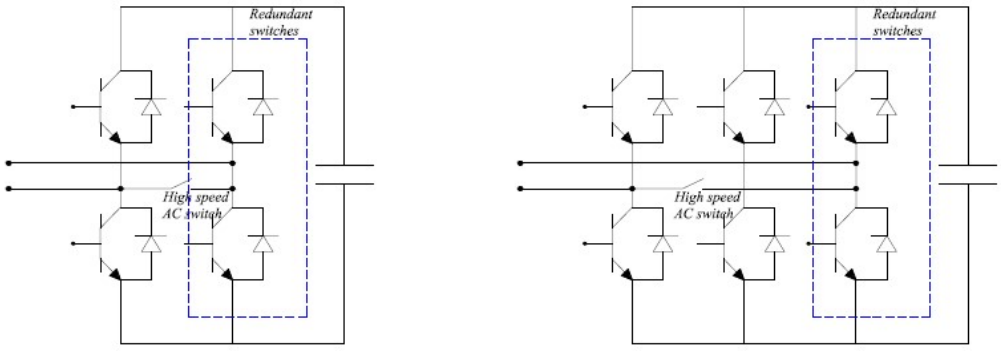


Figure 3.15: Block diagram of fault tolerant control with redundant submodules [96].

The concept of redundancy will improve the fault tolerance, providing maximum safety to MMCs. However, from an economic point of view, the redundancy increases the cost of the MMC, as it adds extra components that are not used during normal operation [96]. Adding to this, the circuit structure and the control system will be more complex.

3.7.2 Fault tolerant control using redundant IGBTs

In this method, the fault tolerance concept is achieved by adding two redundant IGBTs to each submodule and a high-speed AC switch, as shown in Figure 3.16. This means that, for half-bridge submodules, the number of switching devices will be increase from 2 to 4, while the number of switching devices will be increased from 4 to 6 in full-bridge submodules [95]. Figure 3.17 illustrates the way faults are tolerated using the manipulation of firing signals between faulty and redundant submodules.



(a) (b)

Figure 3.16: The circuit diagram of MMC submodule with IGBT redundancy for: a) half bridge, b) full bridge.

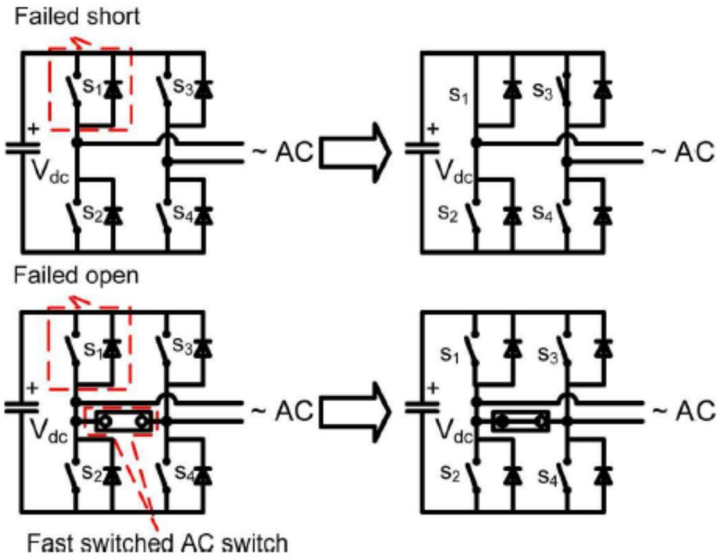


Figure 3.17: Tolerating the faults using redundant IGBTs [95].

If the IGBT S1 suffers from an open circuit fault, the firing of S1 and S2 is transferred to S3 and S4, and this guarantees the continuity of the power flow. However, if the IGBT S1 is suffering from a short circuit fault, a different switching sequence should be followed since the anti-parallel diode of S1 will provide a permanent current path. In this case, the high-speed switch that connects the S2 with S4 is closed to prevent the leakage of current to the DC source through S1. Then, the switching is applied to S3 and S4.

It is obvious that the research conducted concerning FTC of MMCs is not enough, especially as most of the methods proposed in the literature depend on using redundant submodules. This has motivated the author to propose a new FTC technique that depends on sorting algorithms instead of using redundant components, as presented in Chapter 6.

3.8 Chapter Summary

This chapter presented several capacitor voltage balancing techniques that were proposed in literature, showing the main differences between them and the proposed capacitor voltage balancing technique presented in Chapter 4. In addition, different MMC faults have been mapped, showing the consequences of each fault type. Finally, popular fault detection and tolerant control techniques have been also

investigated to show what has motivated the researched to implement the proposed fault detection and tolerant control techniques presented in Chapters 5 and 6.

Chapter 4

Proposed Capacitor Voltage Balancing Technique Based on Capacitor Voltage Estimation Algorithms

4.1 Introduction

As mentioned in Chapter 3, the process of capacitor voltage balancing is mandatory for a stable operation of the MMC. If these voltages are left without control, the difference between them will lead to increasing the converter differential current, which means that the converter losses will be higher. In addition, the differential current affects the quality of the output current because of the superimposed harmonics. This chapter presents a new capacitor voltage balancing technique with a reduced number of sensors. The developed technique is based on capacitor voltage estimation. For this purpose, two adaptive capacitor voltage estimation techniques are developed. The first is based on the ADALINE algorithm, while the other is based on the RLS algorithm. The performance of the two techniques is compared to determine which gives better results in terms of speed of convergence and accuracy. Then, the description of control loops that are incorporated into the proposed balancing strategy are explained. Moreover, the design considerations of these control loops, including the selection of PID gains for each loop is conducted. Finally, simulation results for different case studies are

presented to show the performance of the proposed capacitor voltage balancing technique and compare it with the classical balancing strategy.

4.2 Proposed Technique of Capacitor Voltage Balancing

It can be concluded from subsection 3.2 that most of the capacitor voltage techniques proposed in the literature require the continuous measurement of capacitor voltages. This simply means that if an industrial MMC has 401 levels, the manufacturer must equip its submodules with 800 voltage sensors for each phase, keeping in mind that the acquisition of these sensors will need corresponding communication channels. This motivated the researcher to develop a new technique for balancing voltages of submodule capacitors without the need for measuring actual capacitor voltages, while getting a better performance by increasing the power quality of the MMC output power. The proposed algorithm depends on estimating submodule capacitor voltages instead of direct measurements. It consists of three main stages:

- capacitor voltage estimation,
- averaging control, and
- balancing control for capacitor voltages.

4.2.1 The capacitor voltage estimation technique

The capacitor voltage estimation is considered an extremely important step of the proposed control strategy. Although the capacitor voltage estimation eliminates the use of direct measurements, it is a must to maintain the estimation accuracy to avoid wrong control actions. Different algorithms have been developed in the past for the purpose of tracking dynamically changing signals. Sliding mode observer is one of the oldest methods that had been used to achieve this goal which is considered to be a basic technique supported by the fundamental control theory. In this technique, the procedure of the sliding mode observation starts with designing the intersection of the sliding mode surfaces. Then, the observer gain is determined to drive the estimation error trajectories and maintaining them on the sliding surfaces. The sliding mode observers have a lot of advantages such as: being well established and known technique, their mathematics are built according to the

mathematical model of the system and they are very robust as they do not get affected from system uncertainties and external noises. However, they suffer from critical disadvantages such as: the huge number of calculations (especially for systems with high number of states) and the estimated signals contains a variable steady-state errors[78], [97], [98].

Kalman filter is another technique which is very common in tracking the dynamically changing signals which particularly have multi-input and multi-output systems. Since it is a recursive method, it uses the state space model to get the best estimation of the tracked signal. The error of the estimation is minimized based on different criterions so the convergence stage is reached. Although the Kalman filter have high level of accuracy and the ability estimate invariant dynamic modes, it suffers from many drawbacks [98], [99] such as:

- It is severely affected by external noise and uncertainty of the parameters.
- It is very complex and requires huge number of calculations.
- It is very difficult to achieve real time operation when the system has higher orders such as 4 or 5.

For this particular purpose, the author proposed two capacitor voltage estimation techniques which have better performance when compared to other methods presented in literature. The first is achieved using the ADALINE algorithm, while the second algorithm uses the RLS algorithm.

4.2.1.1 Capacitor voltage estimation using ADALINE technique

The ADALINE technique is known for being a very efficient and quick online tracking technique for tracking dynamically changing voltage signals. It is utilised in many applications because of its robust performance, low calculation burden, and accurate results [100], [101]. The ADALINE algorithm is formed by simple calculations that do not consume large computing time, which is very important in the application of capacitor voltage estimation. To estimate capacitors voltages, the MMC governing equations given by (2.13) and (2.14) are rearranged and rewritten in the vector form as follows:

$$\frac{v_{dc}}{2} - v_o - v_{Lu} = [S_{u1} \quad S_{u2} \quad \dots \quad S_{uN}] \begin{bmatrix} v_{cu\_est} \\ v_{cu2\_est} \\ \vdots \\ v_{cuN\_est} \end{bmatrix}, \tag{4.1}$$

$$\frac{v_{dc}}{2} + v_o - v_{Ll} = [S_{l1} \quad S_{l2} \quad \dots \quad S_{lN}] \begin{bmatrix} v_{cl1\_est} \\ v_{cl2\_est} \\ \vdots \\ v_{clN\_est} \end{bmatrix}, \tag{4.2}$$

where S_{xi} is the switching state for the i^{th} submodule, $v_{Lu} = L_{arm} \frac{di_u}{dt}$, and $v_{Ll} = L_{arm} \frac{di_l}{dt}$.

The ADALINE algorithm produces a linear combination of its input vector $X(k)$, which represents the switching-state vector $[S_{x1} \quad S_{x2} \quad \dots S_{xN}]^T$ at time k, where the suffix T refers to the transpose operation. In this technique, the input vector is multiplied by the weight vector $W(k)$, which resembles the estimated capacitors voltages given in (4.1) and (4.2) to produce the predicted linear output $\hat{y} = X^T W(k)$. The next step is updating the weight vector using the Widro-Hoff delta rule given by [102]:

$$W(k+1) = W(k) + \alpha \frac{X(k)(y(k) - \hat{y}(k))}{X(k)^T X(k)}, \tag{4.3}$$

where α is the reduction factor and y is the actual output, which is given as:

$$y(k) = \frac{v_{dc}}{2} - v_o - v_{Lu}, \tag{4.4}$$

$$y(k) = \frac{v_{dc}}{2} + v_o - v_{Ll}. \tag{4.5}$$

When the difference between the measured signal $y(k)$ and the estimated signal $\hat{y}(k)$ converges to zero, the ADALINE algorithm decomposes the signal and estimates capacitor voltages. Figure 4.1 presents a detailed flowchart for the ADALINE algorithm. It is observed that increasing the reduction factor α increases the convergence speed due to losing the stability, as the prediction error may increase dramatically. This observation is a common behaviour of the Widrow-Hoff delta rule for all the study cases. A practical value for the reduction factor α is 0.002 for this application. This value is determined based on minimising the error to guarantee system stability [103]. It is worth mentioning that the proposed capacitor voltage estimation unit is based on three voltage sensors per phase to measure the voltage across the arm reactors and the output phase voltage.

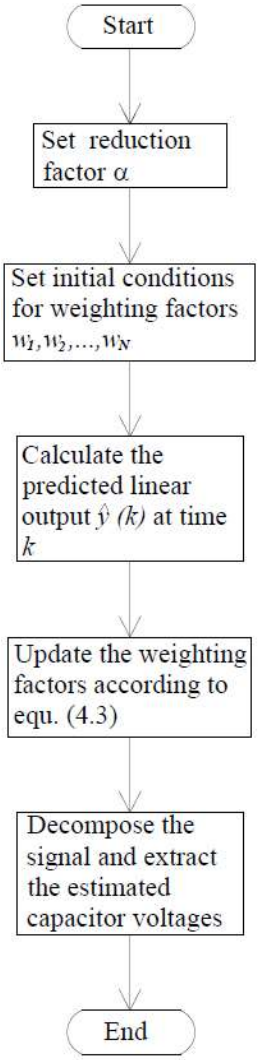


Figure 4.1: Flow chart of capacitor voltage estimation using ADALINE technique.

This action enables the implementation of a low-cost centralised controller for the MMC with a large number of submodules since the voltage measurement of submodules and their associated communication links are eliminated.

4.2.1.2 The capacitor voltage estimation using RLS technique

The RLS technique is a modified method of the least squares solution, which is reformulated into an iterative solution [104]. One of the main advantages of using the RLS as an estimation technique is the reduced dependency on historical measurements from previous iterations.

The fundamental RLS algorithm is formed by two basic equations. The first equation, given in (4.6), is to update the estimate vector $\hat{\theta}(k)$ of the submodule

capacitor voltages, while the second equation is used to update the weighting matrix $P(k)$ as shown in (4.7).

$$\hat{\theta}(k) = \hat{\theta}(k-1) + P(k)\hat{\theta}(k)\left[y(k) - \phi(k)^T\hat{\theta}(k-1)\right], \quad (4.6)$$

$$P(k) = \frac{1}{\lambda}\left[P(k-1) - \frac{P(k-1)\phi(k)\phi(k)^T P(k-1)}{\lambda+\phi(k)^T P(k-1)\phi(k)}\right], \quad (4.7)$$

where $\phi(k)$ is the connection vector that represents the switching-state vector $[S_{x1},\ S_{x2},\ \dots,\ S_{xN}]^T$ at time k, and λ is the forgetting factor that controls the speed of updating the weight matrix in (4.7). The result of multiplying $\phi(k)^T$ by $\hat{\theta}(k-1)$ gives the predicted output, $\hat{y}$ [105]. As shown in Figure 4.2, the predicted signal is subtracted from the measured signal, and the error is used to update the estimated vector. When the estimation error approaches zero, convergence is reached, and the estimated submodule capacitor voltages are calculated.

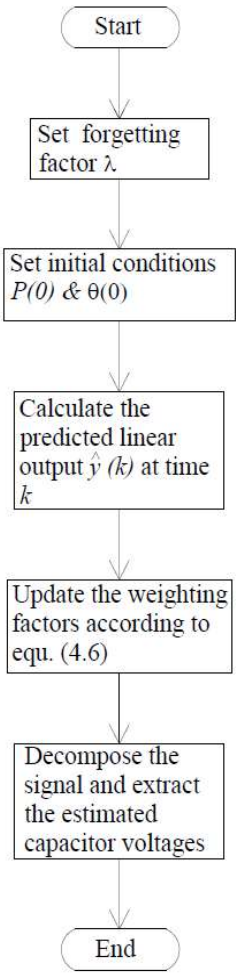


Figure 4.2: Flow chart of capacitor voltage estimation using RLS technique.

It is clear that the calculation burden of the RLS is slightly higher than the ADALINE; however, the RLS is characterised by its fast and accurate dynamic response. Figure 4.3 illustrates the general block diagram of the capacitor voltage estimation and the process of updating the capacitor voltages.

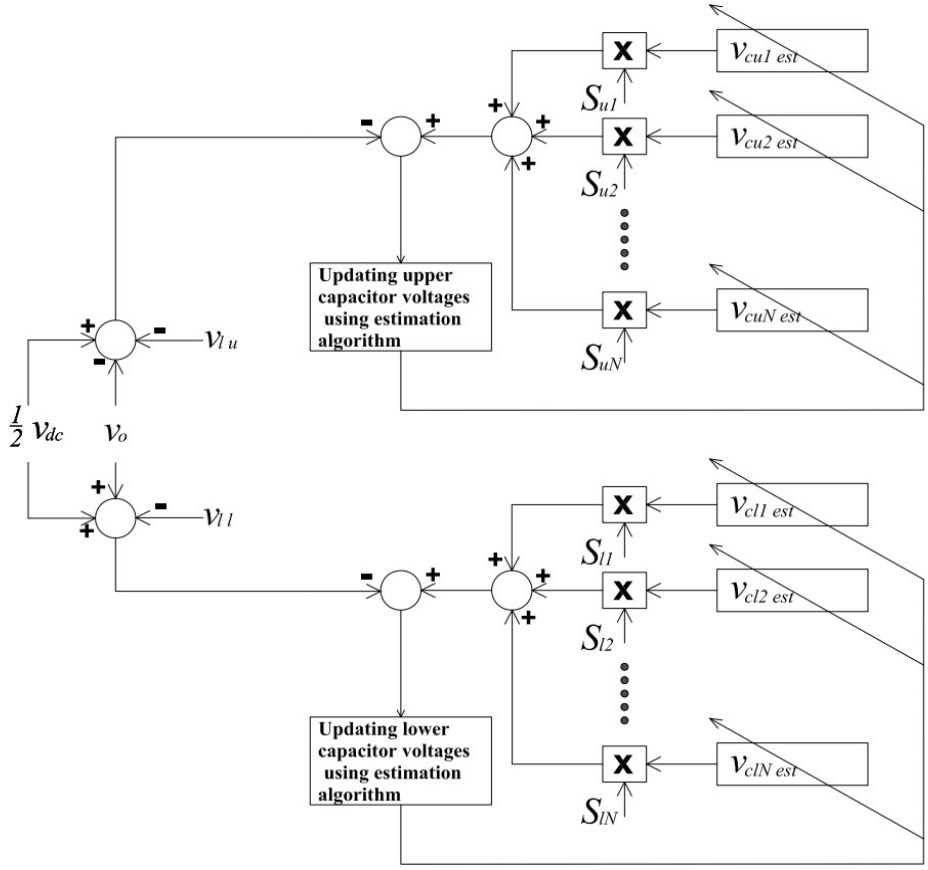


Figure 4.3: Block diagram of capacitor voltage estimation unit.

A test is run to compare between the dynamic performance of ADALINE and the RLS techniques for the estimation of capacitor voltages of the MMC. Figure 4.4 illustrates that the RLS algorithm offers a faster dynamic response and more accurate performance than that of the ADALINE algorithm for estimating the time-varying capacitor voltage signal. Therefore, the RLS algorithm is used to provide the estimated capacitor voltages for the proposed control strategy of the MMC.

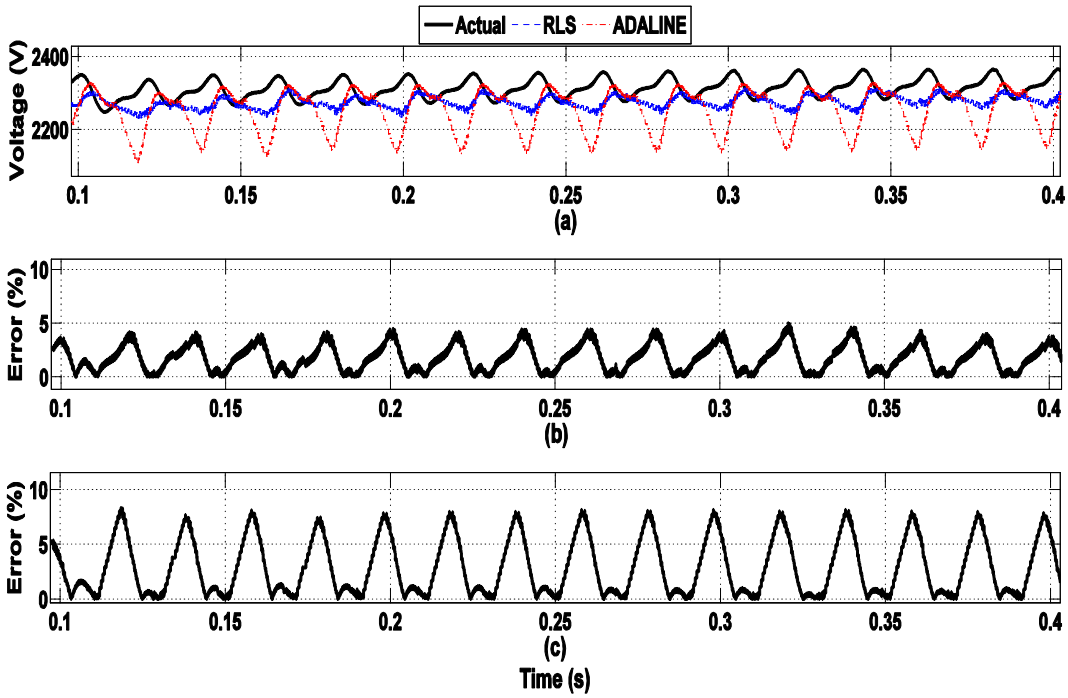


Figure 4.4: Comparison between the RLS and ADALINE performances: a) actual capacitor voltages versus RLS and ADALINE estimated signals, b) percentage error between actual voltage and RLS estimation, c) percentage error between actual voltage and ADALINE estimation.

4.2.2 The averaging control

The averaging control is responsible for controlling the average voltage across the complete leg. This controller is formed from two cascaded loops, as shown in Figure 4.5 [106].

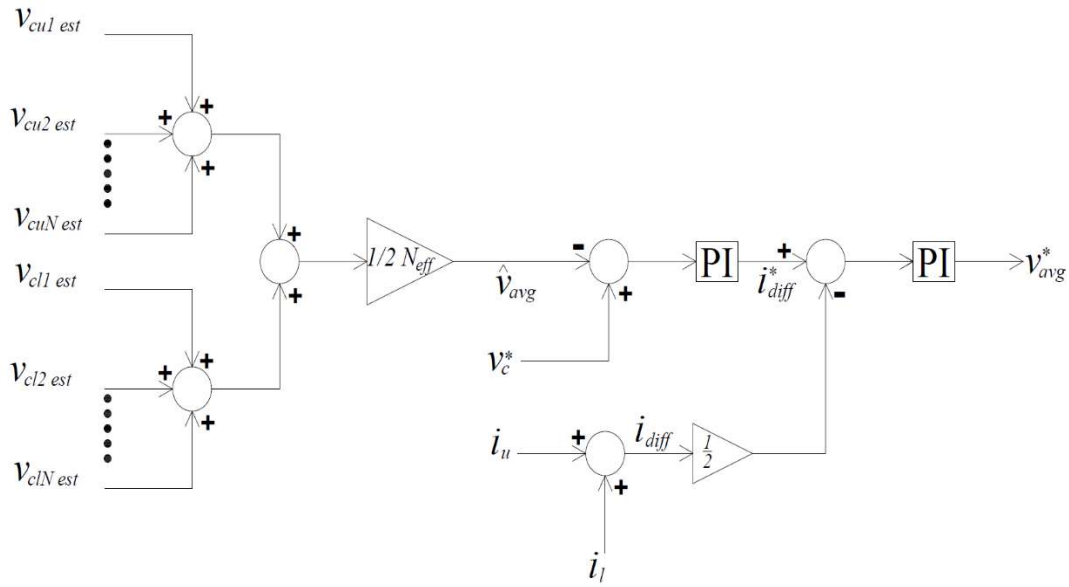


Figure 4.5: Block diagram of the averaging controller.

The first loop is the voltage control loop where the estimated average voltage, $\hat{v}_{avg} = (\sum v_{cu_{est}} + \sum v_{cl_{est}})/2N$, is subtracted from the reference capacitor voltage, v_C^*, and the resultant error is processed through a PI controller to generate the reference signal for the differential current, i_{diff}^*. Another PI controller is utilised in the inner loop to regulate the differential current, calculated from (2.10), at its reference signal. The action of the inner loop controller is the average voltage signal, v_{avg}^*.

To determine the value of the gains for the inner and outer loops PI controllers, the mathematical representation of each loop should be introduced using Laplace transforms. Regarding the inner loop which controllers the differential current, the loop gain is given by:

$$l(s) = \frac{K_i(s)}{ls + r_a} \tag{4.8}$$

This means that the loop has a pole at $s = \frac{-r_a}{l}$, this pole reduces the magnitude and the phase of the loop gain at low frequencies. To cancel the effect of this pole, the PI controller is added to place a zero. This modifies $K_i(s)$ to be:

$$K_i(s) = k_{p1} + \frac{k_{i1}}{s} \tag{4.9}$$

Where k_{p1} and k_{i1} are the proportional and integral gains respectively which should be as follows:

$$k_{p1} = \frac{l}{\tau} \tag{4.10}$$

$$k_{i1} = \frac{r_a}{\tau} \tag{4.11}$$

Where τ is the time constant, based on this the loop gain is changed to:

$$l(s) = \frac{1}{\tau(s)} \tag{4.12}$$

The transfer function of the inner loop is given by:

$$G_i(s) = \frac{i_{diff}}{i_{diff}^*} = \frac{1}{\tau(s)+1} \tag{4.13}$$

To enable the controller from functioning with fast response, the τ should be by far lower than the switching frequency which is 2 kHz. The τ is selected to be 4 ms which is 1% from the value of the switching frequency. By substituting in (4.12) and

(4.13), the values of k_{p1} and $k_{i1}$are 0.5 and 37.5 respectively. Figure. 4.6 demonstrates the bode plot for the inner loop transfer function with the selected PI gains showing a stable performance with fast response.

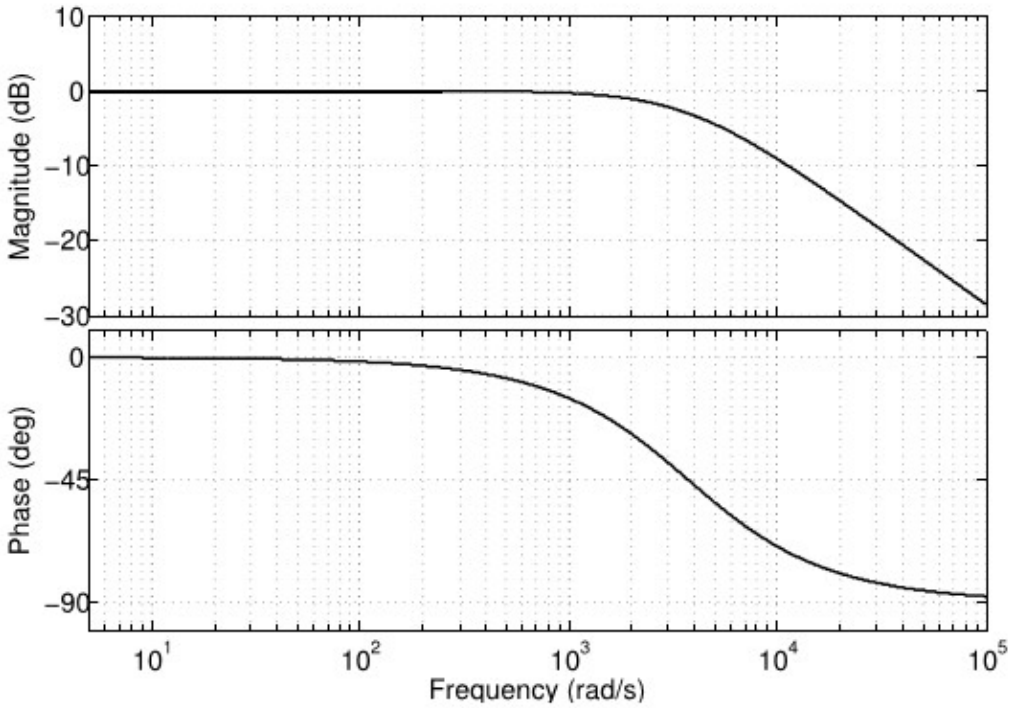


Figure 4.6: The bode plot of the inner loop of the averaging controller.

Moving to the outer loop which controls the average voltage across the whole leg, the steady state error is eliminated by adding the PI controller with the following gain:

$$K_v(s) = k_{p2} + \frac{k_{i2}}{s} \tag{4.14}$$

As shown in (4.14), the transfer function of the inner loop has a bandwidth which is by far higher than the bandwidth of the outer loop. Based on this fact, the gain of the inner loop is assumed to be 1 for the purpose of simplifying the calculations. As a result, the outer loop gain is given by:

$$l_2(s) = \frac{k_{p2}s + k_{i2}}{2\,Csm\,s^2} \tag{4.15}$$

From (4.16), the transfer function of the outer loop can be expressed as a second order differential equation as follows:

$$G_v(s) = \frac{v_{avg}}{v^*_{avg}} = \frac{k_{p2}s + k_{i2}}{2\,Csm\,s^2 + k_{p2}s + k_{i2}} \tag{4.16}$$

Using MATLAB software, this equation is solved for ξ equals 0.7 for a better dynamic response. The gains of the PI dedicated for the outer loop is calculated as follows:

$$k_{p2} = 4\, Csm\, \xi\, \omega_o \tag{4.17}$$

$$k_{i2} = 2Csm\, \xi\, {\omega_o}^2 \tag{4.18}$$

The natural frequency ω_o is kept very low compared to the frequency of the MMC AC voltage output. The k_{p2} and the k_{i2} are 1.5 and 150 respectively. Figure 4.7 shows the bode diagram of the outer loop.

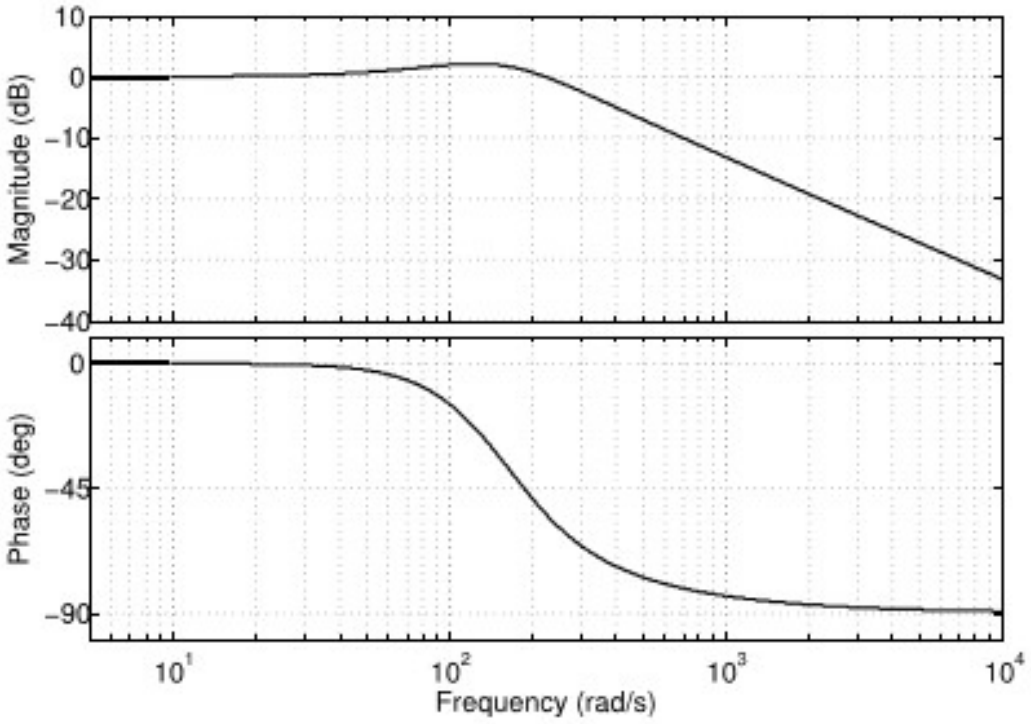


Figure 4.7: The bode plot of the outer loop of the averaging controller.

4.2.3 Balancing control

The balancing control, presented in Figure 4.8, is a centralised control system that generates reference signals to balance the voltage across the submodules capacitors based on the estimated voltages from the ADALINE processing unit. First, the controller subtracts the estimated capacitor voltage of each submodule from the reference capacitor voltage, v_c^*. The resulting errors are passed to simple proportional (P) controllers. The outputs from the P-controllers are multiplied by the sign of their corresponding arm current to form reference signals for balancing the

voltage across capacitors (v_{cul_bal}, …, v_{cuN_bal}, v_{cll_bal}, …, v_{clN_bal}). Finally, to form the modulating signal for a submodule, the balancing control signal for this submodule, the average voltage command, v^*_{avg}, and the reference phase voltage, v^*_o, are added. The PS-PWM technique is utilised to generate the switching signals for the submodules of the MMC [107]. As shown in this subsection, the proposed scheme eliminates the need for massive numbers of voltage sensors for the submodule capacitors and their associated communication systems with the central controllers. Consequently, the proposed strategy has succeeded in substantially decreasing the cost of implementation at a very good operating performance rendered in its application for an MMC system with a large number of submodules.

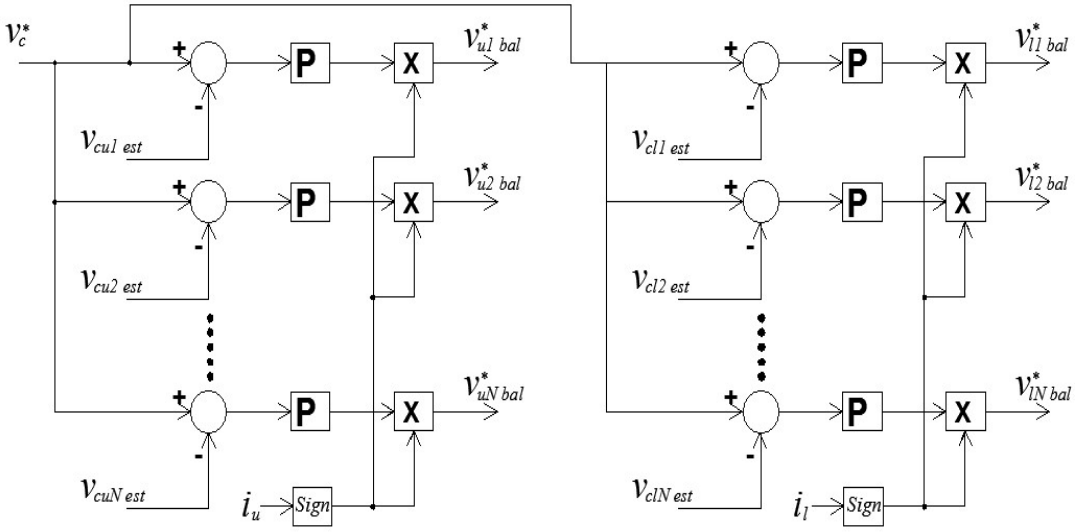


Figure 4.8: Block diagram of the balancing controller.

Following the same design concept introduced in the previous subsection, the gain of the balancing controller $k_{p\ b}$ is selected to be 0.35.

4.3 MMC Simulation Models

Two simulation models have been developed for the validation of all proposed techniques in the thesis. The first model demonstrates a DC voltage source connected to a three-phase load through a detailed five-level MMC. The second model demonstrates two wind farms connected to the grid through a HVDC link based on two MMCs with 77 voltage levels. The average model of the MMC is considered.

4.3.1 MMC Model 1

The first model considers a detailed simulation of a five-level MMC. Each submodule in the MMC is formed from two IGBTs and a capacitor. As shown in Figure 4.9, the MMC connects a DC voltage source to a three-phase load, which means that the MMC permanently acts as an inverter. The rated power of the MMC is selected to be 1 MW, while the rated DC voltage is 9,000 V.

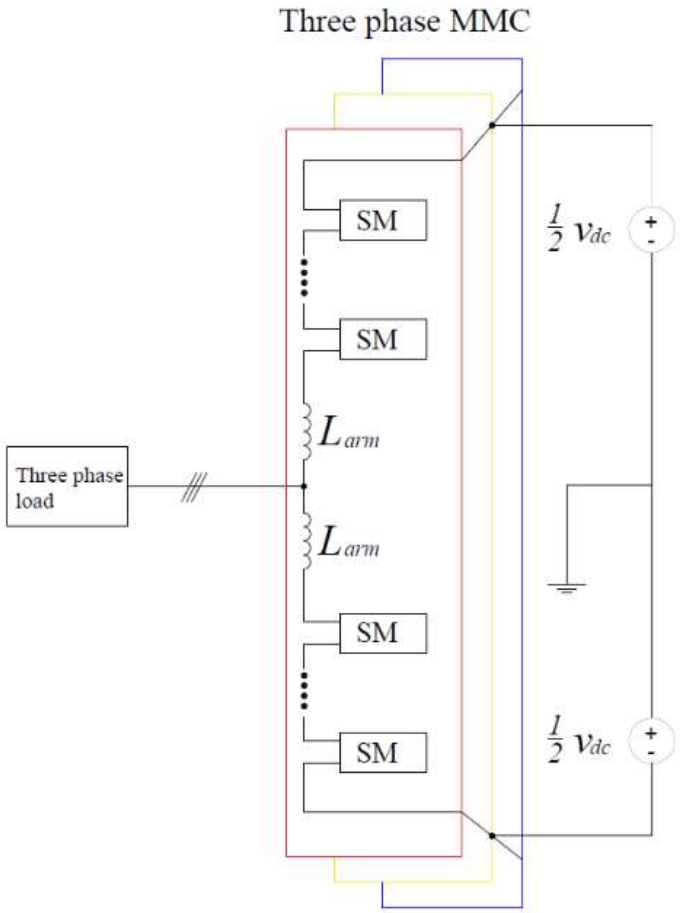


Figure 4.9: The circuit diagram of the first MMC model.

To calculate the size of the capacitor, first the arm energy variation must be plotted according to (2.30), assuming that the power factor is 0.8. Figure 4.10 illustrates the energy variation across the arm. The maximum energy stored in the arm is 3.855 kJ. If the maximum allowable ripples for the capacitor voltage $k_{ripple\ max}$ are 10% and for the arm current Δi_{diff} are 20%, the value of the submodule capacitor C_{SM} is chosen to be 1900 µF to fit the criteria presented in (2.32).

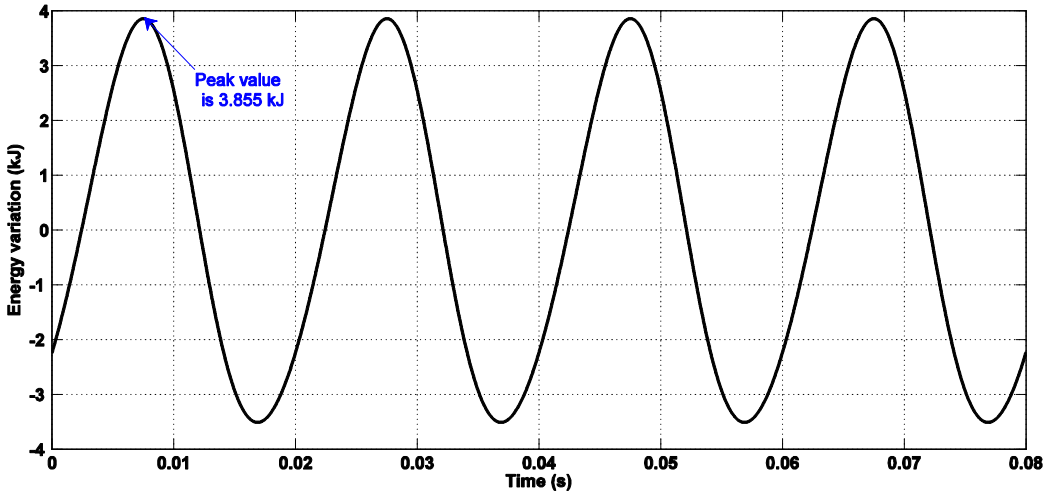


Figure 4.10: The arm energy variation of the MMC simulated in the first model.

Table 4.1: Summary of the MMC parameters of the first model.

MMC model parameters of the first model	
Rated power	1 MW
Submodule rated voltage	2,250 V
Rated DC voltage	9,000 V
Arm inductance	3.3 mH
Submodule capacitance	1900 µF
Number of submodules per leg	8
Carrier frequency, f_c	2 kHz
Load	30 Ω, 10 mH

The PS-PWM modulation technique is utilised for the switching of the MMC submodules. The frequency of carrier signals f_c is 2 kHz, which means that the switching cycle of the IGBT T_s is 0.5 ms. Thus, the arm inductor L_{arm} is selected to have a value of 3.3 mH to fit the rule presented in (2.34). Table 4.1 summarises the parameters of the simulated MMC.

4.3.2 MMC Model 2

Unlike the detailed model presented in the previous subsection, the average model of a 77-level MMC is considered to facilitate the calculations because of the relatively high number of submodules. The average model used in the simulation depends on converting the detailed model of the submodule to its Thevenin equivalent [57].

As shown in Figure 4.11, the model contains two wind farms, where each has a rating of 500 MW. The first wind farm delivers the energy through a permanent magnet synchronous generator (PMSG), and the output voltage of the PMSG is

0.69 kV. The terminals of the PMSG are connected to a back-to-back two-level VSC.

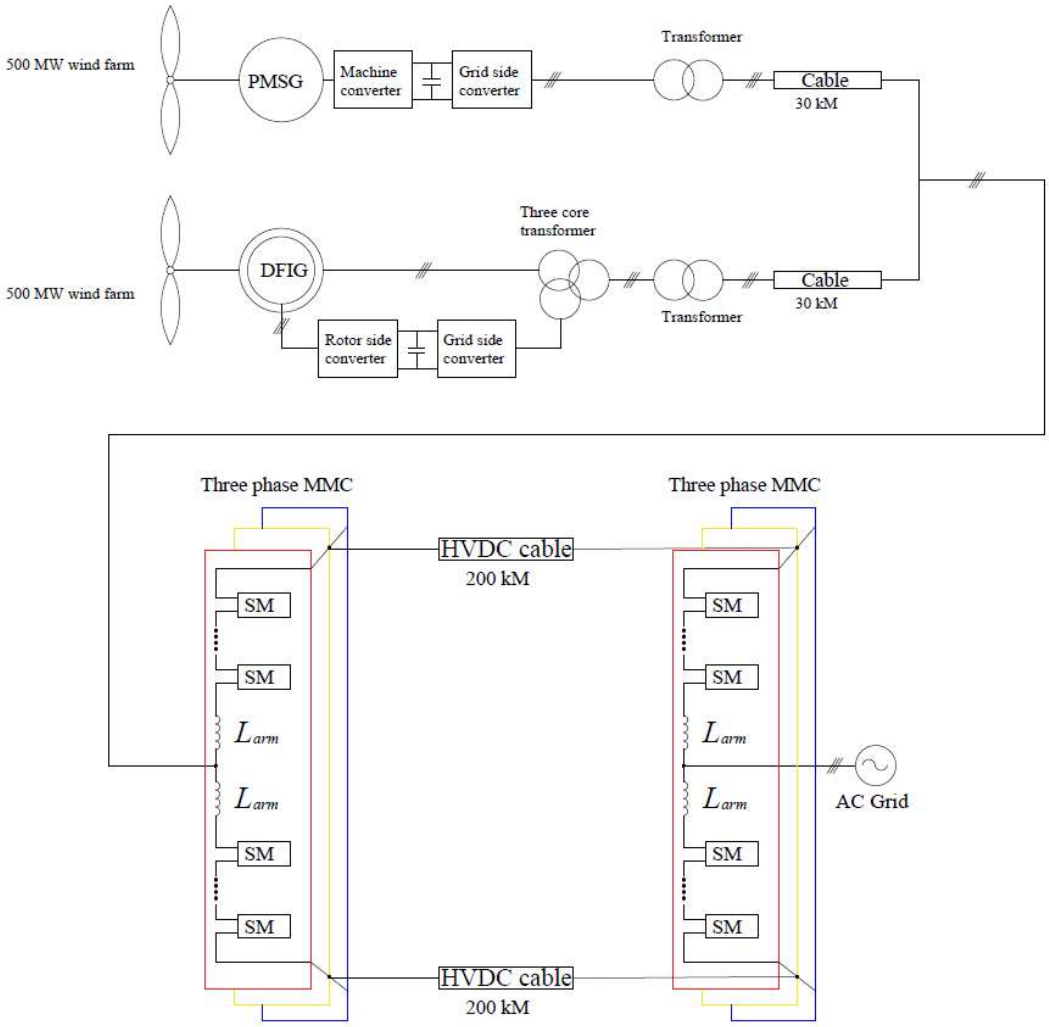


Figure 4.11: The circuit diagram of the second MMC model.

The generator used in the second wind farm is a double-fed induction generator (DFIG), which generates the power at 0.69 kV. The rotor winding of the DFIG is connected to a back-to-back two-level VSC. The output of this VSC and the stator winding of the DFIG are both connected to a three-core transformer. Since both windfarms are working on the same voltage level, a point of common coupling is formed, connecting the two wind farms together with the rectifier stage of the HVDC. The HVDC link is formed from two MMCs connected through a 200 kM cable. The output of the inverter stage of the HVDC system is connected to a 220 kV AC grid. Modelling details of wind turbines, PMSG, DFIG, and all control loops

for controlling the generated power from the wind farms and the injected power into the grid are illustrated in Appendix A.

The rated power of both MMCs is selected to be 1,000 MW, while the rated DC voltage is 640 kV. The size of the submodule capacitor is calculated in the same manner as presented in the previous subsection. First, the arm energy variation must be plotted according to (2.30), where 0.8 power factor is assumed. Figure 4.12 illustrates the energy variation across the arm. It can be seen from the plot that the maximum energy stored in the arm is 3.855 kJ. If the maximum allowable ripples for the capacitor voltage $k_{ripple\ max}$ are 10% and for the arm current Δi_{diff} is 20%, the value of the submodule capacitor C_{SM} is chosen to be 220 μF to fit the criteria presented in (2.32).

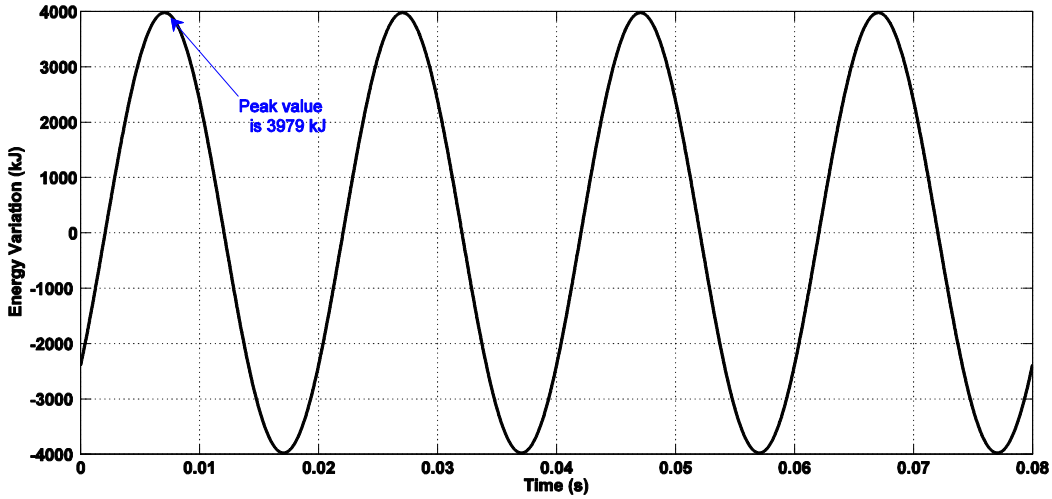


Figure 4.12: The arm energy variation of the MMC simulated in the second model.

Similar to Model 1, the PS-PWM modulation technique is used and the frequency of carrier signal f_c is 2 kHz. A 70 mH arm inductor is selected to fit the rule presented in (2.34). Table 4.2 summarises the parameters of the simulated MMC of Model 2. Details of simulation of both models are found in Appendix B.

Table 4.2: Summary of the MMC parameters of the second model.

MMC Model Parameters of the Second Model	
Rated power	1,000 MW
Submodule rated voltage	640/76=8.4 8 kV
Rated DC voltage	640 kV
Arm inductance	70 mH
Submodule capacitance	220 µF
Number of submodules per leg	152
Carrier frequency, f_c	2 kHz
Grid voltage	220 kV

4.4 Simulation Results

The proposed capacitor voltage balancing strategy is applied to the MMC, which is simulated using the PSCAD/EMTDC software package [108]. Three case studies were simulated to evaluate the performance of the MMC and the proposed capacitor voltage balancing technique under different operating conditions. Case 1 and Case 2 used the system parameters shown in Table 4.1, while Case 3 was applied to the MMC with parameters shown in Table 4.2. Primarily, the first task is dedicated to the performance evaluation of the proposed RLS algorithm in order to estimate capacitor voltages used for controlling the MMC under dynamic reference phase voltage changing conditions, while the second case is devoted to assessing the dynamic performance of the proposed control strategy during the boost operation of the MMC. Regarding the third case, it is conducted to evaluate the proposed capacitor voltage balancing technique when applied to a grid-connected MMC with a large number of voltage levels.

4.4.1 Case 1: Dynamic performance of the proposed capacitor voltage estimation-based control strategy

The purpose of this simulation case is to examine the performance of the proposed capacitor voltage estimation-based control algorithm for the MMC under the dynamic change of the reference phase voltage. The reference capacitor voltage v_c^* is set at vdc/N = 2.25 KV, while the reference phase voltage signal v_o^* is dynamically changed from 0.7 pu to 1 pu at t = 0.2 s. First, the estimation units for capacitor voltages are disabled, and the actual measurements are used in the control system. The three-phase voltages, currents, and capacitor voltages are shown in

Figure 4.13. Similar results to Figure 4.13 are obtained in Figure 4.14, where the proposed estimation unit for the capacitor voltages are enabled and utilised in the proposed control system of Figures 4.5 and 4.8. As displayed in Figure 4.14(a), the measured three-phase AC voltages follow their reference signals. As expected, only six submodules are utilised when $v_o^* = 0.7$ pu, while all the submodules are involved when $v_o^* = 1$ pu. The three-phase load currents are displayed in Figure 4.14(b). Figure 4.14(c) traces the capacitor voltages, which are grouped into two main trajectories: one for the upper arm and the other for the lower arm. These two trajectories are out of phase, and they are identical to that presented in Figure 4.13(c), where the measured capacitor voltages are used instead of their estimated signals in the control of the MMC. The proposed MMC controller succeeds in balancing the capacitor voltages at their reference value of 2.25 KV. Moreover, the estimated capacitor voltages and their corresponding actual measurements for the upper and lower arms are presented in Figures 4.15 and 4.16, respectively. Fast tracking with accurate performance of the proposed RLS algorithm for estimating the submodules capacitor voltages are evident. Furthermore, the circulating current tightly tracks its reference signal, as demonstrated in Figure 4.17(a). Figures 4.17(b) and 4.17(c) illustrate the actions of the averaging controller of Figure 4.5 and the balancing controller of Figure 4.8 for the first submodule at the upper arm $v_{cu1\,bal}^*$, respectively. These results reveal the efficient utilisation of the proposed capacitor voltage estimation technique for the control algorithm of the MMC.

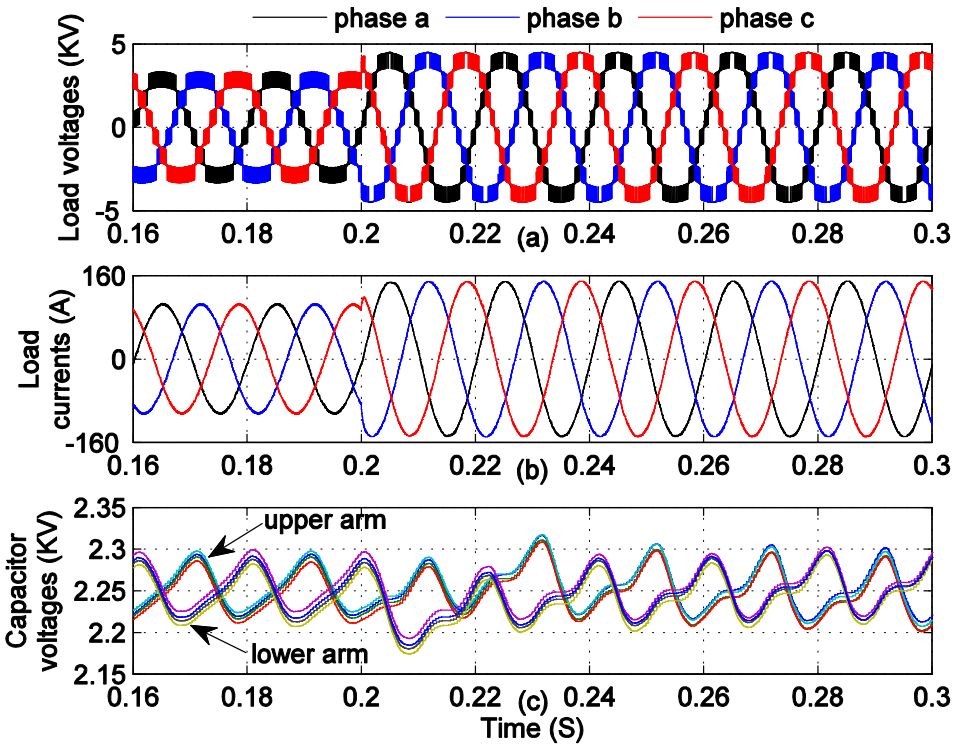


Figure 4.13: Load waveforms of Case 1, while disabling the proposed estimation unit: a) three-phase voltages, b) three-phase load currents, c) voltages of Leg a submodules.

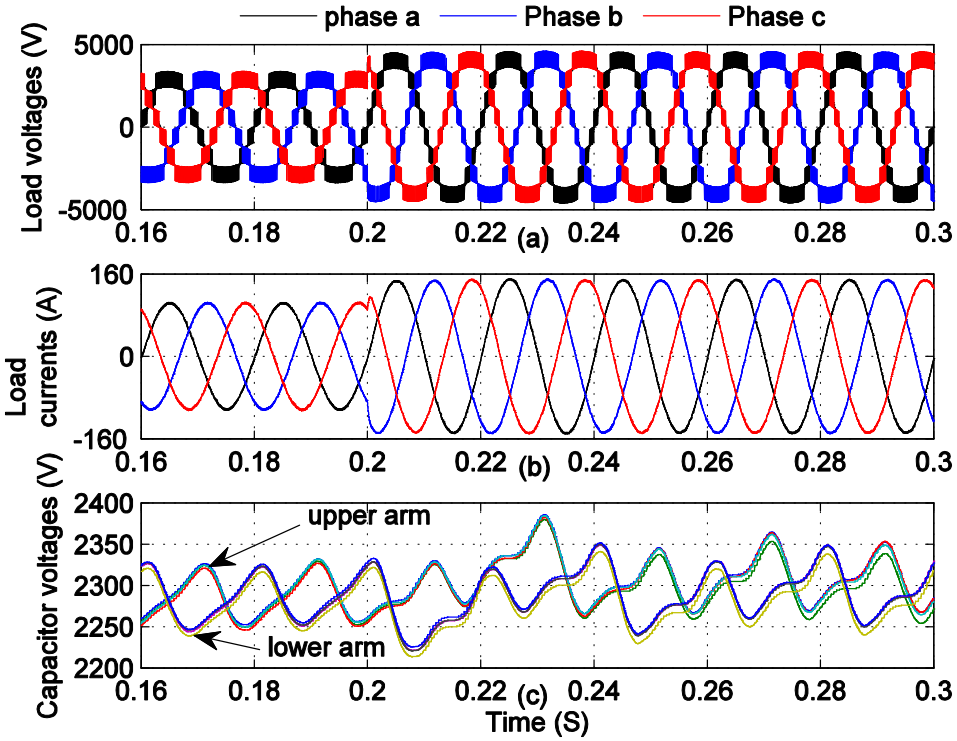


Figure 4.14: Load waveforms of Case 1, while enabling the proposed estimation unit: a) three-phase voltages, b) three-phase load currents, c) voltages of Leg a submodules.

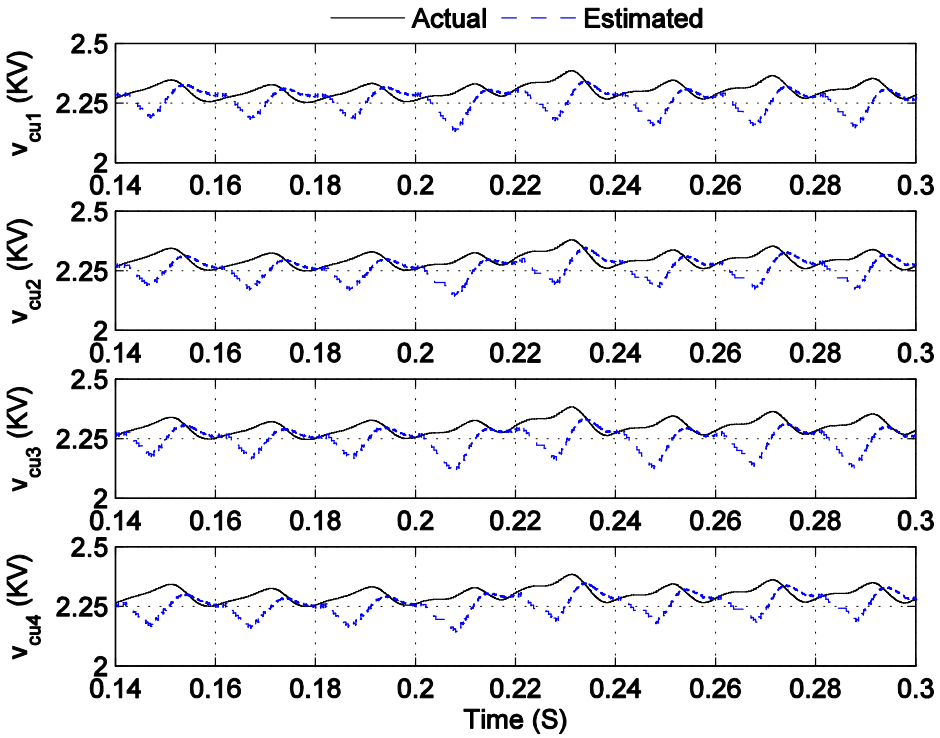


Figure 4.15: Case 1 actual and estimated voltages of the upper arm submodules of Phase a.

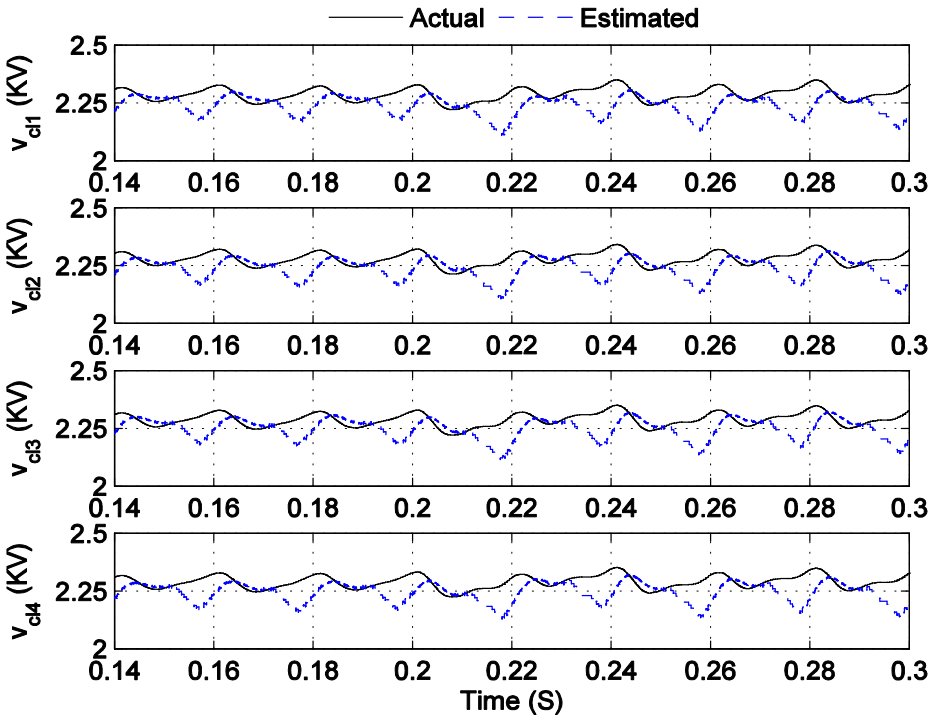


Figure 4.16: Case 1 actual and estimated voltages of the lower arm submodules of Phase a.

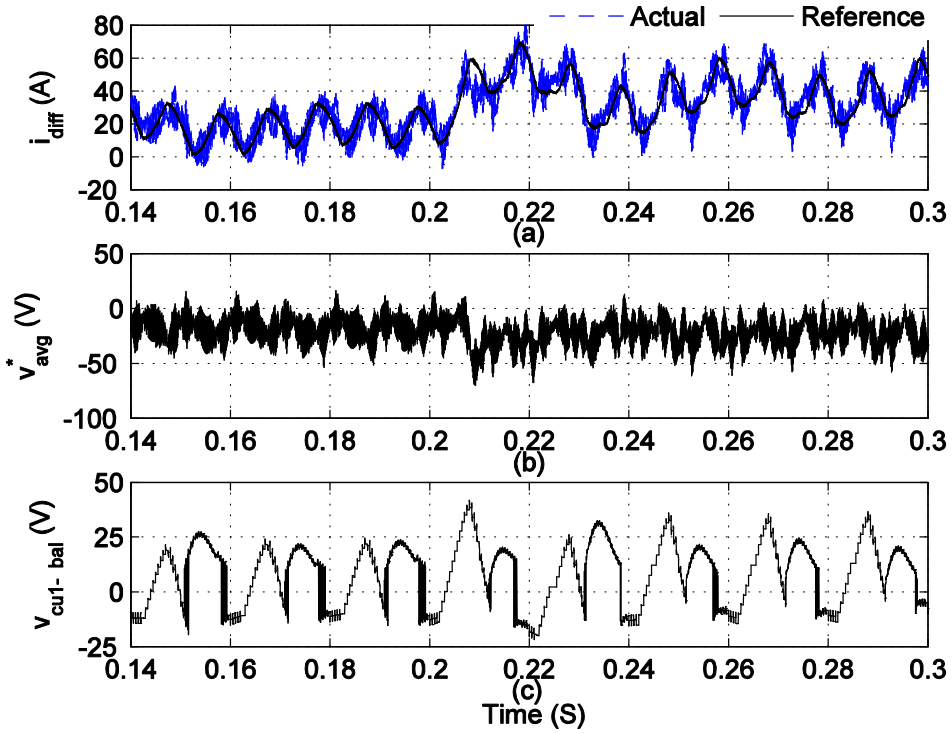


Figure 4.17: Action of the different controllers for Leg a during Case 1: a) actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first submodule of the upper arm.

4.4.2 Case 2: Dynamic performance during the boosting operation of the MMC

In this test scenario, the reference phase voltage signal v_o^* is kept at 1 pu and the capacitor reference voltage command is increased from 2.25 KV to 2.5 KV at t = 0.4 s. Setting v_c^* at values higher than *Vdc/N* results in boosting the operation of the MMC. This operation is useful to compensate for the load voltage during submodule faults. Figure 4.18(a) indicates the increase of the output of three-phase voltages from the MMC at t = 0.4 s when the proposed controller succeeds in boosting and balancing the capacitor voltages at the new set value of 2.5 KV, as illustrated in Figure 4.18(c). Yet again, fast dynamics with a tolerated error of the proposed capacitor voltage estimation units are revealed from Figures 4.19 and 4.20 for the submodules at the upper and lower arms, respectively. Boosting the capacitor voltages increases the circulating current. Hence, the balancing voltage signal is escalated, as demonstrated in Figure 4.21.

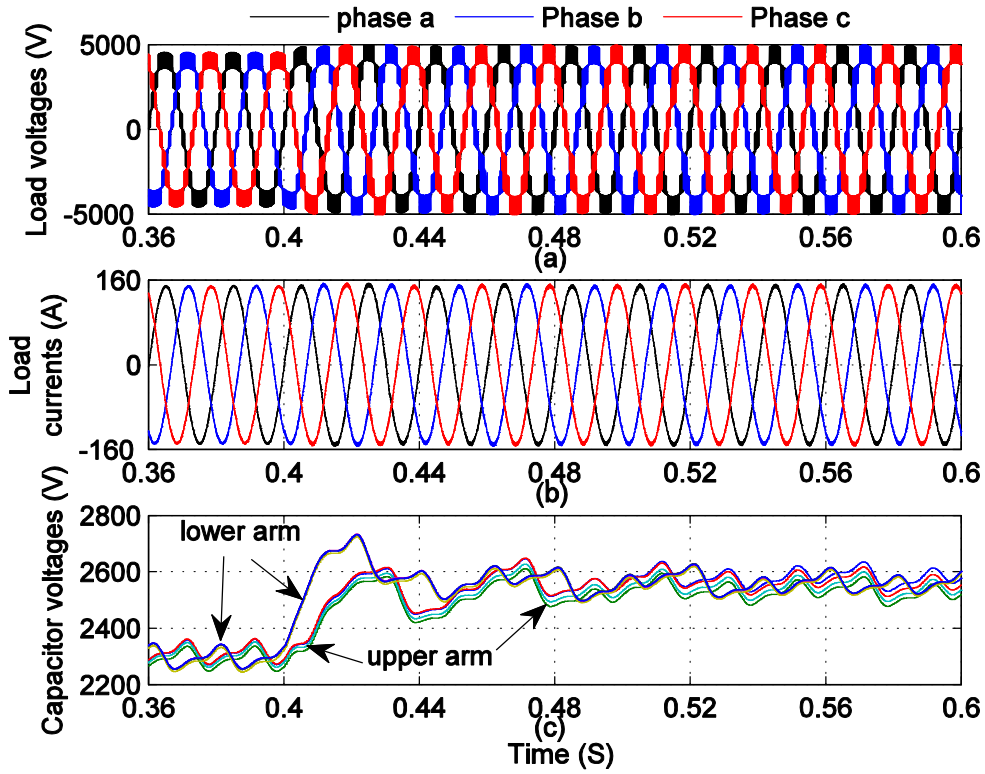


Figure 4.18: Load waveforms of Case 2: a) three-phase voltages, b) three-phase load currents, c) voltages of Leg a submodules.

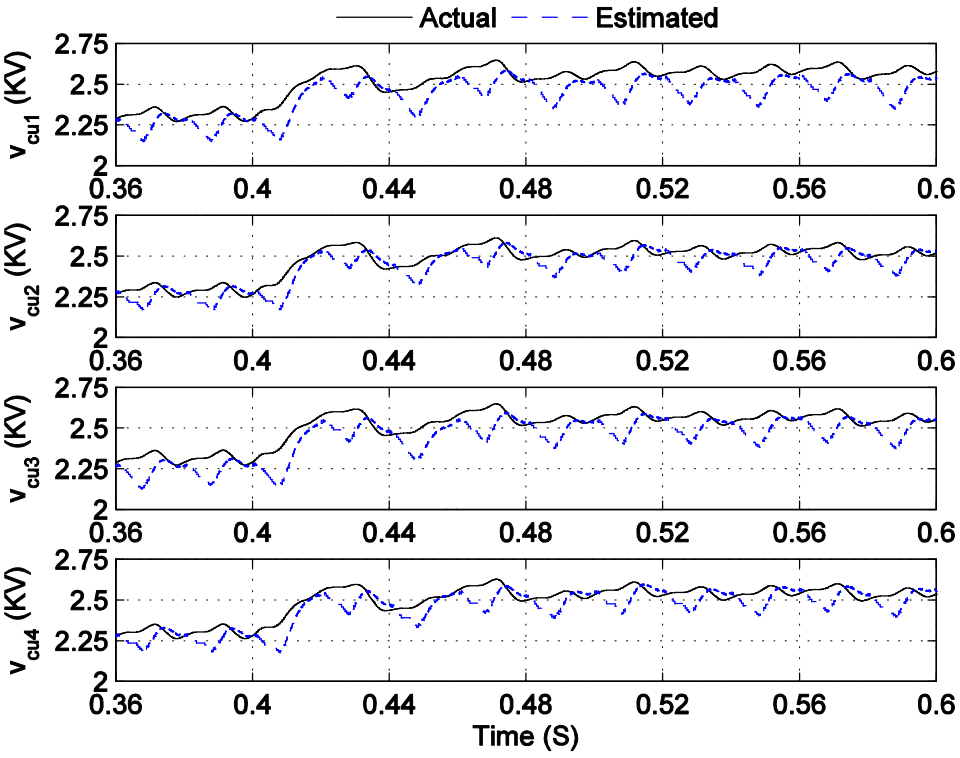


Figure 4.19: Case 2 actual and estimated voltages of the upper arm submodules of Phase a during the boosting operation.

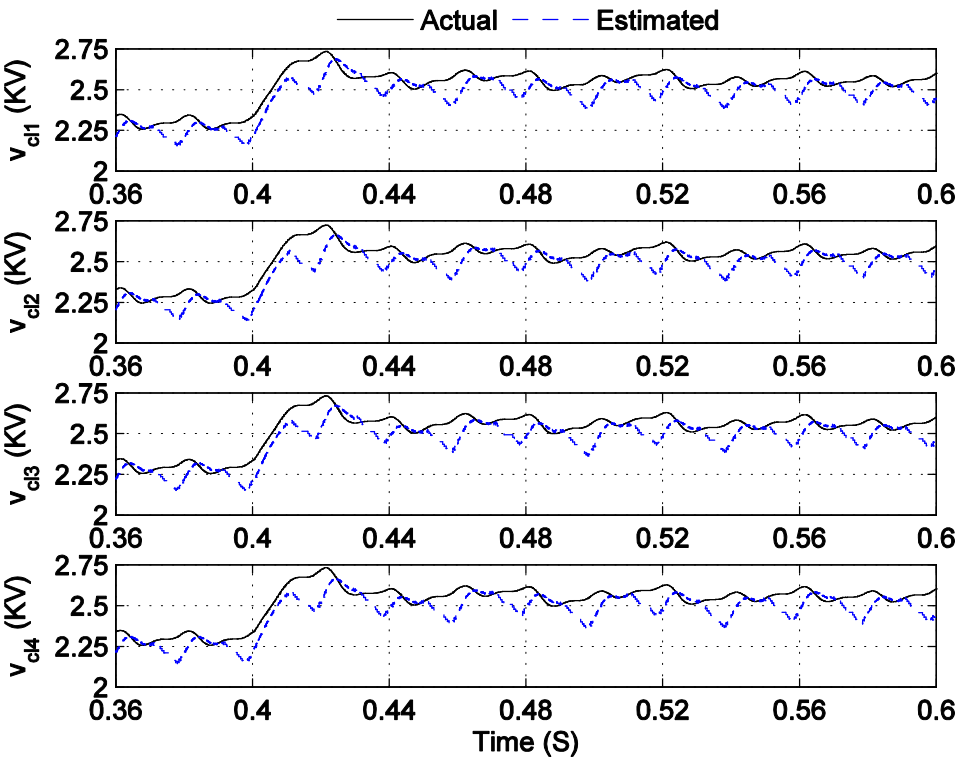


Figure 4.20: Case 2 actual and estimated voltages of the lower arm submodules of Phase a during the boosting operation.

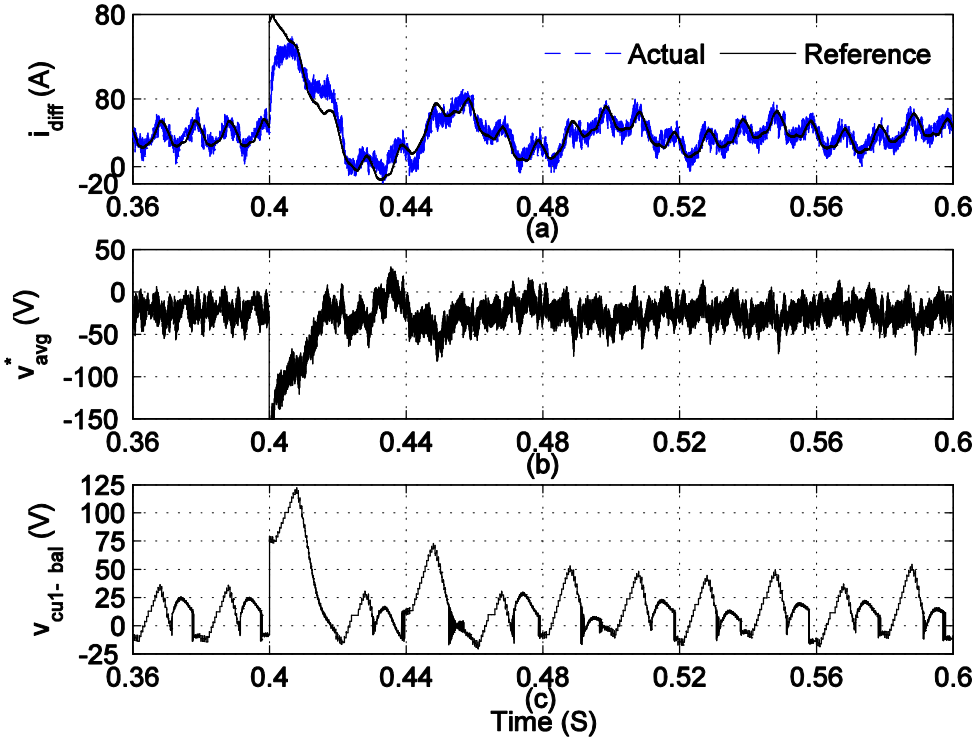


Figure 4.21: Action of the different controllers for Leg a during the boosting operation (Case 2): a) actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first submodule of the upper arm.

4.4.3 Case 3: Performance of capacitor voltage estimation algorithm in grid-connected MMC

This case is particularly developed to evaluate the proposed capacitor voltage estimation technique, when applied to an MMC-based HVDC system that integrates offshore wind power with the grid, and to investigate the accuracy of the proposed capacitor voltage estimation techniques for an MMC with a relatively high number of voltage levels. Furthermore, the dynamic performance of the proposed capacitor voltage estimation technique is assessed under external grid faults. The Model 2 MMC with the parameters shown in Table 4.2 is used. The simulated MMC has 152 submodules per leg. Unlike the previous cases, the capacitor voltage balancing technique used in this case is the reduced frequency-based technique presented in Subsection 3.2.3. The RLS capacitor voltage estimation technique provides it with the estimated capacitor voltages instead of using direct measurements. This is done to prove that the proposed RLS capacitor voltage estimation can be adopted for different capacitor voltage balancing techniques. In this case, the reference DC voltage signal is 640 kV. Then, at t = 6 s, a three-phase fault is applied at the grid side, which lasts for 0.2 s. The capacitor voltage estimation-based voltage balancing technique succeeds in balancing the capacitor voltages, as revealed from the balanced three-phase voltages presented in Figure 4.22. The RLS estimation algorithm provided the balancing control over the whole period even during the external fault period. Figures 4.23(a) and 4.23(b) illustrate the summation of capacitor voltages of the upper and lower arms. Moreover, the capacitor voltages of one submodule from the upper and lower arms are portrayed in Figures 4.23(c) and 4.23(d), respectively, which follows the traces of the actual capacitor voltages of the upper and lower arms, even during the grid fault. Results of this case proves that the proposed capacitor voltage estimation algorithm is not affected by external AC faults or the grid power controls. Therefore, the proposed capacitor voltage estimation algorithm is suitable for an MMC with a high number voltage levels, which are normally used in HVDC circuits.

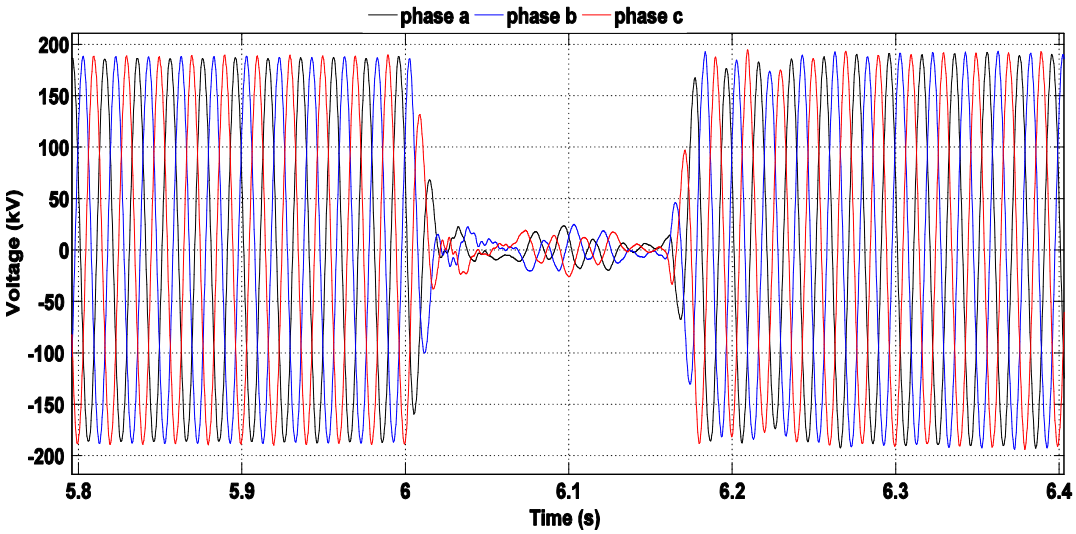


Figure 4.22: Case 3 voltages and currents of grid: a) three-phase voltages, b) three-phase currents.

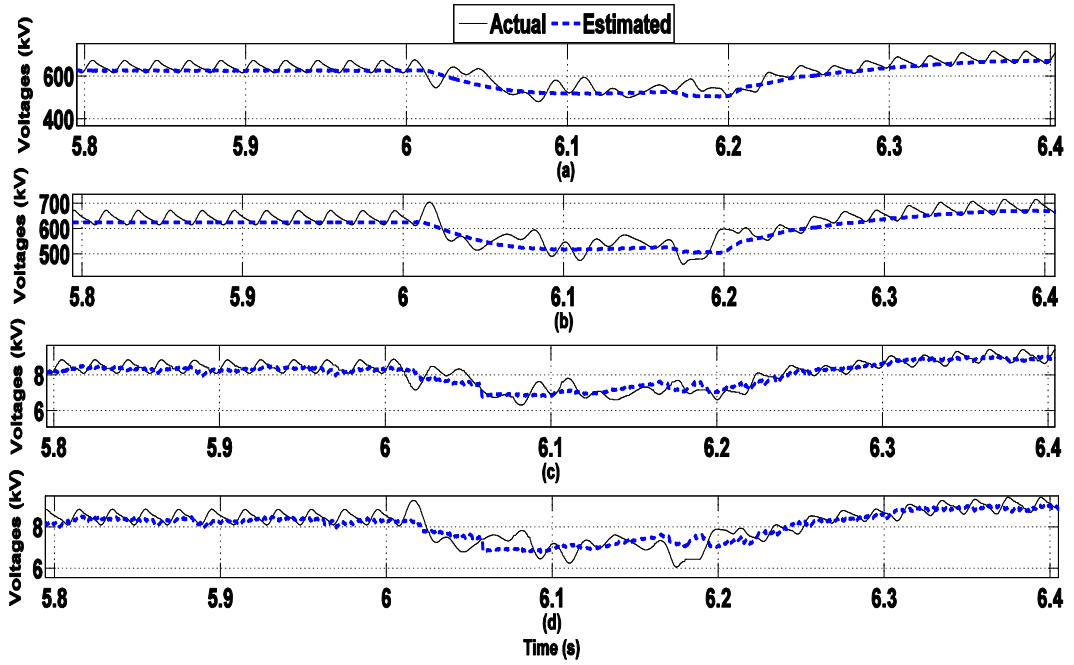


Figure 4.23: Case 3 actual and estimated signals of submodule capacitor voltages in Leg a: a) summation of capacitor voltages in the upper arm, b) summation of capacitor voltages in the lower arm, c) capacitor voltage of one submodule in the upper arm, d) capacitor voltage of one submodule in the lower arm.

4.5 Chapter Summary

This chapter has presented two capacitor voltage estimation units. The first one is based on the ADALINE algorithm, while the second is based on the RLS algorithm. Both are used for estimation submodule voltages of the MMC. For each

leg of the MMC, the proposed estimation units require only three sensors: one for the phase voltage and the other two for the voltages across the arm reactors. The proposed estimation unit is then integrated into a control strategy to balance the voltages across the submodules of the MMC. A comparison between the two estimation techniques has been conducted, showing that the RLS has better performance than the ADALINE in terms of speed and accuracy. As a result, the RLS has been incorporated into the capacitor voltage balancing algorithm. The proposed technique eliminates the need for direct measurement of capacitor voltages and associated communication systems, which renders it suitable for implementing a low-cost centralised controller for an MMC with a large number of submodules. The fast response and accurate tracking of the estimation unit under different dynamic conditions are validated in simulation results. It is important that the proposed MMC controller successfully balances the capacitor voltages at their set values even in boosting operation mode. Furthermore, it could easily balance the capacitor voltages of a grid connected MMC with a high number of voltage levels without being affected by the grid controls or external faults.

Chapter 5

Proposed Fault Detection Technique Based on Capacitor Voltage Estimation Algorithms

5.1 Introduction

Faults that can be located inside submodules of the MMC which are due to failures in semi-conductor devices not only affect the quality of the output power, but also threaten the safety of the converter. Since MMCs have a large number of submodules, the probability of having a fault inside a submodule is relatively high. As a result, it is highly recommended that detection and localization of the fault is carried out quickly, in order to enable the MMC inner control system to deal with the fault, by either converter disconnection or applying a suitable fault tolerant technique.

This chapter presents a new fault detection technique for the diagnosis and localization of submodule faults that develop due to failures in switching devices. As opposed to other fault detection strategies that have been proposed in the literature (Section 3.5), the proposed fault detection technique does not need extra sensors nor special power circuits, as it depends on a hybrid ADALINE-RLS capacitor voltage estimation algorithm, which combines the two estimation algorithms described previously in Chapter 4. The rest of this chapter is organized as follows:

Firstly, the MMC arm currents and submodule voltages are mathematically analysed during submodule faults to determine the consequences of such faults, which is a mandatory step for designing the proposed fault FDU. The proposed unit is then explained in detail, focusing on its advantages compared to other techniques proposed in the literature. Finally, various case studies are applied to the PSCAD-simulation model, in order to evaluate the performance of the FDU under various fault conditions.

5.2 The Proposed Fault Detection Strategy

This fault detection technique has been developed to solve all problems associated with other techniques found in the literature. As shown previously in section 3.5, most of these techniques require additional sensors to guarantee the robustness of the proposed technique, otherwise depending on software techniques such as the ANN-based detection method, which do not offer the required accuracy for this critical application. Thus, the proposed fault detection technique is classified as a model-based software technique. Figure 5.1 illustrates the block diagram of the proposed FDU. The proposed algorithm is built according to the electrical disturbances associated with submodule IGBT faults, without the need to incorporate any sensors or special power circuits, instead depending on an estimation of different signals, based on adaptive strategies.

As shown in Figure 5.2, the proposed FDU receives the values of the RLS estimated submodule capacitor voltages $v_{cxi\ RLS}$ ($x = u,l$) and ($i = 1,2,3.....,N$), then these values are divided by the reference capacitor voltage v_C^* to obtain the per-unit values $v_{cxi\ RLS\ pu}$.

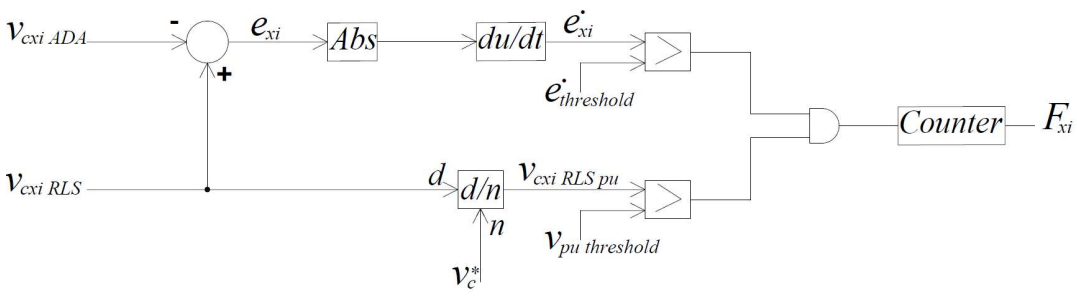


Figure 5.1. Block diagram of the proposed FDU.

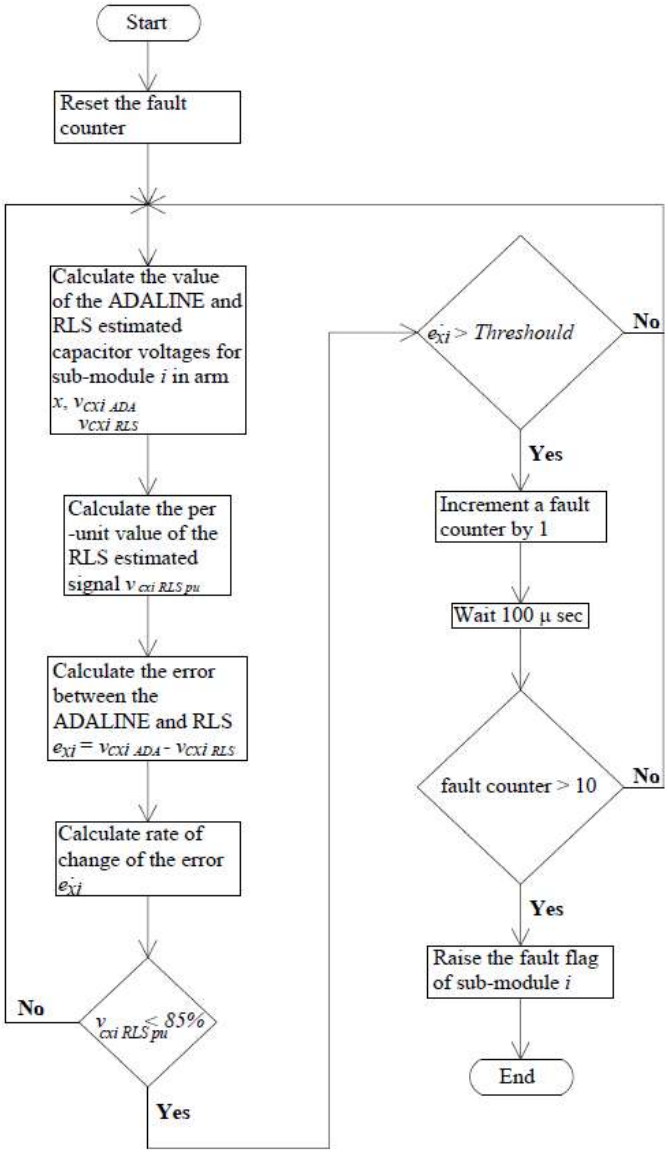


Figure 5.2. Flowchart of the proposed fault detection technique.

At the same time, the error between the ADALINE-estimated capacitor voltage, $v_{cxi\ ADA}$ and the RLS-estimated voltage $v_{cxi\ RLS}$ of each submodule is calculated, and then passed through a high speed differentiator to calculate the rate of change of the error signals $\dot{e_{xi}}$. The next step involves determining each per-unit value of the voltage estimated signal $v_{cxi\ RLS\ pu}$, whether it is higher than 85% or not. The reason for this check is based on the fact that the per-unit estimation of capacitor voltage of a faulty submodule is decreased during faults, this is simply due to the increased error between the actual signal and its estimation as the right and left hand sides of (4.1) and (4.2) being no longer equal. If the comparison result is

true, then the checked submodule is considered to be in a healthy condition, otherwise the algorithm starts to check the differentiated error signal $\dot{e_{xl}}$ and compares it with a predefined threshold, $v_{pu\,threshold}$, which is selected based on the required sensitivity of the FDU.

The reason for calculating this error is that the proposed FDU is based on the difference between the dynamic behaviours of the ADALINE and RLS algorithm results, which is due to their different natures. The FDU here depends on the difference of the behaviour between the two algorithms. As illustrated in the Widro-hoff learning rule given in (4.3), which is used in the update of the ADALINE-estimated voltages, the weighting vector of the current iteration, $W(k+1)$, is updated by adding the error reduction component $\alpha \frac{X(k)(y(k)-\hat{y}(k))}{X(k)^T X(k)}$ to the weighting vector of the previous iteration, $W(k)$. This means that the ADALINE algorithm has no memory, since the Widro-hoff equation is independent of the accumulative value of weighting vectors. This allows the ADALINE to be able to rapidly track sudden changes in capacitor voltage. However, it needs a relatively long time to reach convergence.

Unlike the ADALINE, updating the weighting vector of the RLS algorithm depends on the accumulation of historic values of previous capacitor voltages, as demonstrated in (4.6) and (4.7). This means that the RLS algorithm has a reduced convergence time when compared with the ADALINE. However, in the situation of having a sudden change in capacitor voltage (which occurs during submodule faults), the RLS has a slower response in tracking capacitor voltages.

If the error signal, $\dot{e_{xl}}$ is lower than the threshold, $\dot{e_{threshold}}$, the algorithm considers the submodule as being in a healthy condition, otherwise it increases a counter by one and then starts a 100 μs timer. After this time period, the algorithm repeats the same steps and if the counter reaches 10, this implies that the submodule is faulty.

The proposed method proved its reliability and robustness, as it was tested under different healthy and faulty conditions. This is because it makes the decision based on two factors: the estimated per-unit voltage, and the rate of change of the estimated voltage error signals. Moreover, this method does not require any additional components or devices, as it is based on simple calculations, and can

detect the fault in less than 5ms for short-circuit faults and less than 35 ms for open-circuit faults.

5.3 Simulation Results

The dynamic behaviour of the proposed FDU is tested under different fault conditions when applied to the PSCAD simulations of the MMC, presented in Table 4.1. The first case is devoted to assessing the dynamic performance of the proposed FDU during an open-circuit fault in a submodule, while the second case examines FDU behaviour for the MMC under a short-circuit fault in a submodule. Finally, the third case simulates two faults in two different arms, in order to assess the performance of the FDU during multiple faults.

5.3.1 Case 1: Performance under IGBT open circuit fault

This task is devoted to assessing the capabilities of the proposed FDU under an IGBT open-circuit fault in a submodule. The upper switch of the third submodule in the upper arm of phase *a* is intentionally opened at $t= 0.5s$. As a result, the voltage and current of phase *a* are distorted, as shown in Figures 5.3(a) and 5.3(b), respectively, due to the imbalance of submodule capacitor voltages. The main reason leading to the failure of the voltage-balancing strategy is the increased capacitor voltage of the faulty submodule. This is logical, since the capacitor is allowed only to be charged, with no path for discharging, due to the open circuit condition. One important concern in this case is that all capacitor voltages of the healthy submodules located in the arm are increased, as illustrated in Figure 5.3(c). The increase in capacitor voltages stresses the insulation of MMC components, and may lead to a cascading failure in other submodules.

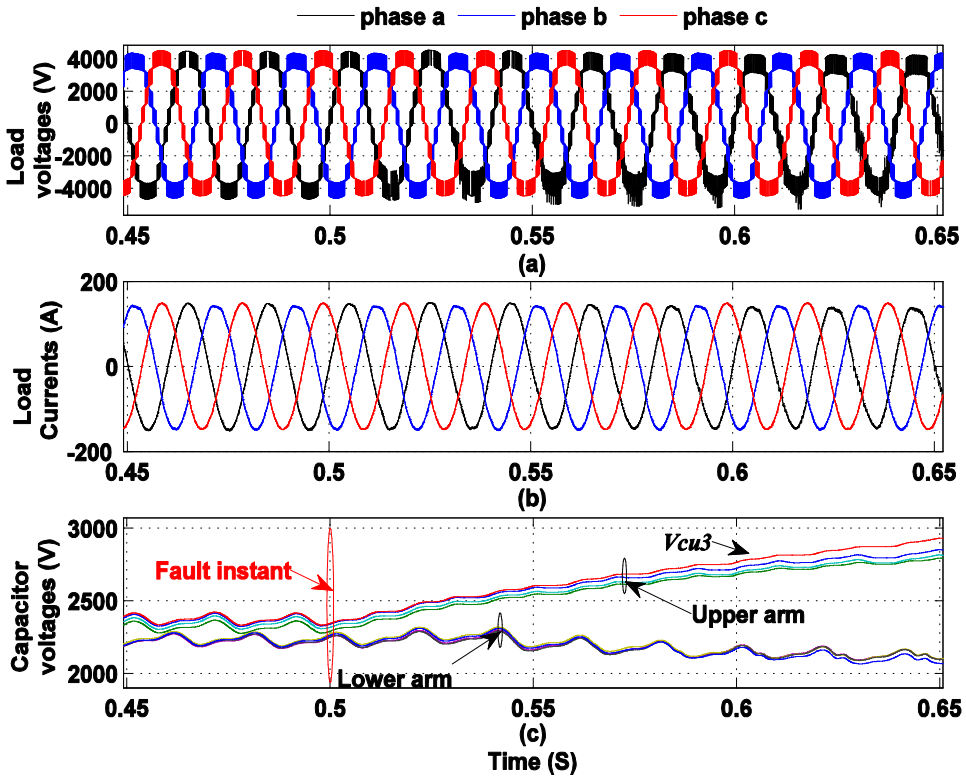


Figure 5.3. FDU performance during an open-circuit fault on the third submodule of the upper arm: a) Three-phase voltages, b) three-phase load currents, c) voltages of leg a submodules.

Figures 5.4 and 5.5 clearly illustrate that the voltages of the healthy submodules adequately track their actual voltages, which proves the robustness of the estimation algorithm during faults, as errors between the actual and estimated signals have not reached 10%. Regarding the faulty submodule, there is a considerable error between the estimated voltage and its corresponding actual voltage, due to the decreased value of the estimated voltage, which enables the FDU algorithm to detect the fault. Figure 5.6 (a) indicates that the differential current is oscillating to twice its value during normal operating conditions. This means that the MMC is no more stable as the differential current, which flows inside the MMC, and the arm currents may exceed their capacities. In other words, the controller failed to balance the capacitor voltages during faults. Moreover, the heavy oscillations of the differential current are transferred to the averaging and balancing control signals, as demonstrated in Figures 5.6 (b) and (c), respectively. As a result, the MMC is no longer stable and must be deactivated.

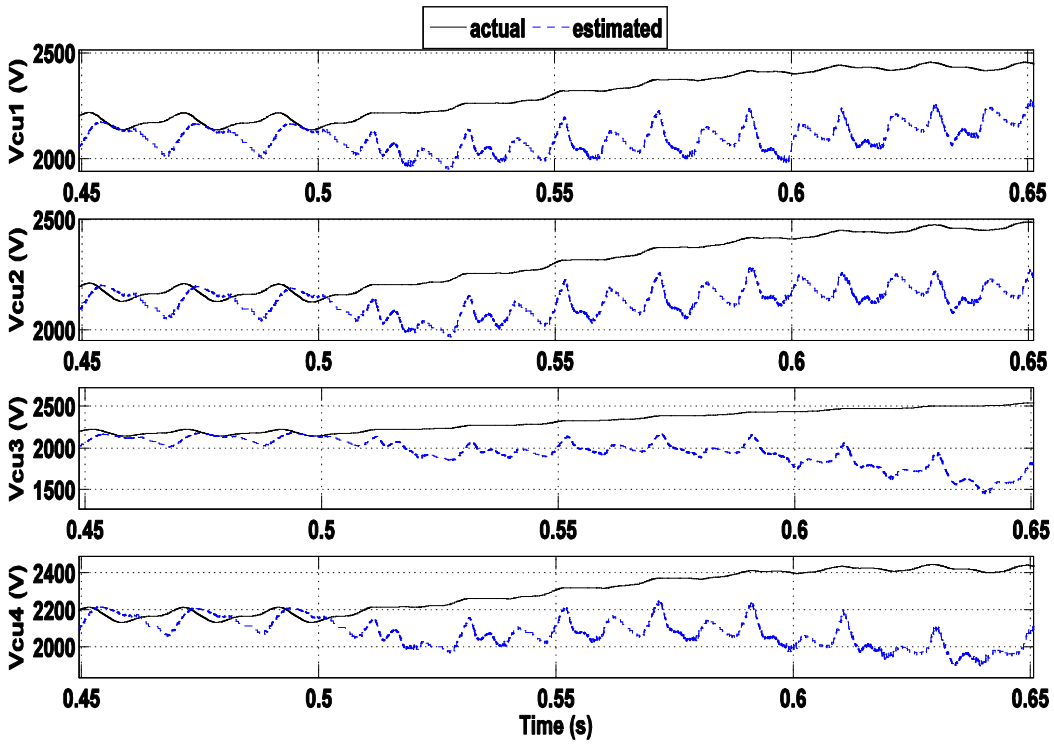


Figure 5.4. Actual and estimated voltages of the upper arm submodules of phase a, under an open-circuit fault.

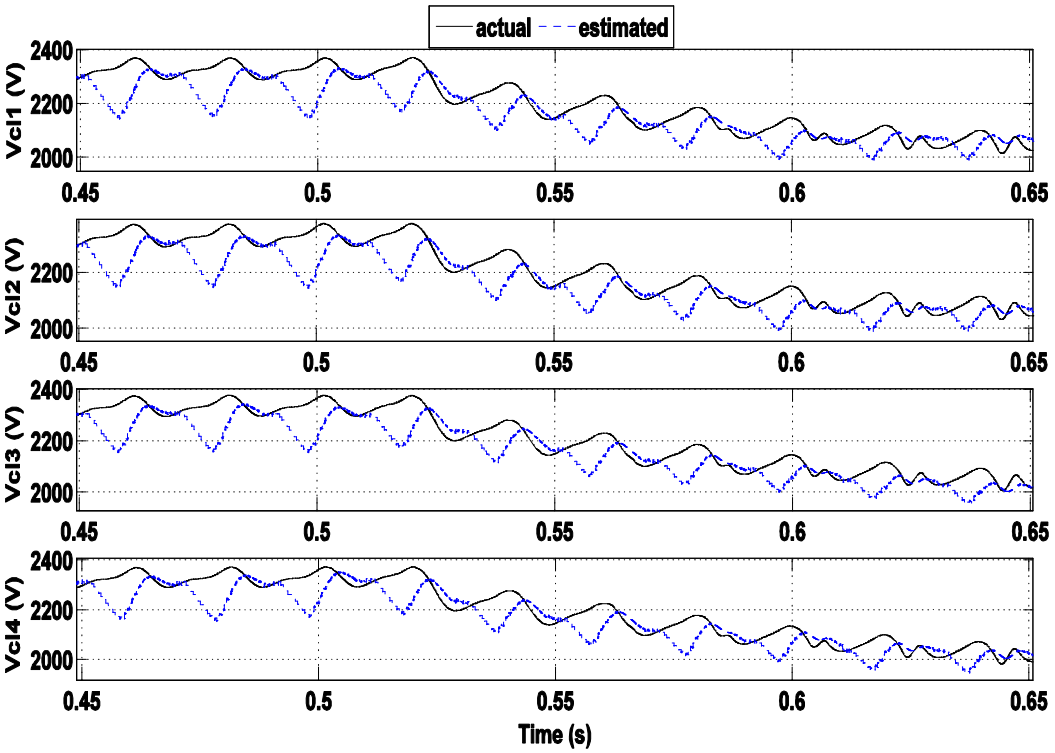


Figure 5.5. Actual and estimated voltages of the lower arm submodules of phase a, under an open-circuit fault.

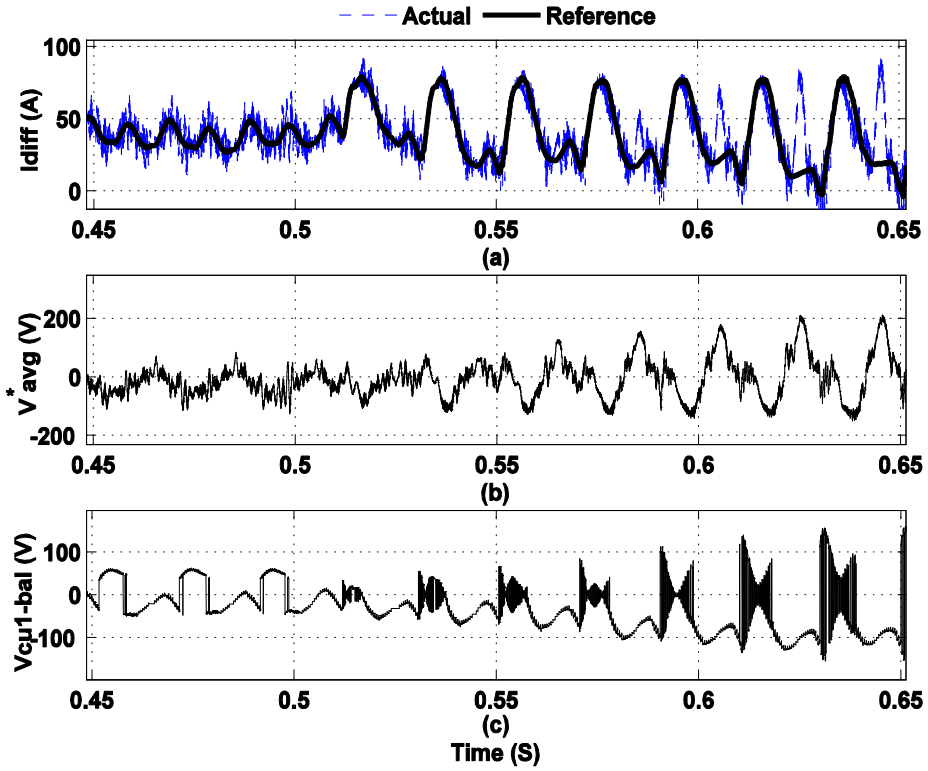
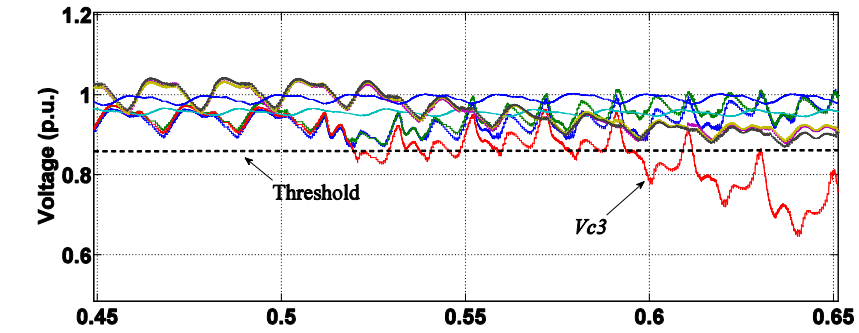
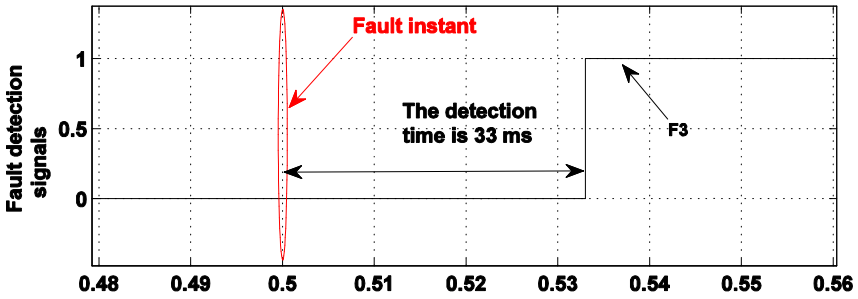


Figure 5.6. Action of the different controllers for leg a during the open-circuit fault: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first submodule of the upper arm.

As shown in Figure 5.7(a), the estimated voltage of the faulty submodule exceeded the FDU voltage threshold for a longer period than the other voltages. This is the first condition for the FDU to detect the fault. The estimated signals of all other submodules in the healthy arm are by far higher than the FDU voltage threshold. Ten ms after the fault, the derivative of the error signal between the RLS and ADALINE-estimated voltages for the faulty submodule by far exceeded the pre-defined threshold, and this is the second condition which the FDU needs to satisfy to successfully detect the fault. The FDU succeeds in detecting and localizing the fault 33 ms after being activated, as illustrated in Figure 5.7 (b). With the slow rate of increase of the capacitor voltages, the 33 ms period of detecting an open-circuit fault is enough to guarantee the safety of the MMC.



(a)



(b)

Figure 5.7: The performance of the FDU under IGBT open circuit fault: a) The RLS estimated voltages of the upper arm of phase a, b) The detection time consumed by the FDU to detect the open circuit fault.

5.3.2 Case 2: Performance under IGBT short circuit fault

This case is conducted in order to investigate the capabilities of the proposed FDU under IGBT short circuit fault in a submodule. A short-circuit fault is applied to the upper switch of the third submodule in the upper arm of phase *a* at *t= 0.5s*. Figures 5.8 (a) and 5.8(b) illustrate the increased level of harmonics and DC components on the voltage and current waveforms of phase *a*, respectively. The submodule capacitor voltages are not balanced, as indicated in Figure 5.8(c).

Figures 5.9 and 5.10 show the RLS estimated capacitor voltages. The voltages of the healthy submodules adequately track their actual voltages, which proves the robustness of the estimation algorithm during faults. Regarding the faulty submodule, there is an error between the estimated voltage and its corresponding actual voltage, which enables the FDU algorithm to detect the fault.

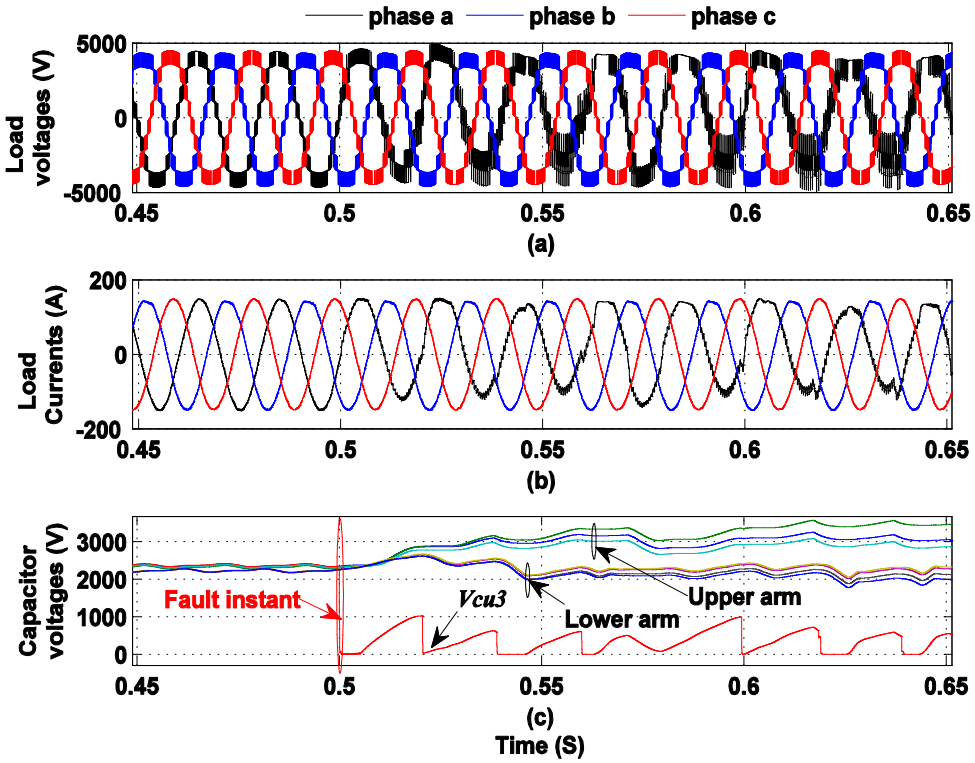


Figure 5.8: Operation during a short-circuit fault on the third submodule of the upper arm: a) Three-phase voltages, b) three- phase load currents, c) voltages of leg a submodules.

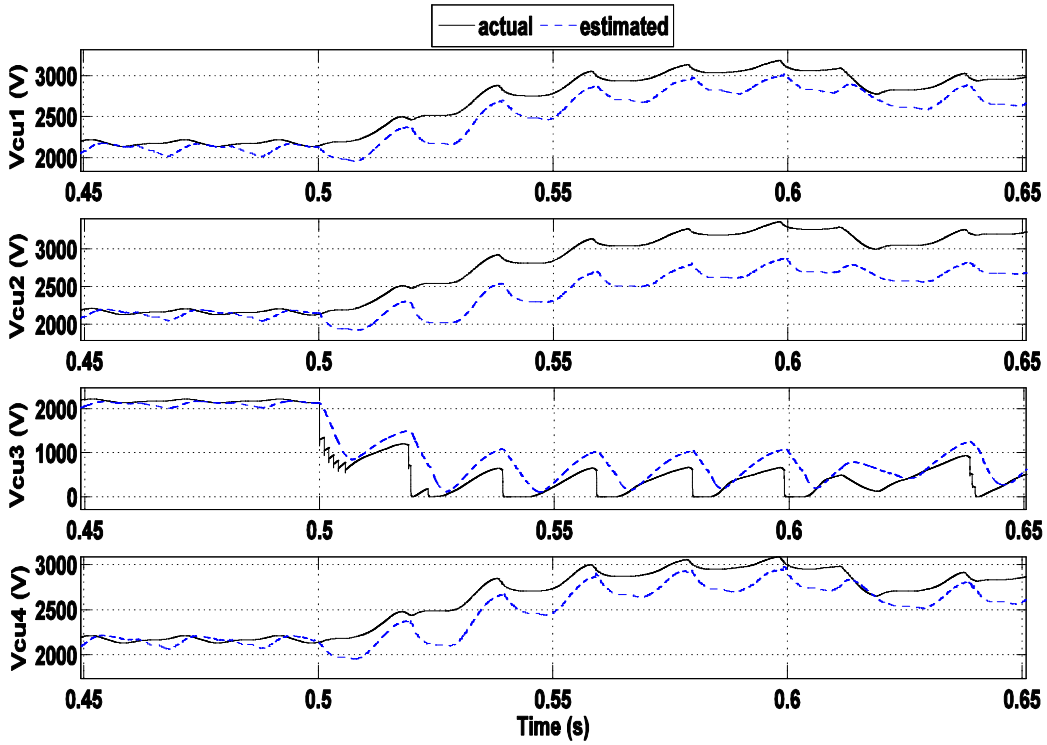


Figure 5.9: Actual and estimated voltages of the upper arm submodules of phase a, under a short-circuit fault.

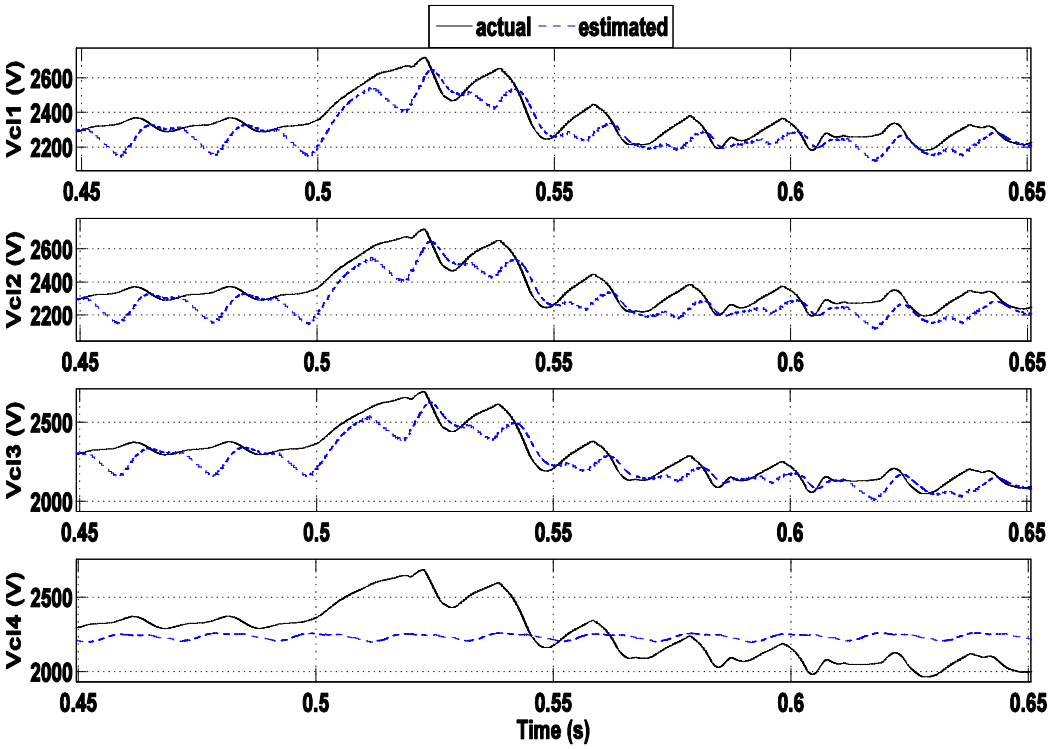


Figure 5.10: Actual and estimated voltages of the lower arm submodules of phase a, under a short-circuit fault.

The voltage-balancing strategy fails due to short-circuiting the faulty submodule capacitor when activating its lower switch. The proposed balancing strategy fails to regulate the differential current at its increased reference signal, as shown in Figure 5.11 (a). The value of differential current approaches the level of the load current, which threatens the safety of the MMC as the arm currents may exceed the rated current of the IGBT switches. Consequently, the averaging and balancing control signals are not stable, and bounce between the upper and lower limits of their controllers, as exhibited in Figures 5.11 (b) and (c), respectively. These results demonstrate that it is extremely dangerous to continue operation of the MMC with an IGBT short circuit fault without either the disconnection of the MMC, or applying a suitable fault tolerant control strategy.

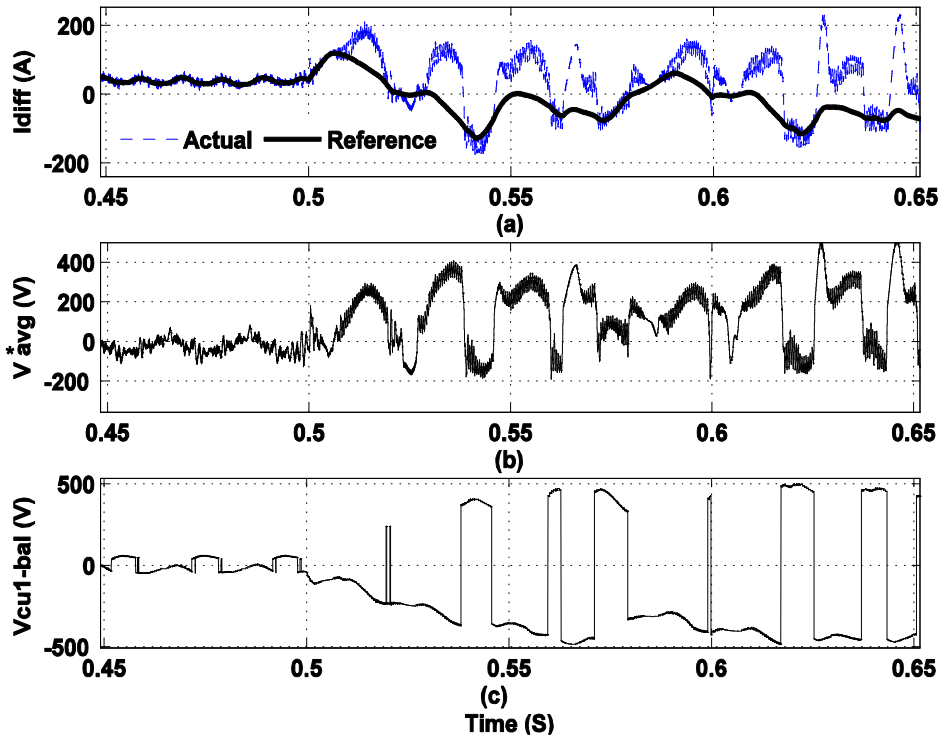


Figure 5.11: Action of the different controllers for leg a during the short-circuit fault: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first submodule of the upper arm.

As shown in Figure 5.12 (a), the estimated voltage of the faulty submodule exceeded the FDU voltage threshold for a longer period than the other voltages. This is the first condition for the FDU to detect the fault. While the estimated signals of all other submodules in the healthy arm are by far higher than the FDU voltage threshold. Also the derivative of the error signal between the RLS and ADALINE-estimated voltages for the faulty submodule by far exceeded the pre-defined threshold, and this is the second condition which the FDU needs to satisfy to successfully detect the fault. The FDU succeeds in detecting and localizing the short-circuit fault after 2.2 ms from its incidence, as demonstrated in Figure 5.12. (c). This detection time is fast, as the required time for clearing short circuit faults must not exceed 5 ms [25].

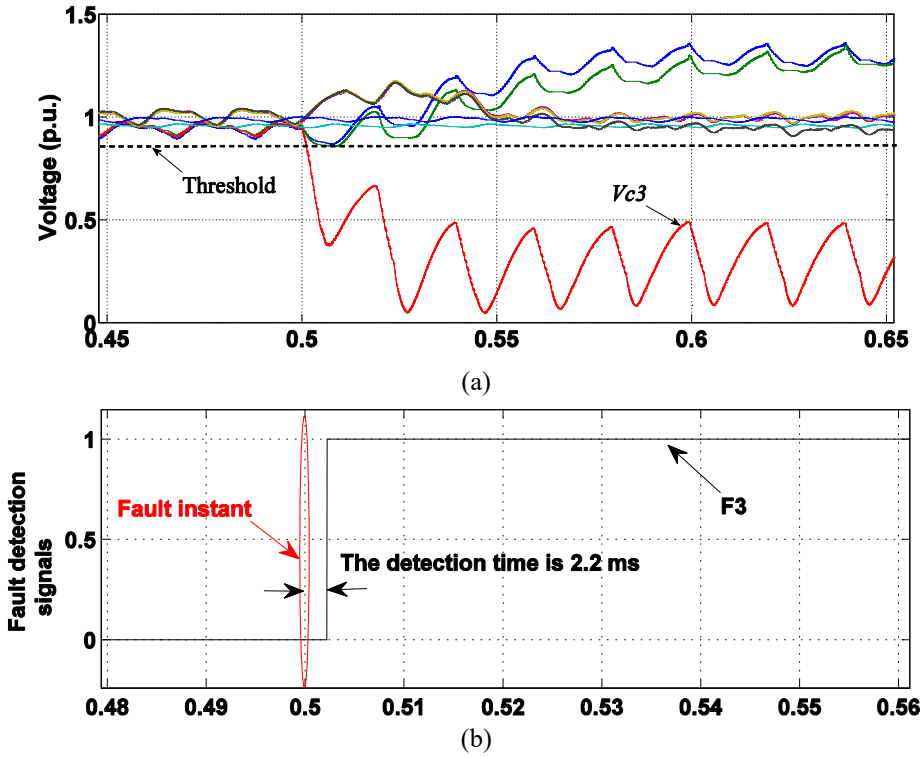


Figure 5.12: The performance of the FDU under IGBT short circuit fault: a) The RLS estimated voltages of the upper arm of phase a, b) The detection time consumed by the FDU to detect the open circuit fault.

5.3.3 Case 3: Performance under multiple faults in two different arms

This case is conducted in order to investigate the capabilities of the proposed FDU under multiple faults in two different arms. An open-circuit fault is applied to the upper switch of the third submodule in the upper arm of phase *a* at $t= 0.5s$, while a short circuit fault is applied to the lower switch in the second submodule in the lower arm of phase *a* at $t= 0.7s$. As shown in Figures 5.13 (a) and 5.13(b), the voltage and current of phase *a* suffer from an increased level of harmonics and high DC component just after the occurrence of the open-circuit fault. After applying the short circuit fault, the harmonics increase, affecting the power quality of the voltage and current and lowering it to a very poor level. The submodule capacitor voltages start to lose their balance just after the first fault, and increase rapidly after the application of the second fault, as indicated in Figure 5.13(c).

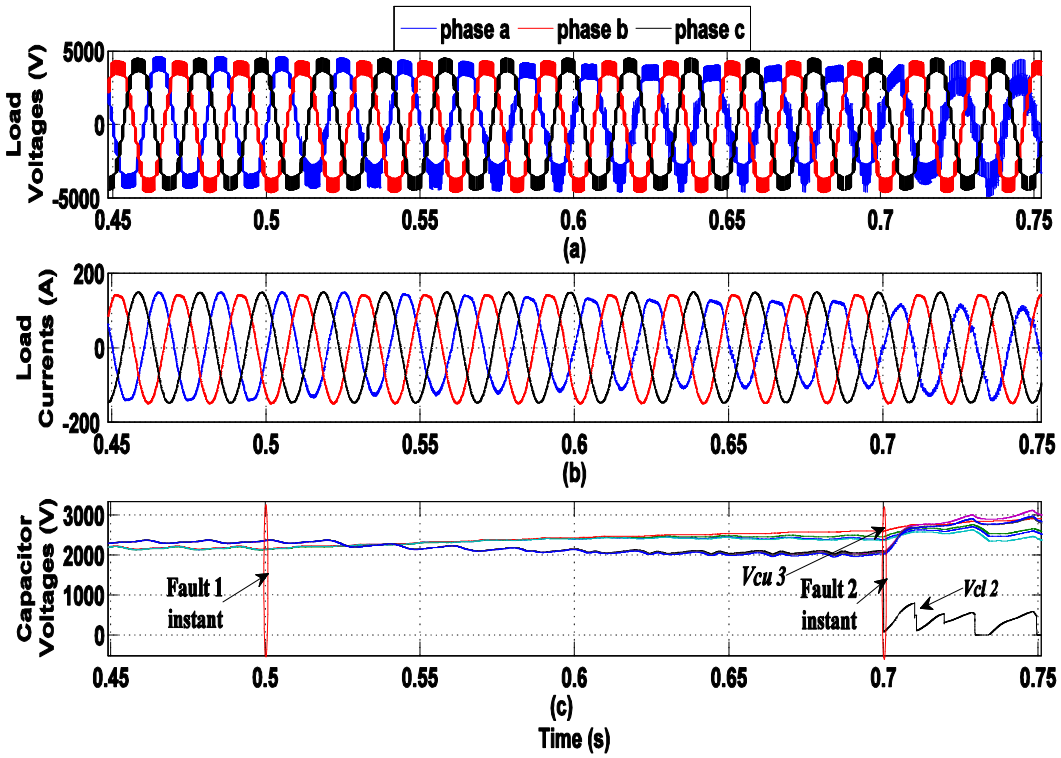


Figure 5.13: Operation during multiple faults: a) Three-phase voltages, b) three-phase load currents, c) voltages of leg a submodules.

The RLS-estimated voltages of leg *a* are shown in Figures 5.14 and 5.15. These estimated voltages track their actual voltages until the occurrence of the two faults. Following each fault, the estimated voltages contain a steady-state error. Regarding the estimated voltages of the faulty submodules, it is apparent that these signals rapidly decrease, which enables the FDU to easily detect the two faults.

Since the capacitor voltage of the third submodule cannot be charged and discharged properly due to the first fault, the voltage-balancing strategy partially fails to achieve its function. However, after the second fault, the situation becomes worse, and the balancing algorithm totally fails to balance the capacitor voltages. This appears in the failure of regulating the differential current at its increased reference signal, as shown in Figure 5.16 (a).

The value of differential current approaches the level of the load current after the first fault, and exceeds it after the second fault. This condition threatens the safety of the MMC, as the arm currents may exceed the rated current of the IGBT switches. Consequently, the averaging and balancing control signals are not stable, and bounce between the upper and lower limits of their controllers, as exhibited in Figures 5.16

(b) and (c), respectively. These results demonstrate that it is dangerous to continue operation of the MMC under multiple faults without a fault tolerant control.

As shown in Figure 5.17 (a), the estimated voltage of the two faulty submodules exceeded the FDU voltage threshold for a longer period than the other voltages. This is the first condition for the FDU to detect the fault. While the estimated signals of all other submodules are by far higher than the FDU voltage threshold. Also the derivative of the error signal between the RLS and ADALINE-estimated voltages for the faulty submodules by far exceeded the pre-defined threshold, and this is the second condition which the FDU needs to satisfy to successfully detect the fault. The FDU succeeds in detecting and localizing the first fault after 18.8 ms, while for the second fault the detection time is lower than 2.2 ms, as demonstrated in Figure 5.17. (b). This case has proved that the proposed FDU is able to detect multiple faults very quickly, which is required in MMCs as the high number of submodules may lead to several failures concurrently.

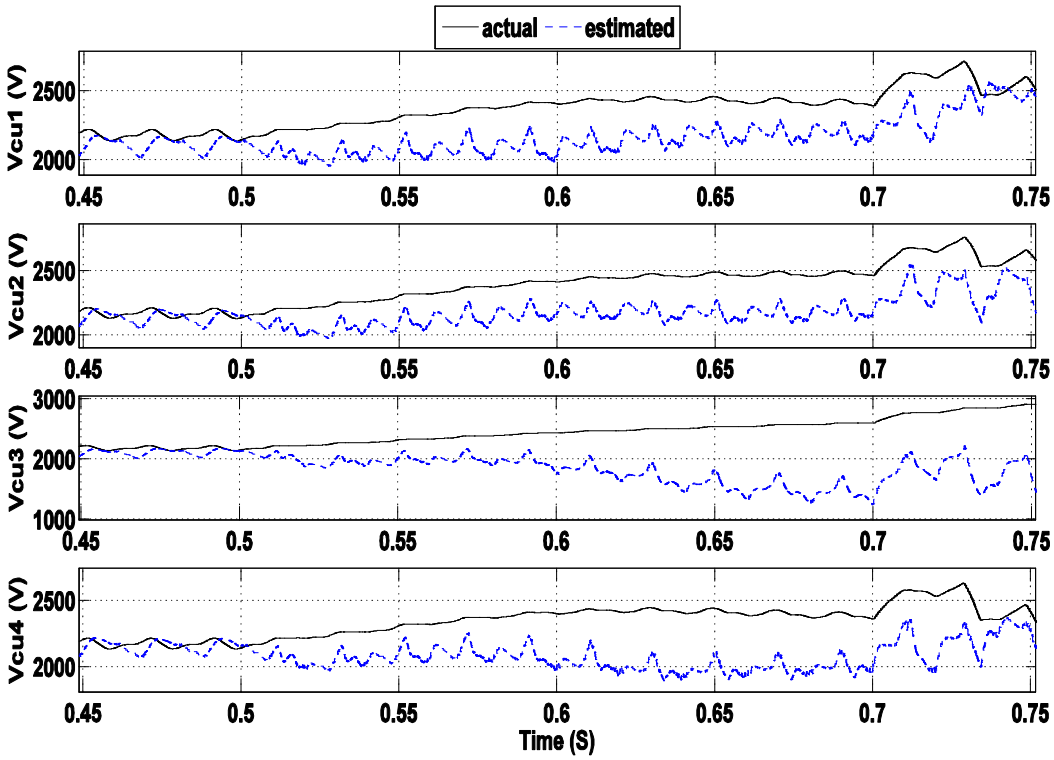


Figure 5.14: Actual and estimated voltages of the upper arm submodules of phase a, under two faults.

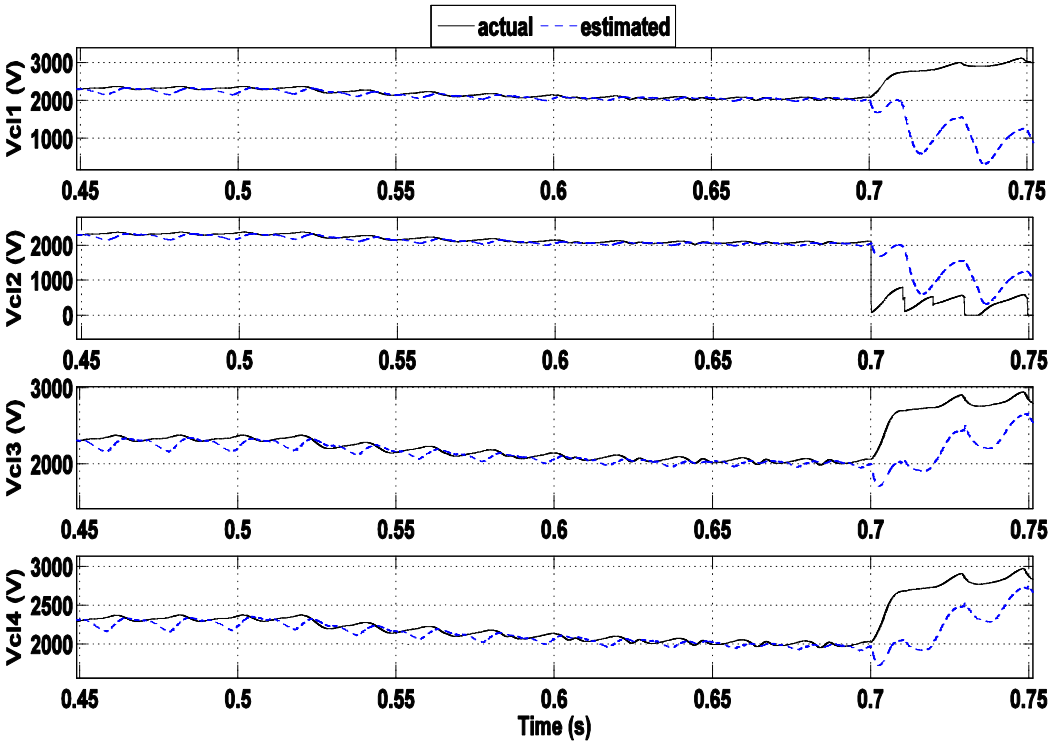


Figure 5.15: Actual and estimated voltages of the lower arm submodules of phase a, under two faults.

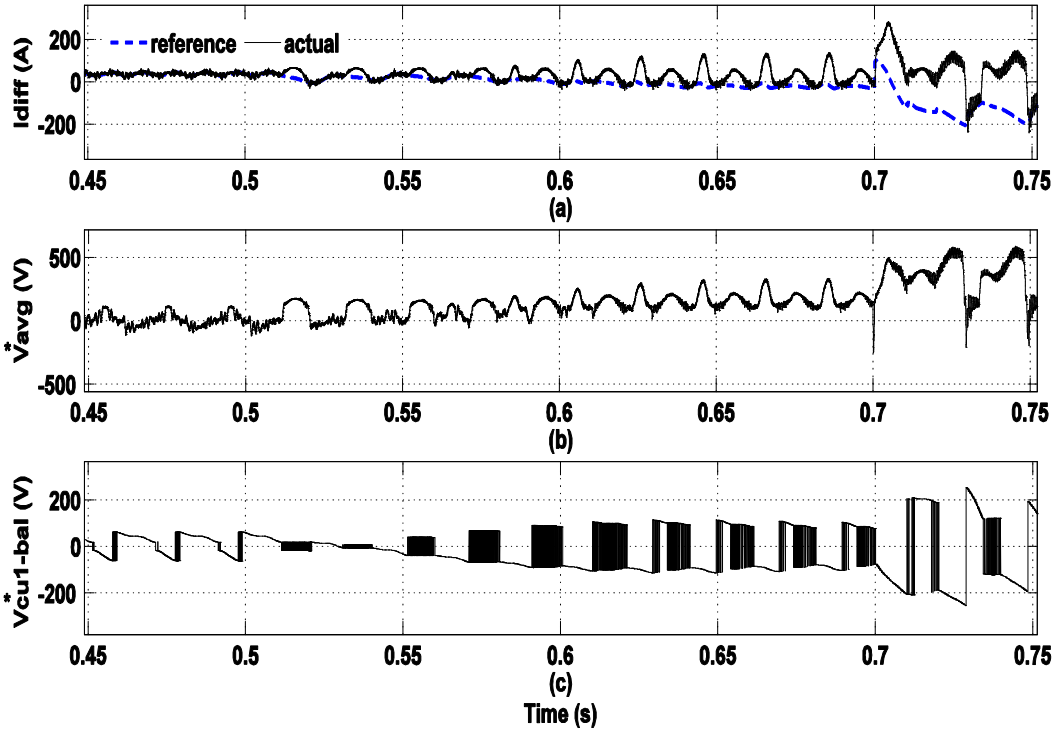
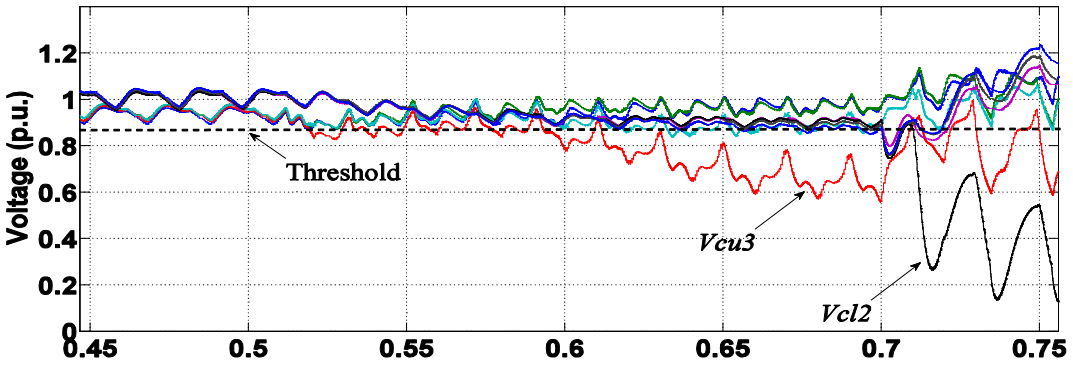
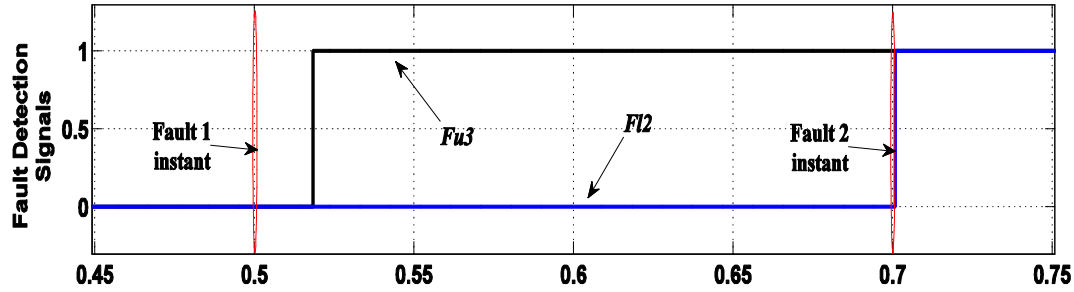


Figure 5.16: Action of the different controllers for leg a during multiple faults: a) actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first submodule of the upper arm.



(a)



(b)

Figure 5.17: The performance of the FDU under two faults: a) The RLS estimated voltages of the upper arm of phase a, b) The detection time consumed by the FDU to detect the open circuit fault.

5.4 Chapter Summary

In this chapter, a new fault detection technique for the detection and localization of MMC submodule switch faults has been presented. The proposed FDU is based on a hybrid ADALINE-RLS capacitor voltage estimation algorithm, and does not require any additional components as they are based on the estimation algorithms that are simultaneously utilized for the proposed control of the MMC (presented in Chapter 4). PSCAD simulations illustrated the technique's accuracy for detecting and localizing different faults, and is a result of its hybrid processing where the fault decision is not only based on reduction of the estimated per-unit voltage, but also on the rate of change of the difference between the estimated voltages from the proposed ADALINE and RLS algorithms. Further, the results show the necessity of having a fault tolerant control scheme to protect the MMC during submodule faults, which helps it to continue in a safe operation mode, which is discussed in Chapter 6.

Chapter 6

Proposed Fault Tolerant Control Strategy Based on a Sorting Algorithm

6.1 Introduction

FTC systems are required to provide the MMC with fault-handling capability without blocking the converter during faults. Thus, this concept enhances the reliability of the MMC by increasing its availability with high levels of security, even in the case of having internal faults. This chapter presents a new fault tolerant control technique, which is integrated with the proposed capacitor voltage balancing and fault detection strategies presented in Chapters 4 and 5, respectively, in order to provide a complete inner controller for the MMC which is capable of controlling the converter during normal and abnormal operations. The proposed fault tolerant control is based on updating the parameters of the proposed capacitor voltage balancing technique, and the PS-PWM switching algorithm. This means that it does not need any redundant components or special conditioning circuits, which makes it very cost effective when compared to other techniques proposed in the literature (Section 2.9).

Firstly, the proposed FTC strategy is explained. Then, the reliability of the MMC is assessed before and after applying the proposed fault tolerant control technique, in order to evaluate the amount of reliability enhancement. Finally, the

inner MMC control technique, which contains the proposed capacitor voltage balancing, fault detection and fault tolerant control techniques is tested using PSCAD simulations, in order to evaluate its performance under different operating conditions.

6.2 The Proposed Fault Tolerant Control Algorithm

The proposed FTC system is built to overcome the problems presented in the previous section. The developed technique offers a good alternative to others proposed in the literature, as it does not need redundant components nor special circuits, whilst at the same time it does not affect the quality of the output power.

The proposed fault tolerant control unit (FTCU) has two main tasks: to isolate faulty submodules, and to modify the capacitor balancing algorithm. As shown in Figure 6.1, the sorting algorithm starts with the acquisition of the fault flags F_{x1}, F_{x2}, ... and F_{xN}. where x can be either u for the upper arm or l for the lower arm.

It then calculates the number of faulty submodules in the arm, as per the following expression:

$$N_{xF=\ x1}+F_{x2}+\cdots+F_{xN} \tag{6.1}$$

The algorithm then compares the percentage of faulty submodules to the total number of submodules in each arm. If this percentage is higher than 25%, the FTC sorting algorithm considers this a cascading failure condition, which means that a critical problem has occurred in the whole arm, and will spread to other arms. Thus, the algorithm isolates all MMC submodules and blocks the converter. If the percentage of faulty submodules is less than 25%, the sorting algorithm isolates the faulty submodules, and compares the number of faulty submodules in the upper and lower arms of each leg. If this number is not equal, it then isolates some healthy submodules until it becomes equal, in order to balance the energy between the two arms. Moreover, the algorithm calculates the number of effective submodules that are still in the operation:

$$N_{eff} = N - 2N_{xi} \tag{6.2}$$

After this step, the algorithm updates the reference capacitor voltage v_c^* according to the new number of connected submodules N_{eff}, to compensate the energy lost due to the isolation of faulty submodules:

$$v_c^* = v_c^* \frac{N}{N_{eff}} \tag{6.3}$$

Finally, the algorithm modifies the phase shift of the PS-PWM presented in (2.23), in order to cope with the new number of submodules:

$$\theta = \frac{360}{N_{eff}-1} \tag{6.4}$$

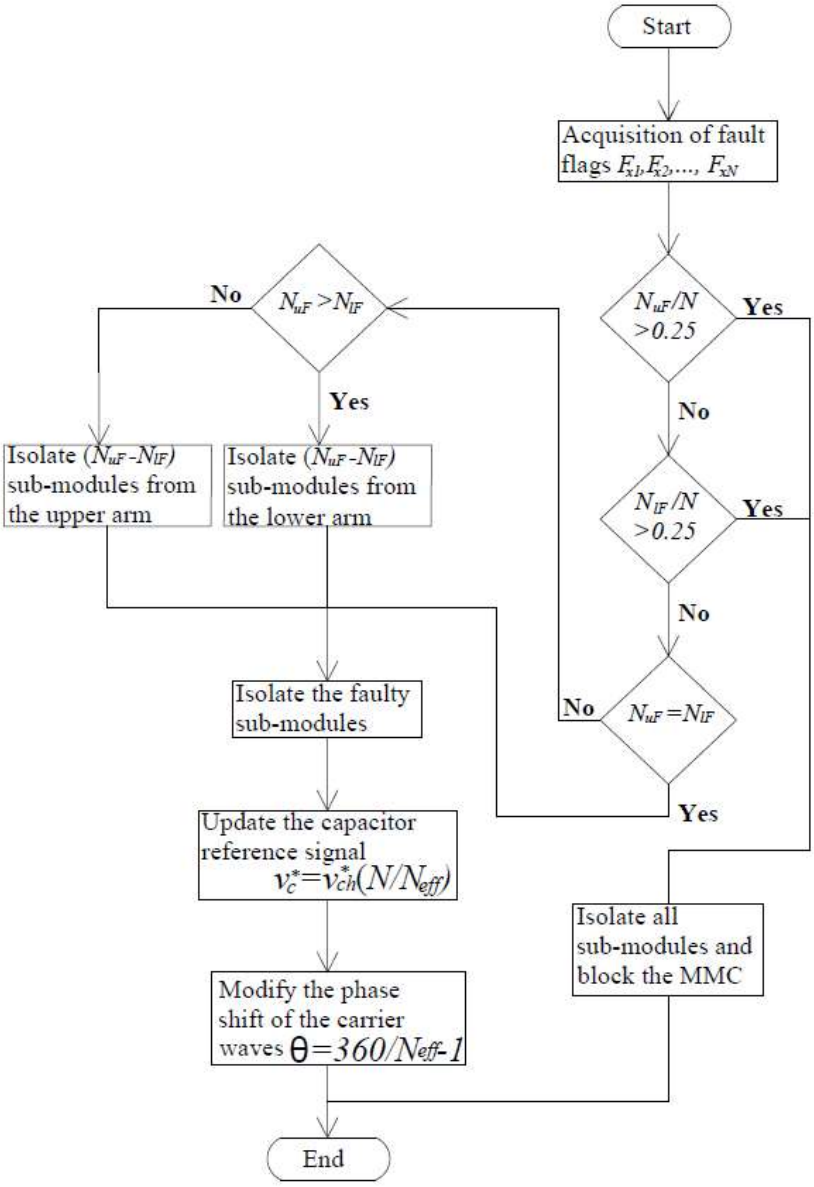


Figure 6.1: The proposed fault tolerant control algorithm.

It is important to mention that the threshold representing the percentage of failed submodules compared to the total number of arm submodules should be carefully selected according to the number of submodules per arm, the ratings of submodule components and the quality of the output power.

This strategy is designed to permit the converter to continue its operation, provided that the number of faulty submodules per arm does not reach a pre-defined value based on the number of submodules and the ratings of the devices. Otherwise, the control system considers the MMC to be suffering from cascading failure (which is selected to be 25% for the simulated MMC) and in this case, it isolates all submodules and deactivates the converter. The submodule capacitor must be carefully selected, taking into consideration the worst case condition at which the maximum number of faulty submodule can be tolerated. This can be done by calculating the maximum energy variation, the boosted capacitor voltage level and the allowable voltage ripples, and selecting the capacitor value so that it fits the capacitor selection rule presented in (2.32).

This strategy guarantees a stable performance for the MMC under internal abnormal operating conditions, without the need of any redundant components. Moreover, this technique can be applied to an MMC with more than 400 levels, as it is a software technique and can be implemented by simple instructions formed from the required sorting instructions.

Figure 6.2 illustrates a block diagram of the proposed integrated control system of the MMC, which achieves the capacitor voltage balancing technique presented in Chapter 4, the FDU proposed in Chapter 5 and the proposed FTCU presented here.

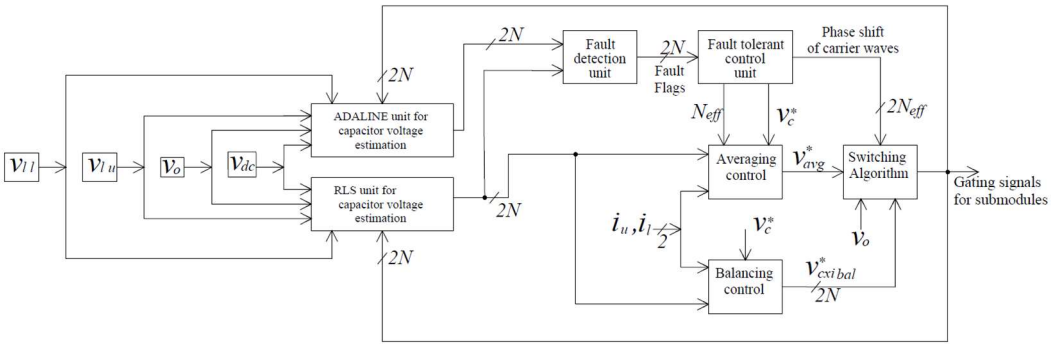


Figure 6.2: Block diagram of the proposed MMC control strategy.

It is apparent that the proposed scheme eliminates the need for significant numbers of voltage sensors for the submodule capacitors and their associated communication system with the central controllers. Consequently, the proposed strategy renders its application for a MMC system with a large number of submodules.

6.3 Reliability Assessment of the Proposed Fault Tolerant Control Technique

The main outcome of applying a fault tolerant control technique is to enhance the reliability of the entire system. For this purpose, the reliability of the MMC is assessed before and after the application of the proposed fault tolerant control technique, in order to address the amount of enhancement resulting from the proposed fault tolerant control algorithm.

6.3.1 MMC reliability definitions

A system failure can be represented by its probability to occur; this is performed considering the process behaviour as a random variable which receives its value from finite state space elements. To assess the reliability of the MMC, firstly the failure rate of the IGBT λ_0 should be assumed. The reliability function *R(t)* is the probability of success for the system, which is expressed as:

$$R(t) = 1 - F(t) \tag{6.5}$$

Where *F(t)* is the probability of system failure, which is complementary to the *R(t)*, and is given by:

$$F(t) = \int_0^t f(\tau)d\tau \tag{6.6}$$

Where *f(t)* is rate of change for the failure probability of a certain component, thus (6.6) can be rewritten as [109]:

$$f(t) = \frac{dF(t)}{dt} \tag{6.7}$$

Another important definition is the mean time to failure (MTTF), which gives an indication for the expected life time of a component that cannot be repaired or maintained. The MTTF is expressed as [109]:

$$MTTF = \int_0^\infty R(t)dt \tag{6.8}$$

6.3.2 Reliability calculations for MMC without fault tolerant control

For a system without fault tolerant control, the MMC will fail if one submodule suffers from a fault in either the upper or lower legs. To model the reliability of the converter in this case, a Markov chain is developed, as illustrated in Figure 6.3.

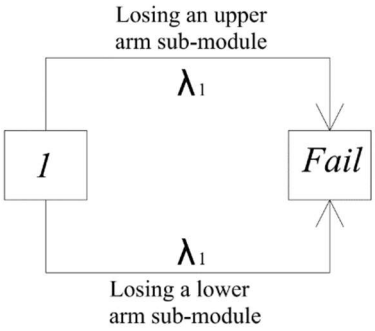


Figure 6.3: Markov chain for a modular multilevel converter without fault tolerant control.

In this case the failure rate for one submodule in a certain leg should equal:

$$\lambda_1 = (2N-1)\lambda_0 \tag{6.9}$$

Where λ_0 is the failure rate of each IGBT switch.

Based on the Markov chain, and from (6.9) substituting in (6.7), this gives:

$$\frac{dP_1}{dt} = -2\,\lambda_1\,P_1(t) \tag{6.10}$$

Solving the first order differential equation presented in (6.10), the reliability function can be expressed as:

$$R(t) = P_1(t) = e^{-2\,(2N-1)\lambda_0\,t} \tag{6.11}$$

From (6.11) substituting in (6.8), the mean time to failure is:

$$MTTF_{MMC\ without\ FTC} = \frac{1}{2\lambda_0}\left(\frac{1}{2N-1}\right) \tag{6.12}$$

6.3.3 Reliability calculations for MMC with the redundancy based fault tolerant control

In this case, the reliability of the MMC can be figured out from Figure 6.4 which has two failure rates. The first failure rate when losing one sub-module, λ_1. While the second failure rate, λ_2 indicates losing two sub-modules in the same leg.

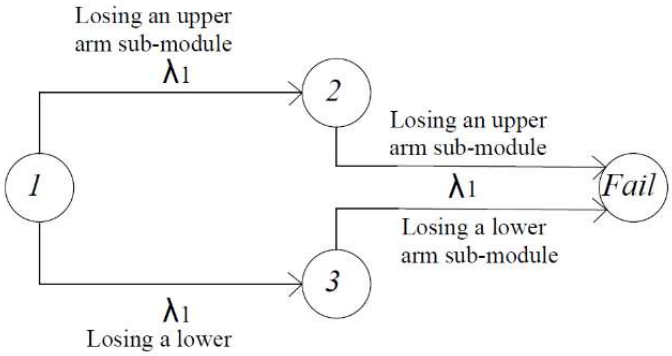


Fig. 6.4. Markov chain of the MMC with the classical redundancy based FTC technique.

In the sub-module redundant based FTC, each leg is assumed to be equipped with one redundant sub-module. Thus, the sub-module failure rates are given by:

$$\lambda_1 = (\frac{2N-1}{2} + 1)\lambda_0 \tag{6.13}$$

$$\lambda_2 = (\frac{2N-1}{2})\lambda_0 \tag{6.14}$$

Based on the Markov chain, the probability for the first state *P1* will remain the same, as presented in (6.7).

Following the same way, the failure probability of state 2 gives:

$$\frac{dP_1}{dt} = \lambda_1 P_1(t) - \lambda_2 P_2(t) \tag{6.15}$$

Solving (6.15) gives:

$$P_2(t) = (\frac{2N-1}{2})(e^{-\left(\frac{2N-1}{2}\right)\lambda_0 t} - e^{-\left(\frac{2N-1}{2}+1\right)\lambda_0 t}) \tag{6.16}$$

From (6.7) and (6.16), the probability of the fail state is the summation of $P_1(t)$ and $P_2(t)$:

$$R(t) = P_1(t) + P_2(t) = \left(\left(\frac{1-2N}{2}\right)e^{-\left(\frac{2N-1}{2}+1\right)\lambda_0 t}\right) + (\frac{2N-1}{2})(e^{-\left(\frac{2N-1}{2}\right)\lambda_0 t}) \tag{6.17}$$

From (6.17) substituting in (6.12), the MTTF is:

$$MTTF_{MMC\ with\ FTC\ 1} = \frac{1}{\lambda_0}\left(\frac{1-N}{N+1}\right) \tag{6.18}$$

6.3.4 Reliability calculations for MMC with the proposed fault tolerant control

The reliability of the MMC has a root change after the application of the proposed fault tolerant control, which is due to the ability of the MMC to work under

faults until reaching the cascading failure condition in one arm. To simplify the calculations and give a sense of the results, the reliability calculations are performed for the simulation model, which incorporates four submodules per arm, as previously presented (Table 4.1). In this particular case, the Markov reliability chain is developed as shown in Figure 6.5.

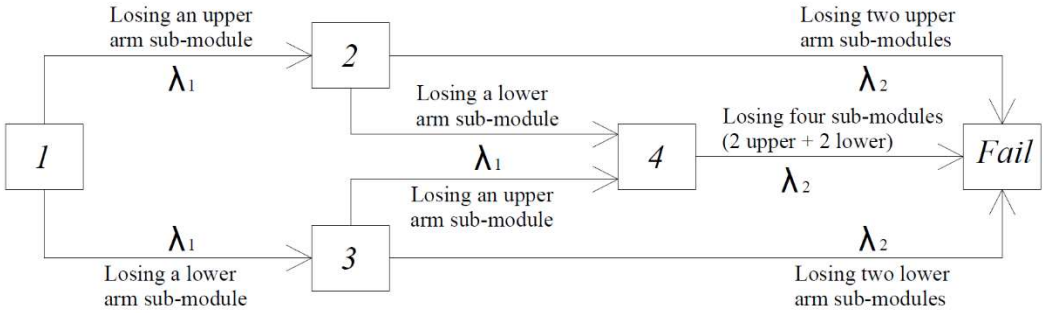


Figure 6.5: Markov chain for a five-level modular multilevel converter with the proposed fault tolerant control.

The Markov reliability chain shows that the MMC, with the proposed FTCU, has four possible finite states before reaching the failure state, instead of one as discussed in the previous section. The possible states are:

- State 1: The healthy state (no faulty submodules)
- State 2: Losing a submodule in the upper arm
- State 3: Losing a submodule in the lower arm
- State 4: Losing two submodules (one in the upper arm and one in the lower arm)
- Fail state: Losing two submodules in the upper arm or two submodules in the lower arm, or both

In this case, the two failure rates should be presented as λ_1 and λ_2. λ_1 is the failure rate of one submodule, and will be the same as calculated in (6.9). λ_2 is the failure rate for losing two submodules, and should equal:

$$\lambda_2 = (2N - 3)\lambda_0 \tag{6.19}$$

Based on the Markov chain, the probability for the first state *P1* will remain the same, as presented in (6.7). Regarding the probability of the second state *P2*, it can be expressed as follows:

$$\frac{dP_2}{dt} = -(\lambda_1 + \lambda_2)P_2(t) + \lambda_1 P_1(t) \tag{6.20}$$

The solution of the differential equation given in (6.20) gives:

$$P_2(t) = \frac{2N-3}{2}\left(e^{-(\lambda_1+\lambda_2)t} - e^{-2\lambda_1 t}\right) \quad (6.21)$$

$P_3(t)$ has the same probability of $P_2(t)$, since the conditions are the same. Moving to the forth state probability, this can also be emphasized from the Markov chain, as follows:

$$\frac{dP_4}{dt} = -(2\lambda_2)P_4(t) + \lambda_1 P_2(t) + \lambda_1 P_3(t) \quad (6.22)$$

The solution of this differential equation is expressed as:

$$P_4(t) = \frac{(2N-3)^2}{4}\left(e^{-2\lambda_1 t} + e^{-2\lambda_2 t}\right) - \frac{(2N-3)^2}{2}e^{-(\lambda_1+\lambda_2)t} \quad (6.23)$$

The reliability function *R(t)* is the summation of the four probabilities, as follows

$$R(t) = P_1(t) + P_2(t) + P_3(t) + P_4(t)$$

$$= \left((2N-2) + \frac{(N-3)^2}{4}\right)e^{-2\,(2N-1)\lambda_0\,t} + \left((2N-3) - \frac{(2N-3)^2}{4}\right)e^{-2(2N-2)\lambda_0\,t} + \left(\frac{(2N-3)^2}{4}\right)e^{-2(2N-3)\lambda_0\,t} \quad (6.24)$$

From (6.24), substituting in (6.8), the mean time to failure is:

$$MTTF_{MMC\ with\ FTC} = \frac{1}{2\lambda_0}\left(\frac{\left((2N-2)+\frac{(2N-3)^2}{4}\right)}{(2N-1)} + \frac{\left((2N-3)-\frac{(2N-3)^2}{4}\right)}{(2N-2)} + \frac{\left(\frac{(2N-3)^2}{4}\right)}{(2N-3)}\right) \quad (6.24)$$

To compare the reliability before and after the application of the proposed fault tolerant control, the reliability density functions presented in (6.11), (6.17) and (6.24) are plotted against time for a five-level MMC. The IGBT failure rate λ_0 is assumed to be $10^{-7}h^{-1}$, which is almost three years [110].

As shown in Figure 6.6, the reliability density function is considerably enhanced, which means that the rate of failure for the MMC is decreased.

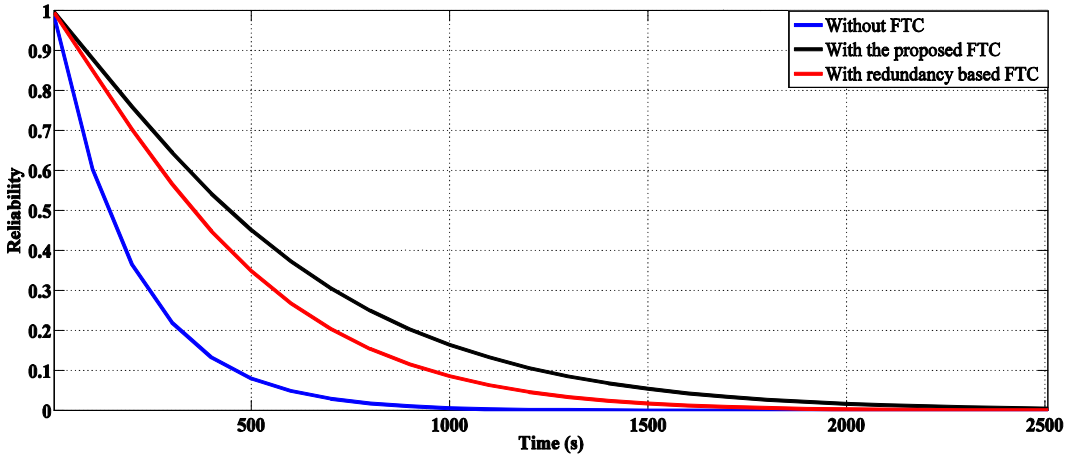


Figure 6.6: Plot of reliability density functions before and after the application of the proposed fault tolerant control.

This is also apparent when the MTTF is calculated, which gives 1615 days when applying the proposed fault tolerant control and 998 days when applying the redundancy based fault tolerant control compared to 82 days when the FTCU is deactivated.

6.4 Simulation Results

6.4.1 The FTCU performance under IGBT open circuit fault

This task is devoted to assessing the capabilities of the proposed control strategy, the FDU and the FTCU under an IGBT open circuit fault in a submodule. The upper switch of the third submodule in the upper arm of phase *a* is intentionally opened at $t= 0.5s$, while enabling the proposed FDU and FTCU. The FTCU isolates the faulty submodule, and the third submodule in the lower arm, to balance the energy between the two arms. Furthermore, the FTCU increases the v_c^* from 2.25 kV to 3 kV (Figure 6.7), and adjusts the phase shift of the carrier waves from 45º to 60º, in order to compensate for the loss of two isolated submodules. These actions are sufficient to tolerate the fault and restore the stability of the MMC control system, as apparent from the results seen in Figures 6.8 (a) and (b), where the three-phase output voltages and currents are balanced. The capacitor voltages of the remaining submodules restore their balance around the new desired value set by the FTCU, as indicated in Figure 6.9 (c). As expected, the capacitor voltages increase slightly at the moment of fault detection, t = 0.533s. It should be noted that the capacitor voltages of the isolated submodules freeze at their values when isolation occurs. Figures 6.10 and 6.11 demonstrate that the proposed RLS algorithm adequately estimates the capacitor voltages during the fault. The ADALINE and RLS algorithms provide the FDU and the FTCU with accurate data that result in precise performance during transient periods. With the help of the FTCU, the averaging and balancing control loops are able to quickly overcome the consequences of a fault, and forces the differential current to reach its rated value prior to the occurrence of the fault, as displayed in Figure 6.11 (a). Moreover, the averaging and balancing control signals retain their stability, as illustrated in Figures 6.11 (b) and (c), respectively.

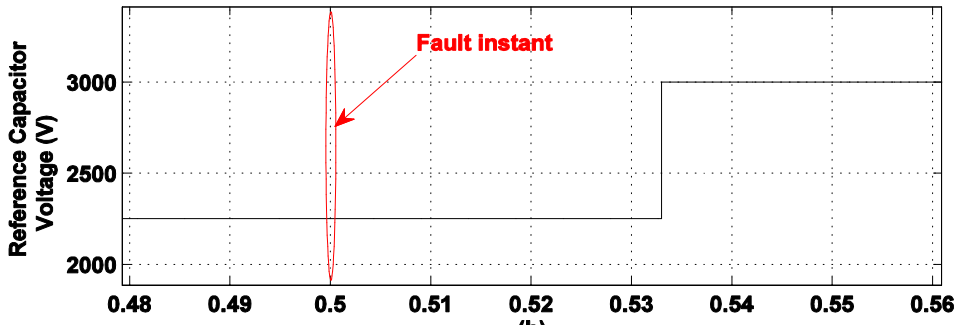


Figure 6.7: Dynamic performance of the proposed FTCU under an open-circuit fault in a submodule.

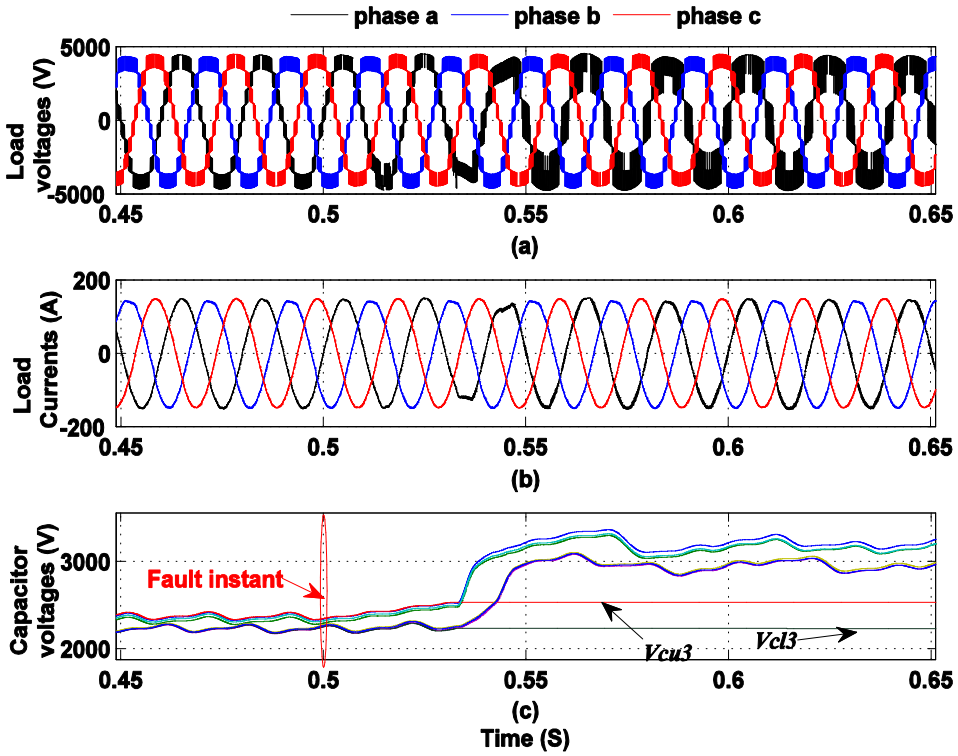


Figure 6.8: Enabling the proposed FTCU for an open-circuit fault: a) Three-phase voltages, b) three-phase load currents, c) voltages of leg a submodules.

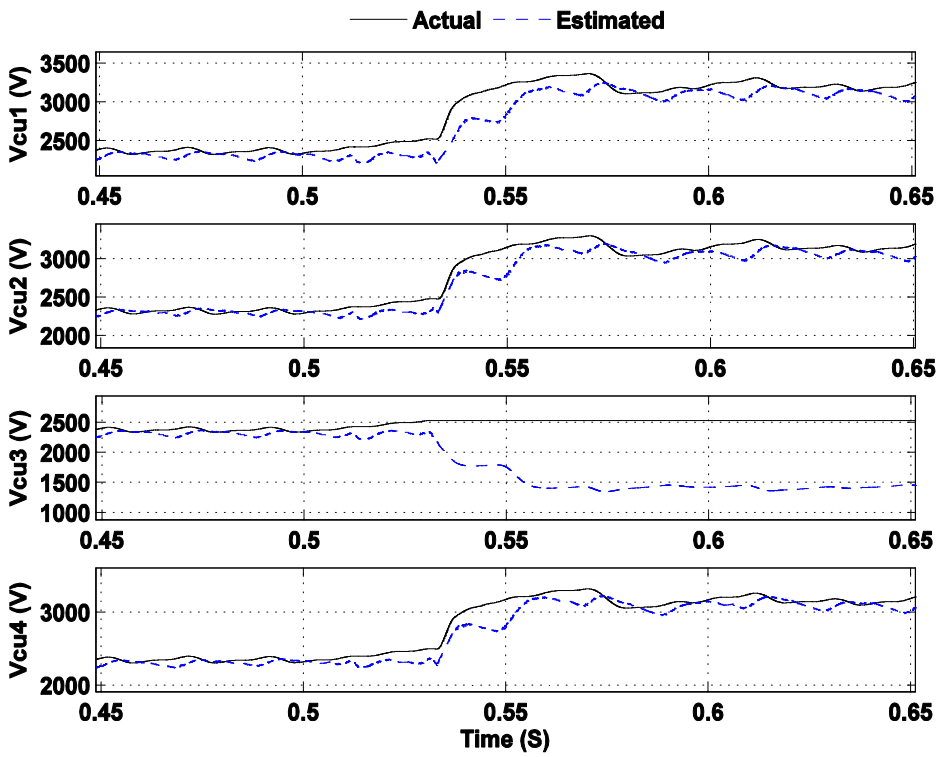


Figure 6.9: Actual and estimated voltages of the upper arm submodules of phase a, under an open-circuit fault while enabling the proposed FTCU.

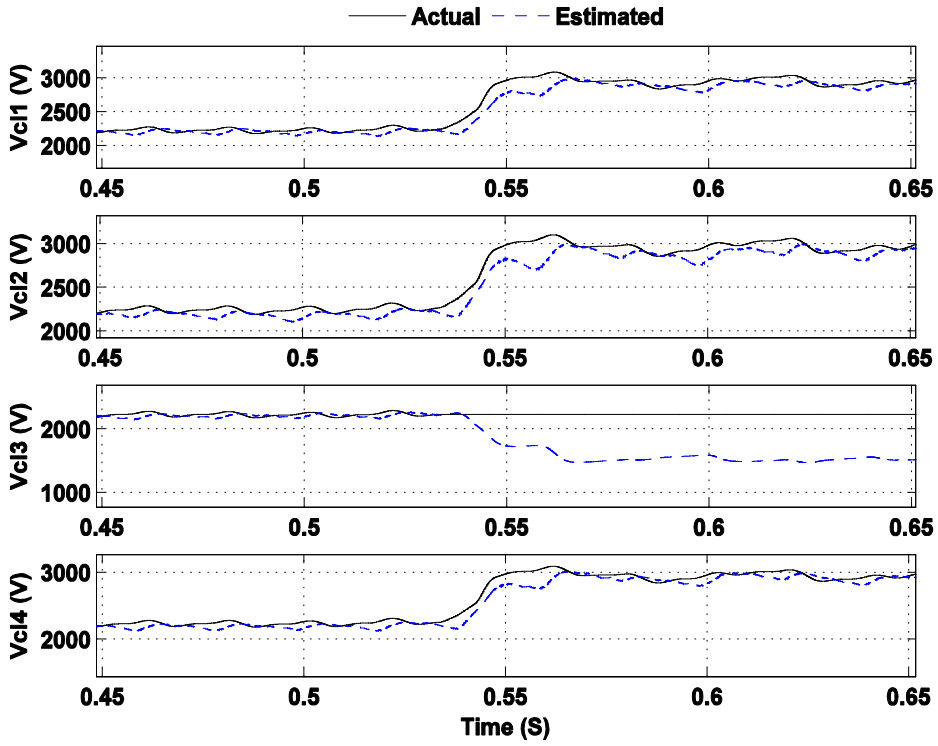


Figure 6.10: Actual and estimated voltages of the lower arm submodules of phase a, under an open-circuit fault while enabling the proposed FTCU.

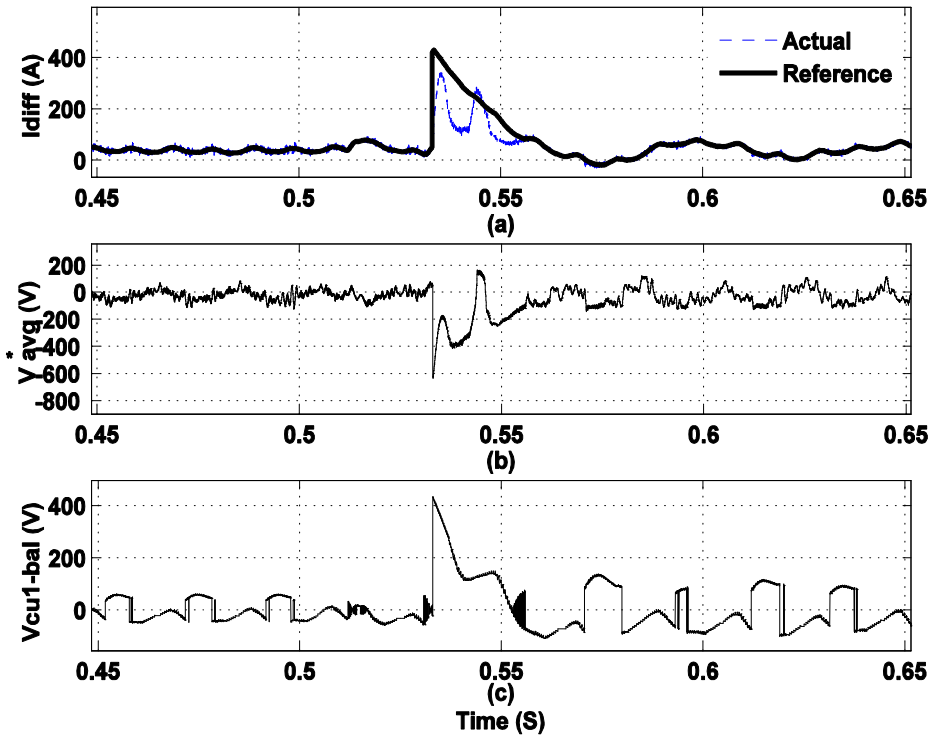


Figure 6.11: Action of the different controllers for leg a with enabling the FTCU for an open-circuit fault: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first submodule of the upper arm.

6.4.2 The FTCU Performance under IGBT short circuit fault

This case is conducted in order to investigate the capabilities of the proposed control strategy, the FDU and the FTCU under an IGBT short circuit fault in a submodule. A short-circuit fault is applied to the upper switch of the third submodule in the upper arm of phase *a* at *t= 0.5s*, while enabling the proposed FDU and FTCU. At the instant of fault detection, the FTCU isolates the faulty submodule in the upper arm, and its corresponding third submodule in the lower arm, in order to balance the energy between the two arms. Furthermore, the FTCU increases the v_c^* from 2.25 kV to 3 kV, as displayed in Figure 6.12, and modifies the phase shift of the carrier waves from 45º to 60º to compensate for the loss of two submodules. Figures 6.13 (a) and (b) show the three-phase output voltages and currents, which are balanced. The capacitor voltages of the remaining submodules restore their balance at the new set value, as illustrated in Figure 6.13 (c). The proposed RLS scheme accurately estimates the capacitor voltages during a short-circuit fault, as indicated in Figures

6.14 and 6.15. Figure 6.16(a) shows that the FTCU stabilizes the operation of the averaging and balancing control loops, which succeed in limiting the magnitude of the differential current, and tightly track its reference. Additionally, the improved averaging and balancing control signals are portrayed in Figures 6.16 (b) and (c), respectively.

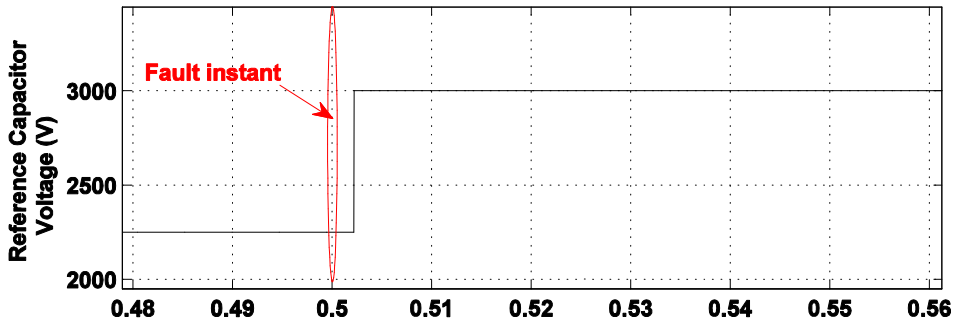


Figure 6.12: Dynamic performance of the proposed FTCU under a short-circuit fault in a submodule.

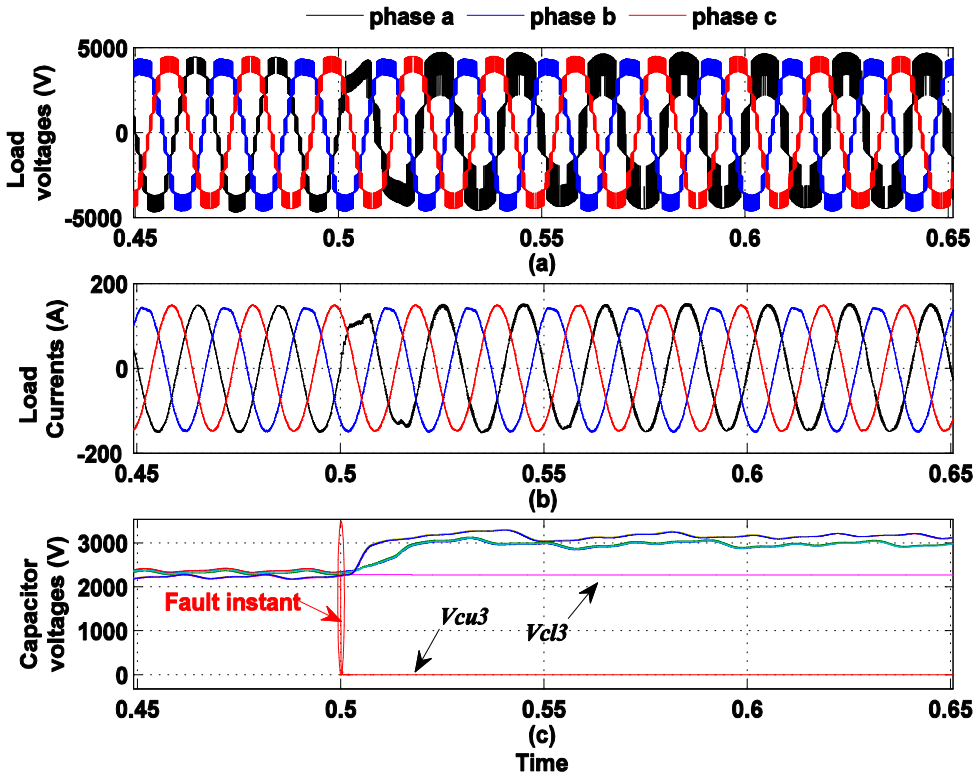


Figure 6.13: Enabling the proposed FTCU for a short-circuit fault: a) Three-phase voltages, b) three-phase load currents, c) voltages of leg a submodules.

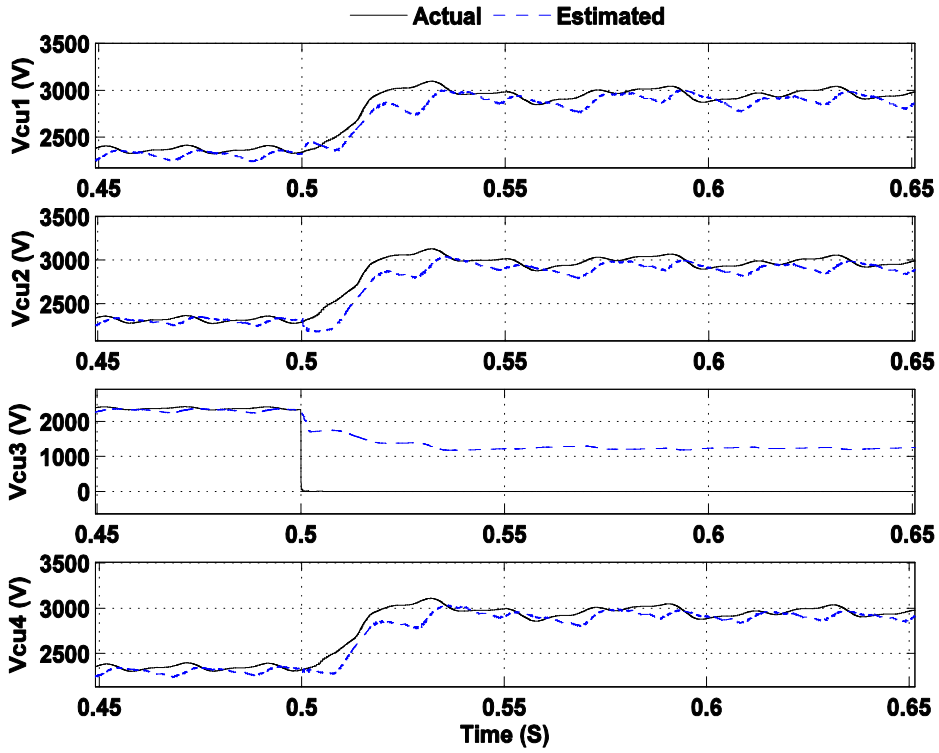


Figure 6.14: Actual and estimated voltages of the upper arm submodules of phase a, under a short-circuit fault.

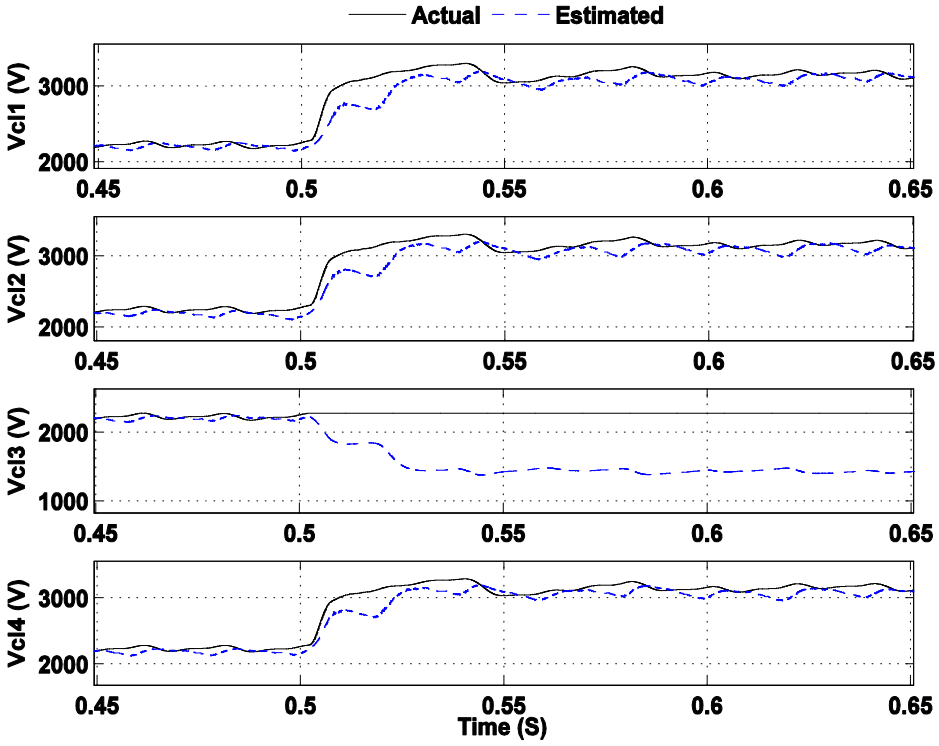


Figure 6.15: Actual and estimated voltages of the lower arm submodules of phase a, under a short-circuit fault.

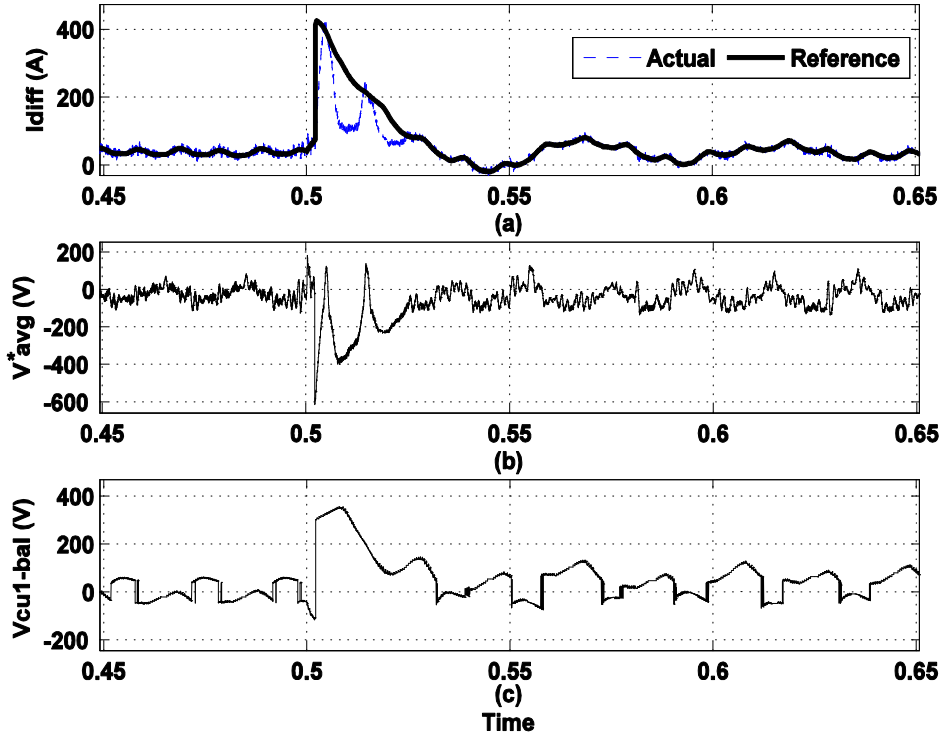


Figure 6.16: Action of the different controllers for leg a with enabling the FTCU for a short-circuit fault: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first submodule of the upper arm.

6.4.3 Performance of the FTCU under multiple faults

This case is devoted to investigating the capabilities of the proposed control strategy, the FDU and the FTCU under multiple IGBT faults in different submodules. Firstly, an open-circuit fault is applied to the upper switch of the third submodule in the upper arm of phase *a* at *t= 0.5s*. Then, at *t= 0.7s*, a short-circuit fault is applied to the second submodule in the lower arm of phase *a* while enabling the proposed FDU and FTCU. At the instant of the first fault detection, the FTCU isolates the faulty submodule in the upper arm, and its corresponding third submodule in the lower arm, to balance the energy between the two arms. Furthermore, the FTCU increases the v_c^* from 2.25 kV to 3 kV, and modifies the phase shift of the carrier waves from 45º to 60º, in order to compensate for the loss of two submodules. At the moment of detection of the second fault, the FTCU instantaneously isolates the second submodule in the lower arm of phase *a* which is faulty, and re-inserts the third submodule in the same arm which has been previously

bypassed as a response from the FTCU against the first fault, thus the energy between the two arms is always balanced. Figures 6.17 (a) and (b) show the three-phase output voltages and currents which are balanced during the entire period, and after the application of the two faults. The capacitor voltages of the remaining submodules restore their balance at the new set value, as illustrated in Figure 6.17(c). The proposed RLS scheme accurately estimates the capacitor voltages during the entire period, as indicated in Figures 6.18 and 6.19. Figure 6.20 (a) shows that the FTCU stabilizes the operation of the averaging and balancing control loops during the two faults, which succeeds in limiting the magnitude of the differential current and tightly tracking its reference. Additionally, the improved averaging and balancing control signals are portrayed in Figures 6.20 (b) and (c), respectively.

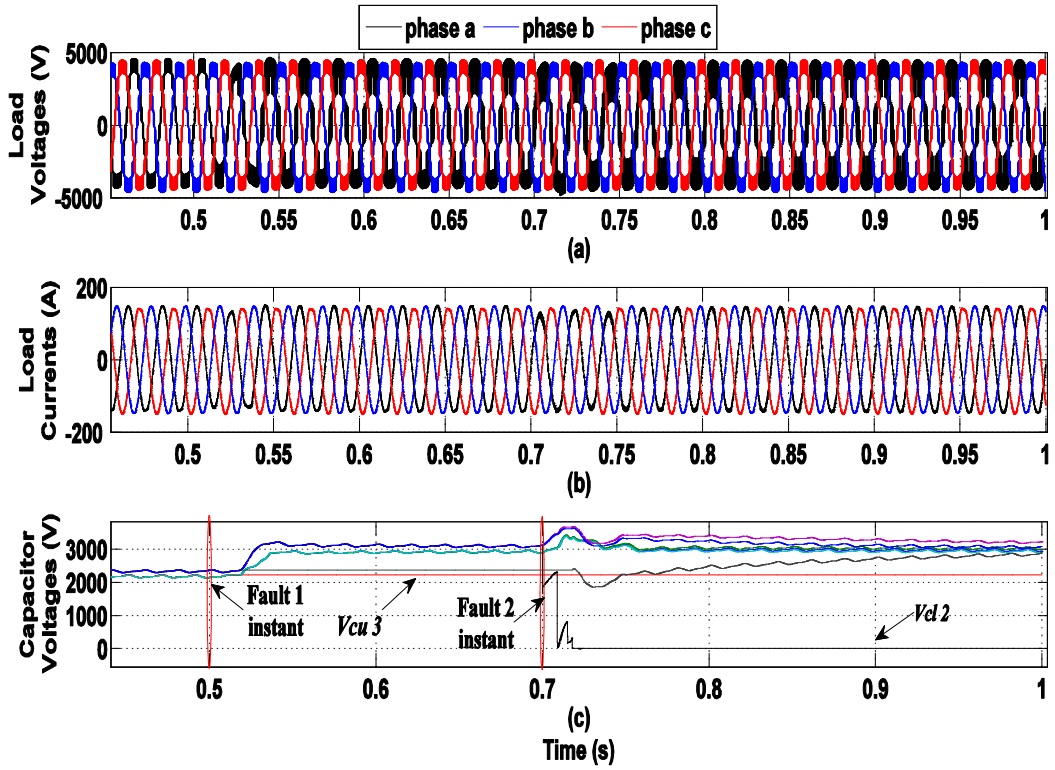


Figure 6.17: Enabling the proposed FTCU for multiple faults: a) Three-phase voltages, b) three-phase load currents, c) voltages of leg a submodules.

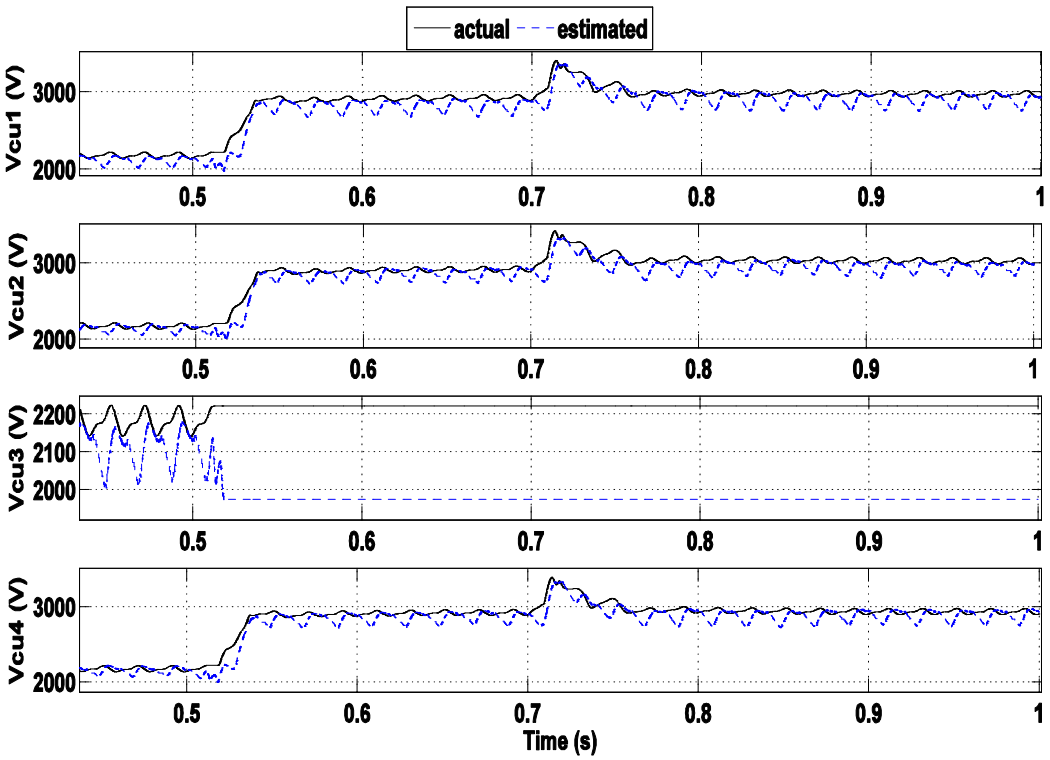


Figure 6.18: Actual and estimated voltages of the upper arm submodules of phase a, under multiple faults.

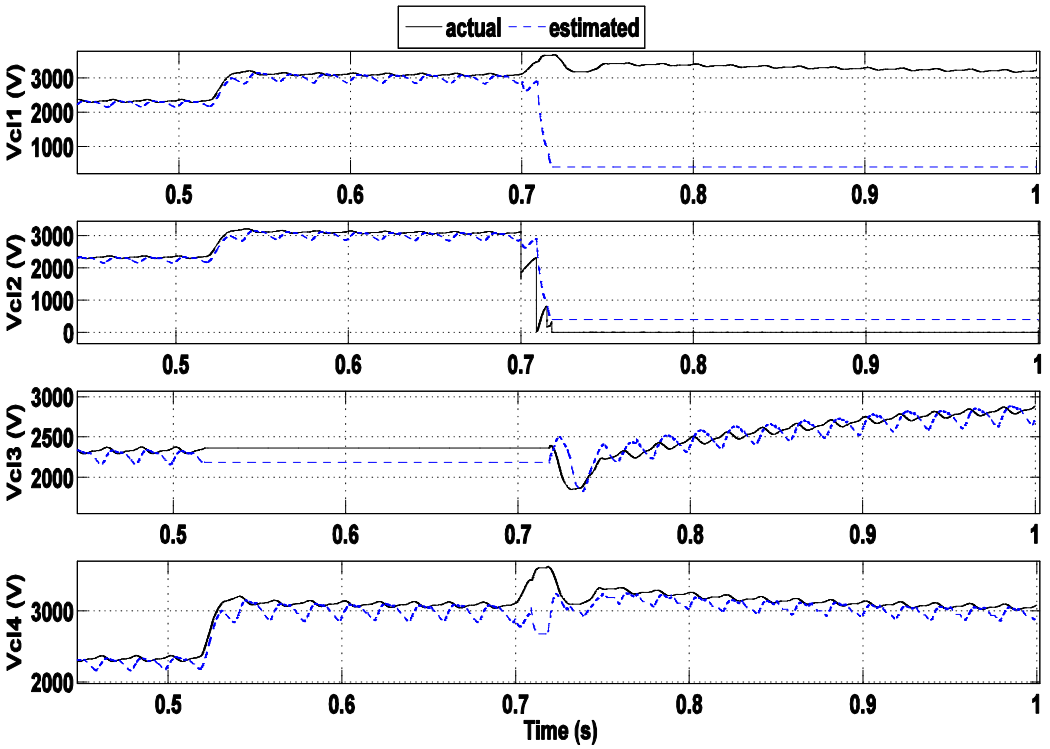


Figure 6.19: Actual and estimated voltages of the lower arm submodules of phase a, under multiple faults.

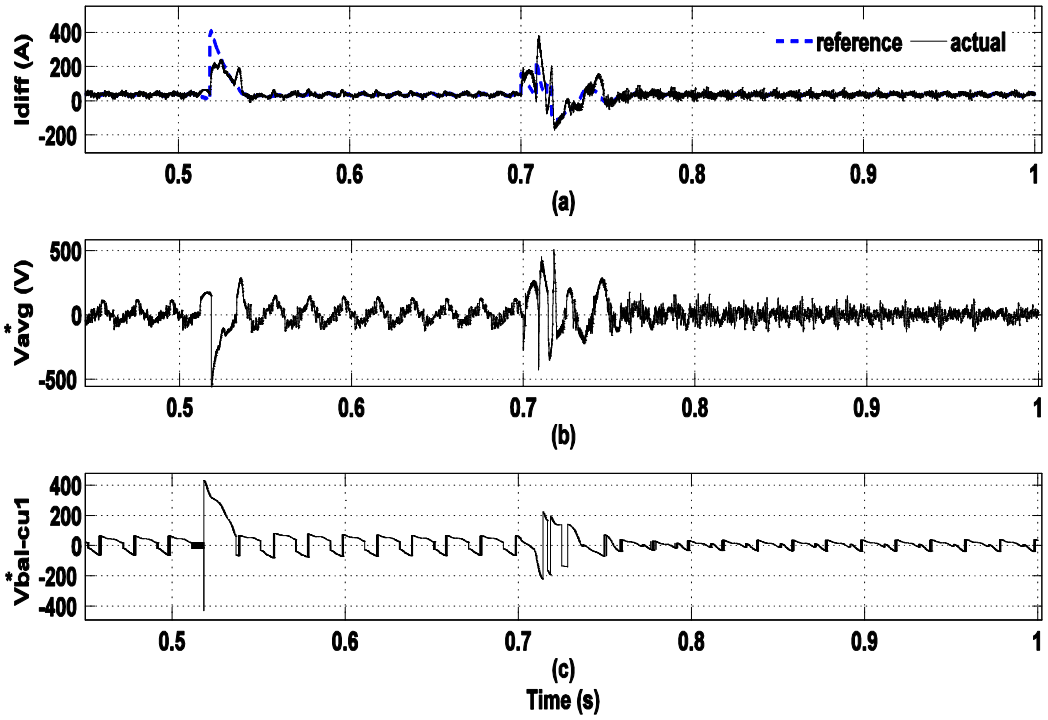


Figure 6.20: Action of the different controllers for leg a with enabling the FTCU for multiple faults: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first submodule of the upper arm.

6.4.4 Performance of the FTCU under cascading failures

This case is performed in order to investigate the capabilities of the proposed control strategy, the FDU and the FTCU under cascading failure. Firstly, an open-circuit fault is applied to the upper switch of the third submodule in the upper arm of phase *a* at *t= 0.5s*. Then, at *t= 0.55s*, another short-circuit fault is applied to the forth submodule in the same arm whilst enabling the proposed FDU and FTCU. At the instant of the first fault detection, the FTCU isolates the faulty submodule in the upper arm, and its corresponding third submodule in the lower arm, in order to balance the energy between the two arms. Furthermore, the FTCU increases the v_c^* from 2.25 kV to 3 kV, and modifies the phase shift of the carrier waves from 45º to 60º, in order to compensate for the loss of two submodules. At the moment of the second fault, the FTCU considers this condition as a cascading failure condition, since the percentage of faulty submodules to the total number of submodules in the upper arm of phase *a* is higher than 25%. As a result, the FTCU isolates all submodules in the three legs and blocks the converter. Figure 6.21 shows the

reference of capacitor voltages, which increased from 2.25 to 3 kV after the first fault, while after the second fault are decreased to 0 kV, in order to block the MMC. Figures 6.22 (a) and (b) show the three-phase output voltages and currents which are balanced after the application of the first fault, but after the second fault, the three phase voltages and currents progress towards zero. The capacitor voltages of the remaining submodules restore their balance at the new set value after the first fault, and then remain constant due to the isolation of the MMC, as a result of the second fault, as illustrated in Figure 6.22(c). The proposed RLS scheme accurately estimates the capacitor voltages until the application of the second fault, as indicated in Figures 6.23 and 6.24. Figure 6.25 (a) shows that the FTCU stabilizes the operation of the averaging and balancing control loops during the application of the first fault, which succeeds in limiting the magnitude of the differential current and tightly tracking its reference. Additionally, the improved averaging and balancing control signals are portrayed in Figures 6.25 (b) and (c), respectively. However, after the detection of the second fault, the output signals of the proposed controller are nulled, due to the MMC blocking order.

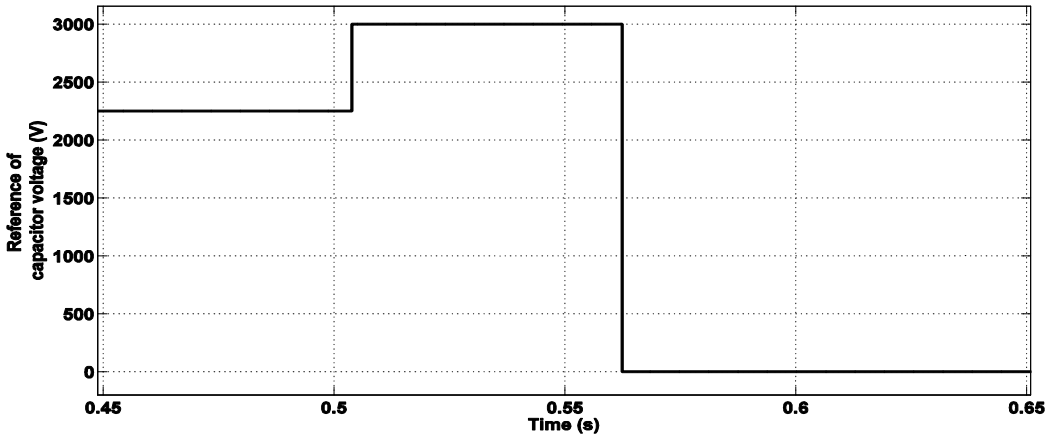


Figure 6.21: Dynamic performance of the proposed FTCU under cascading failure.

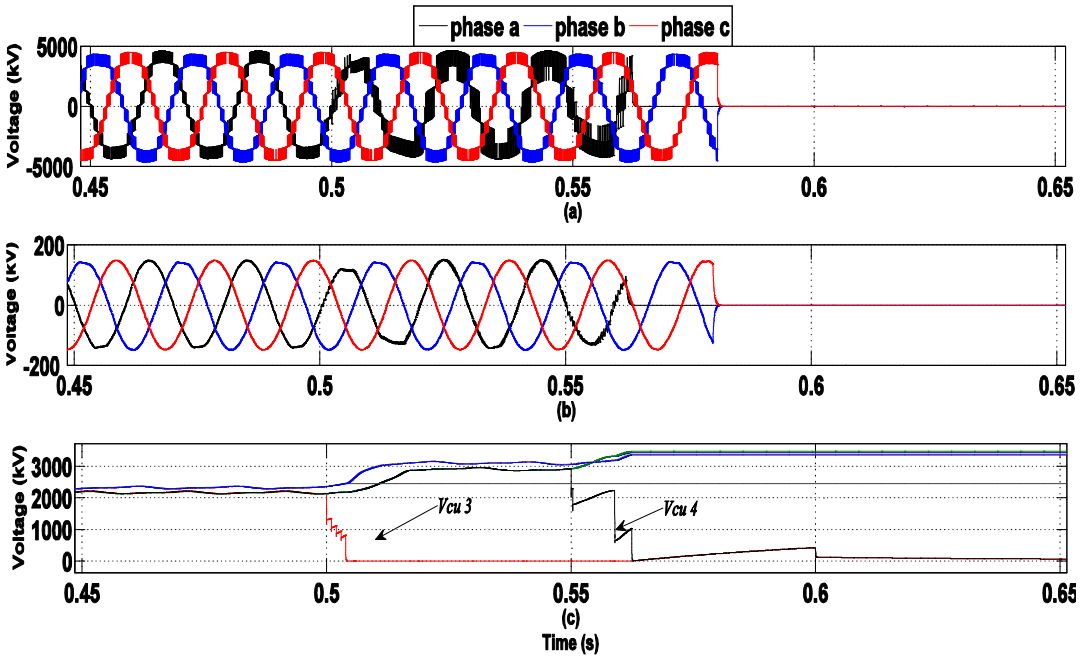


Figure 6.22: Enabling the proposed FTCU for cascading failures: a) Three-phase voltages, b) three-phase load currents, c) voltages of leg a submodules.

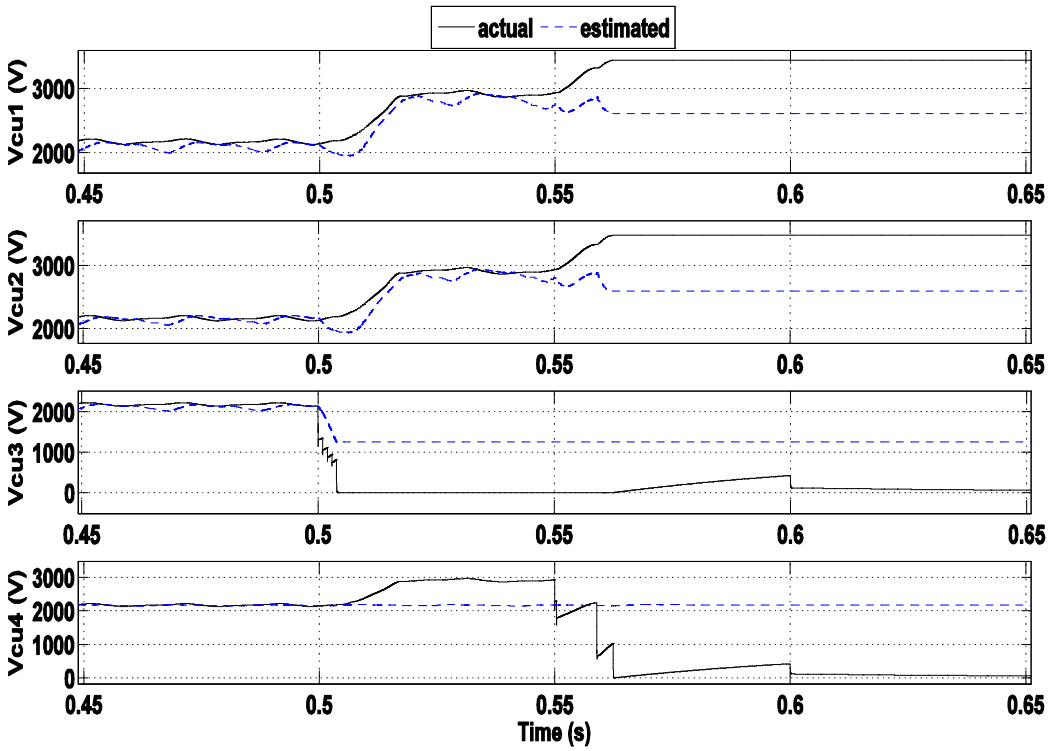


Figure 6.23: Actual and estimated voltages of the upper arm submodules of phase a, under cascading failures.

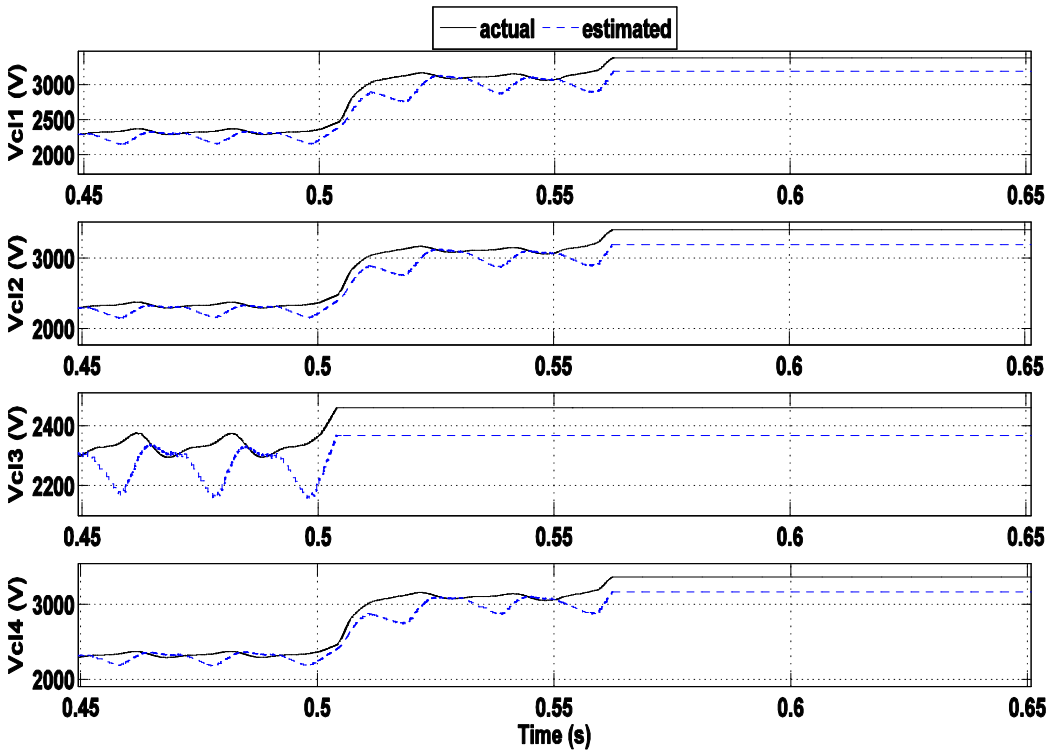


Figure 6.24: Actual and estimated voltages of the lower arm submodules of phase a, under cascading failures.

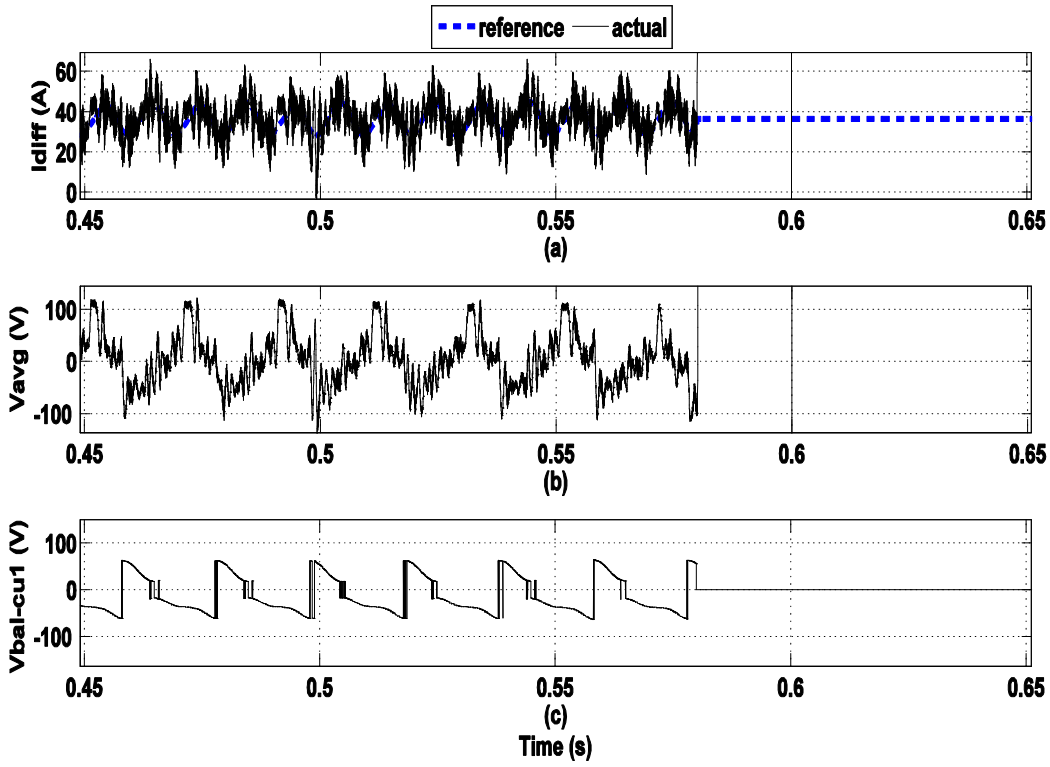


Figure 6.25: Action of the different controllers for leg a with enabling the FTCU for cascading failures: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first submodule of the upper arm.

6.5 Chapter summary

The chapter has presented a new fault tolerant control strategy for the MMC which is based on modifying the parameters of the capacitor voltage balancing technique presented in Chapter 4. The proposed method is integrated with the fault detection algorithm introduced in Chapter 5 to form a complete inner controller for the MMC. This action results in a significant reduction of the number of sensors and their associated wiring issues. Furthermore, the reliability enhancement of the MMC with the proposed FTCU is studied using Markov chains, and was significantly improved, which is reflected in an increased MTTF. Accurate performance of the proposed fault tolerant-based control strategy is revealed from the results presented and discussed in this chapter. In addition, these results prove that the proposed fault tolerant control strategy balances the capacitor voltages of the different SMs at a new set value, and limits the circulating current during SM faults.

Chapter 7

Validation of Proposed Techniques Using Hardware in The Loop Real-Time Simulations

7.1 Introduction

This chapter presents the validation of the proposed capacitor voltage balancing, fault detection and tolerant control techniques using a HIL simulation concept, in order to practically evaluate the performance of the proposed control. This is done by using a real-time digital simulator connected to a real-time field programmable gate array (FPGA) based physical controller. Firstly, the concept of HIL simulation systems is presented with focus on their advantages over offline simulations and experimental setups. Then, the platform of the HIL used for testing the proposed techniques is described, showing its main parts. A comparative study is also conducted, in order to illustrate the practical assessment of the proposed techniques when applied to a real MMC project with a large number of voltage levels. Finally, different case studies are applied to the HIL system, and their corresponding results are analysed and compared with those captured from the off-line PSCAD simulations.

7.2 HIL System Description

Although off-line simulations are accurate modelling techniques for power systems, they may suffer from various difficulties such as high computational time, particularly for an application such as MMC, which is composed of a large number of series connected submodules. Moreover, they cannot precisely illustrate the in-operation behaviour of real controllers under different operating conditions [111]. HIL simulations can be used as a suitable alternative for testing and prototyping newly developed control techniques that will be applied to power electronic devices. The HIL simulator is defined as a setup that emulates a system, by immersing faithful physical replicas of some of its subsystems within a closed-loop virtual simulation of the remaining subsystems[112]. This means that the basic task of the HIL simulator is to capture the bi-directional or closed loop interactions between a physical controller and the virtual simulation. As shown in Figure 7.1, the HIL simulation platform combines a real-time physical controller and a real-time digital simulator.

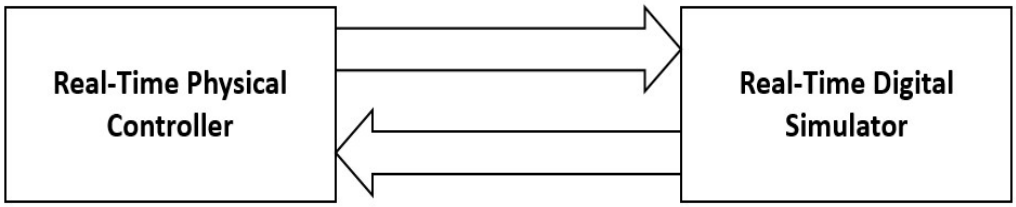


Figure 7.1: Structure of the HIL platform.

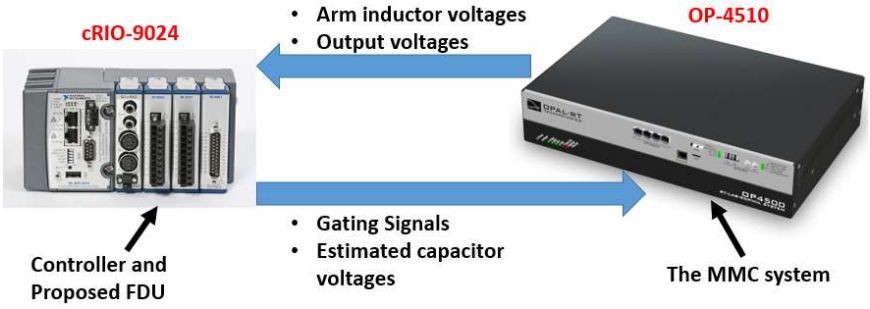
The main advantages of the HIL simulations can be summarized in the following points [113], [114]:

- Cost effective due to the reduced hardware when compared to experimental circuits
- Since it is a simulation-based system, rapid prototyping is available as it does not need hardware modifications
- The ability to run on a real-time basis due to its advanced computational structure
- HIL simulators are comprehensive and repeatable which means that they can be used in the testing of controllers that require a variety of operating conditions

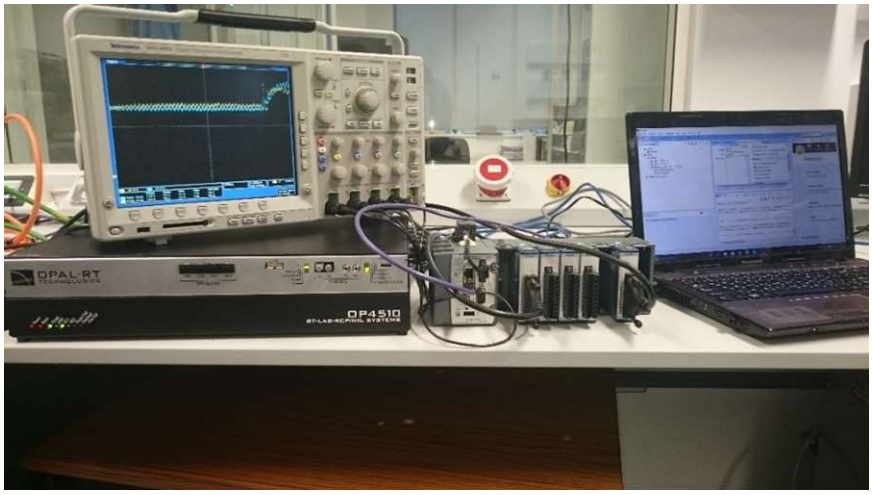
- Finally, its most two important features are non-destructiveness and safety, which is very important in the research since it depends on applying faults on the MMC

7.3 HIL System Implementation

The MMC system is simulated using the RT-LAB [111], and downloaded to the OP-4510 real time digital simulator [115], while the proposed MMC control technique and its associated capacitor voltage estimation units are programmed using the LAB-VIEW software [116], and uploaded to an FPGA physical controller type cRIO-9024 [117], as shown in Figure 7.2. Appendix C shows the details of the HIL simulations.



(a)



(b)

Figure 7.2: The HIL platform system components: a) the block diagram of the HIL platform, b) a snapshot of the HIL system.

The system parameters are identical to the PSCAD-simulated systems that are presented in Table 4.1. The following sub-sections illustrate each part of the platform.

7.3.1 The real-time physical controller

The real-time controller shown in Figure 7.3 is a cRIO system type 9024 reconfigurable controller made by National Instruments [117]. This controller contains an internal real-time process and FPGA controller type virtex 5 [118], which combines high speed calculations with the ability to deal with various types of physical signals. Moreover, it has 8 slots where different modules can be fitted, offering a wide range of analogue and digital cards that can be utilized for both signal acquisition and measurements.

Figure 7.3: The cRIO-9024 real-time controller.

The real-time controller is responsible for controlling the MMC in very small time steps (25 ns) by applying the proposed control technique and then generating the submodules' switching signals. As shown in Figure 7.4, the main advantage of using FPGA controllers over processor-based systems is the ability to implement the application logic in hardware circuits, instead of using a complex operating system, which saves a significant amount of time and enables it to be competitive for real-time control applications. It is programmed using LABVIEW, in order to demonstrate 4 control loops through which the controller performs its desired functions. The tasks of these loops are:

- Submodule capacitor voltage estimation techniques (ADALINE and RLS)
- The proposed capacitor voltage-balancing algorithm
- The submodule fault detection algorithm

To achieve these functions, the real-time controller must receive from the real-time digital simulator the output voltage and the arm voltages. Further, it should output the firing signals required for switching the MMC submodules.

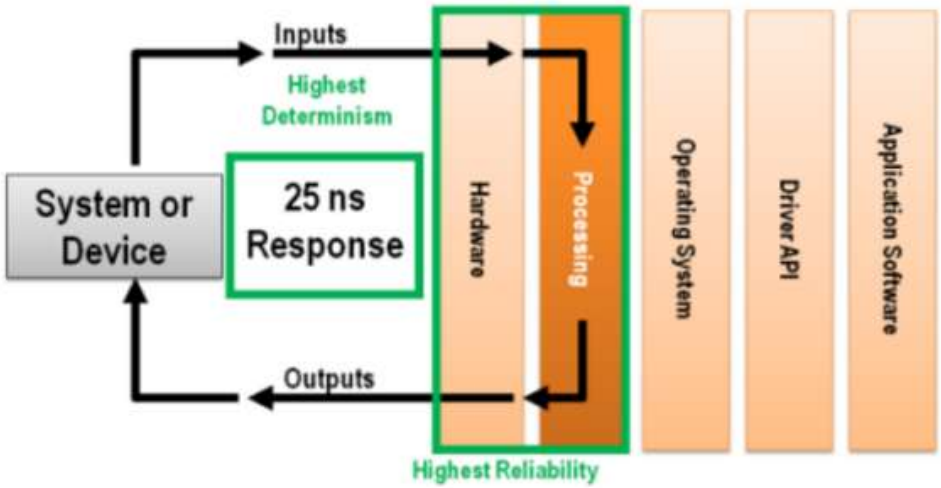


Figure 7.4. The application logic inside the FPGA-based controller [119], [120].

7.3.2 The real-time digital simulator

The real-time digital simulator used in the HIL platform is the OP4510, made by OPAL-RT (Figure 7.5).

Figure 7.5: The OP4510 real-time digital simulator.

It is responsible for simulating the MMC power system and exchanging data with the real-time controller through its hardware ports. As shown in Figure 7.6, the OP4510 consists of three main parts:

1. The KINTEX 7 FPGA carrier board is responsible for controlling the I/O ports, which enables the system to exchange signals with the physical controllers demonstrating different signal types.
2. The multi-core CPU, which builds the state space representation for the MMC system, and performs the real-time calculations that are necessary for system modelling

3. The Ethernet port, which connects the OP4510 with a host PC for the purpose of changing the system parameters

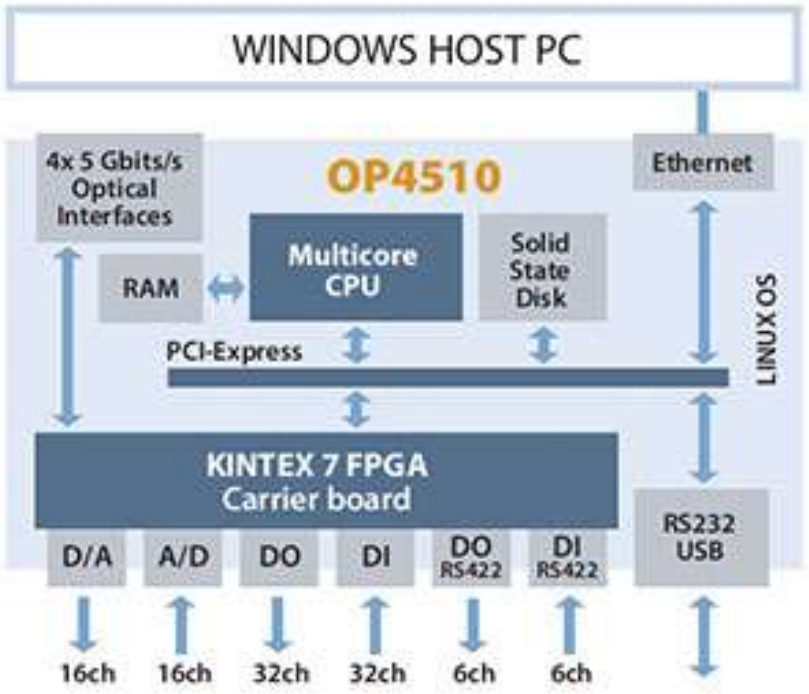


Figure 7.6: The OP4510 internal structure [115].

The OP4510 is programmed using the RT-LAB software package and MATLAB/SIMULINK [121]. The process starts with modelling the MMC and its attachments using SIMULINK, including the hardware signals that need to be inputted or outputted from the simulator. The RT-LAB is then responsible for synthesizing the system, building the bootable file which will be loaded into the simulator, and then running the real-time simulation. Looking inside the simulation, the real-time simulation model expects to receive the IGBT's firing signals from the cRIO controller while sending the arm inductor voltages and the AC output voltage. It is important to mention that the whole system is running at a very low time step (25 μs), which makes it convenient for real-time testing.

7.4 Practical Assessment of the Proposed Techniques

The main aim of building a HIL platform is an ability to assess any proposed control technique by determining whether it can be implemented industrially or not.

Also the use of HIL simulations ascertains the feasibility of any developed algorithms. Regarding the proposed techniques for MMC inner control, fault detection and tolerant control algorithms, the great challenge in implementing these control functions is the computational volume required, as all tasks depend on the estimation of the capacitor voltages for all submodules, which may total at least 800 per leg. If the computational burden is too high, a computer with a very large processor is required, and in this case the control technique would need code optimization and several reductions in the calculations. For this purpose, the computational burden of the simulated MMC is presented, and based on this a conception is shown for a real MMC project with 800 submodules per arm. The computational burden can be calculated by the number of logical resources consumed inside the FPGA. The building unit of an FPGA is the lookup table (LUT). As shown in Figure 7.7, a 4-input LUT is a small piece of RAM which is connected in the form of combinational logic to perform a specific function. The relationship between the 4 inputs and the outputs are simply a truth table, which is built through the synthesizing process.

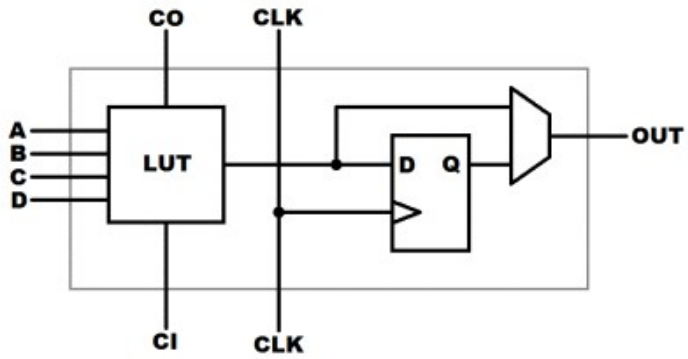


Figure 7.7: 4-way LUT.

The implementation of the proposed control on the cRIO virtex 5 based FPGA controller for controlling a MMC with 8 modules per arm consumed 19,872 LUTs, with the physical controller having an embedded FPGA system with a maximum number of 28800 LUTs, which means that only 70% of the FPGA's resources are utilized. This means that when selecting a controller for an MMC with 800 submodules per leg, applying the proposed control technique will require 1,987,200 LUTs. This can easily be achieved by using three FPGA controller type VIRTEX 7s, which have 2,000,000 LUTs inside their processing unit [119], [120]. Therefore, 99% of the logic capacity of the controller is utilized, which means that

the proposed control techniques can be implemented practically in terms of computational burden.

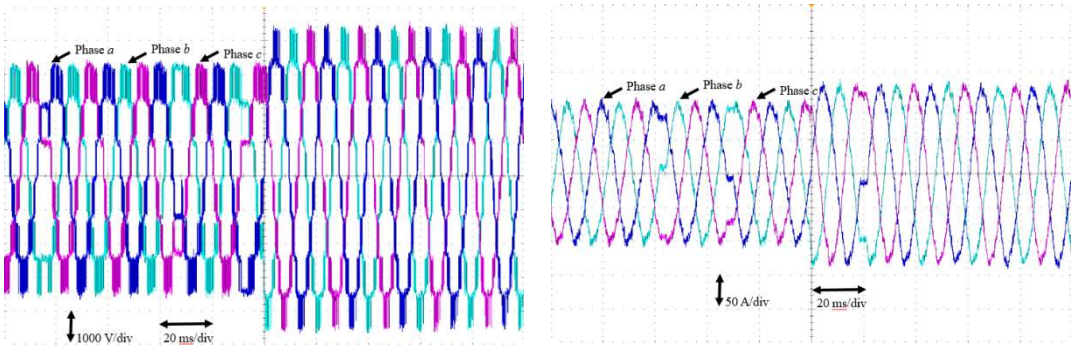
7.5 HIL Simulation Results

All case studies conducted using PSCAD simulations were repeated using HIL simulation, in order to examine the performance of the proposed techniques and compare the acquired results in both simulation systems.

7.5.1 Case 1: The performance of the proposed control under dynamic change of output voltage reference

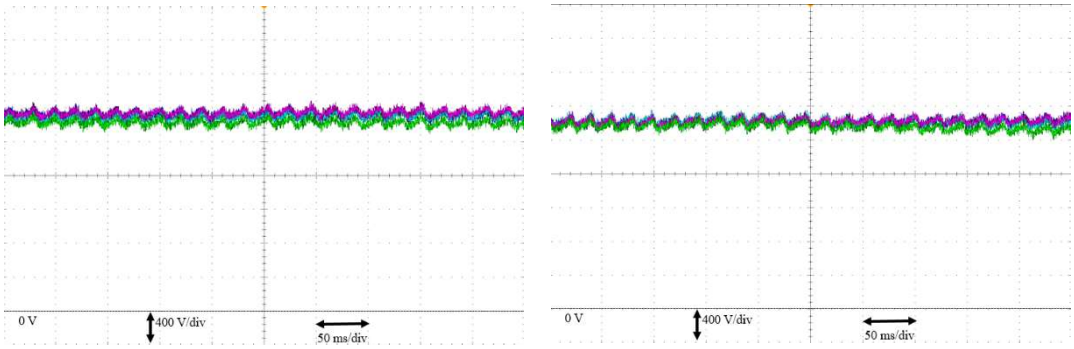
This case is identical to that presented in sub-section 4.4.1, and is dedicated to examining the performance of the proposed capacitor voltage estimation-based control algorithm for the MMC under the dynamic change of the reference phase voltage. The reference capacitor voltage v_c^* is set at v_{dc}/N = 2.25KV, while the reference phase voltage signal v_o^* is dynamically changed from 0.7pu to 1 pu.

The measured three-phase AC voltages follow their reference signals, as illustrated in Figure 7.8(a). Initially, when $v_o^* = 0.7$ pu, six submodules are utilized, and when $v_o^* = 1$ pu, all submodules are encompassed. Figure 7.8(b) displays the three-phase load currents. Figures 7.9(a) and 7.9(b) trace the capacitor voltages, which are grouped into two main trajectories, one for the upper arm and the other for the lower arm. The proposed MMC controller succeeds in balancing the capacitor voltages at their reference value of 2.25 KV. Moreover, Figure 7.10 (a) displays the estimated capacitor voltage of the first submodule, and compares it with its corresponding actual voltage. Fast tracking with accurate performance of the proposed scheme, based on the RLS algorithm for estimating submodule capacitor voltages, is evident. Furthermore, the circulating current tightly tracks its reference signal, as demonstrated in Figure 7.10(b). Figures 7.11(a) and 7.11(b) illustrate the actions of the averaging and balancing controllers for the first submodule at the upper arm $v_{cu1\ bal}^*$, respectively. These results reveal the efficient utilization of the proposed capacitor voltage estimation scheme for the control algorithm of the MMC.



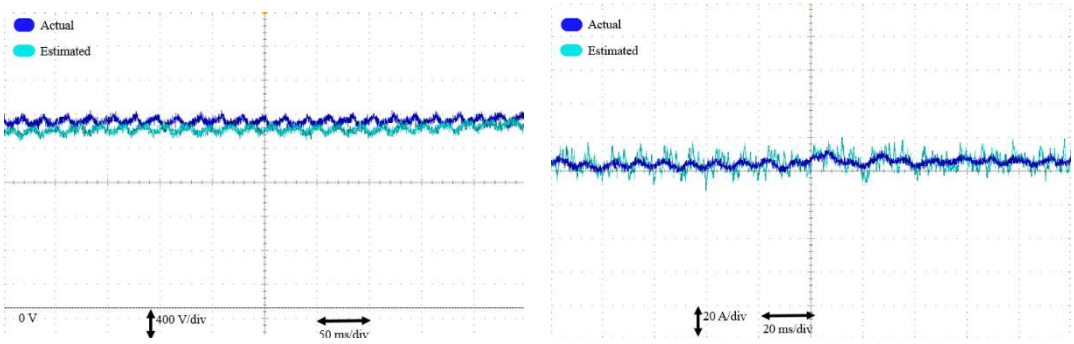
(a) (b)

Figure 7.8: Performance of the proposed inner controller under dynamic change of v_o^*: a) Three-phase voltages, b) three-phase load currents.



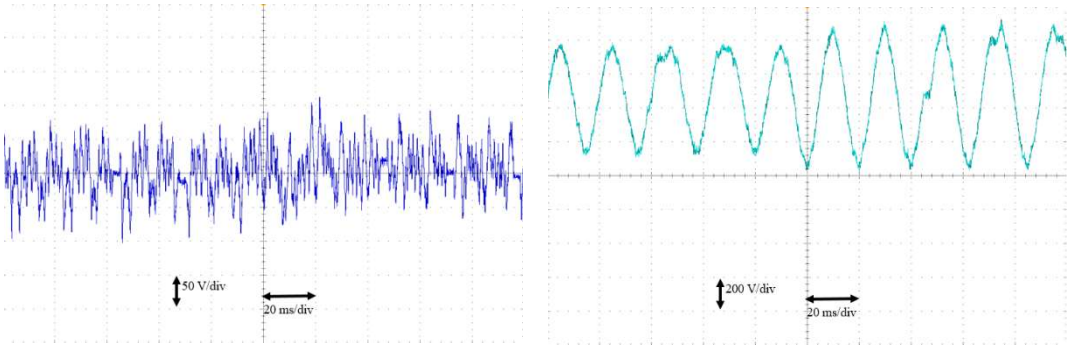
(a) (b)

Figure 7.9: Performance of the proposed inner controller under dynamic change of v_o^*: a) submodules voltages of upper arm in leg a, b) submodules voltages of lower arm in leg a.



(a) (b)

Figure 7.10: Action of the different controllers for leg a during dynamic change of v_o^*: a) Actual voltage of submodule 1 and its estimated signal, b) Actual and reference waveform of the circulating current.



(a) (b)

Figure 7.11: Action of the different controllers for leg a during dynamic change of v_o^*: a) averaging voltage reference, b) modulating signal for the first submodule of the upper arm.

7.5.2 Case 2: The performance of the proposed under IGBT open circuit fault

This case is similar to that presented in sub-section 6.4.1, with the lower IGBT of the third submodule being opened to resemble an open-circuit fault condition. The results are in contrast with PSCAD simulations. As shown in Figure 7.12, the proposed FDU successfully detected the fault after 35.6 ms, compared to 33 ms in off-line simulations. This increase in detection time is logical, as the physical controller runs at a definite clock frequency. The FTCU succeeds in restoring the stability of the MMC directly after the detection of the fault. This is performed by isolating the faulty submodule, and one healthy submodule, from the other arm to balance the energy. The reference signal of the capacitor voltage, v_c^*, is then increased from 2.25 to 3 kV, which compensates the lost energy of the faulty submodule. Moreover, the phase shift between carrier signals is increased from 45° to 60°. This appears in the three phase voltages and currents shown in Figures 7.13 (a) and (b), respectively, since they are free from DC components and distortion. Also, the capacitor voltages have their reference signals, v_c^*, tracked in a balanced manner over the entire test period, as illustrated in Figure 7.14. The RLS unit estimates all healthy capacitor voltages, with an average error significantly lower than 5%, as shown in Figure 7.15 (a). Regarding the estimation of the faulty submodule, the estimated signal contains large amounts of steady state error, which helps the FDU quickly detect the fault, as demonstrated in Figure 7.15 (b). The proposed capacitor voltage balancing succeeds in controlling the MMC during the

fault with the aid of the FTCU. This appears in the reduced value of the differential current, i_{diff}, which strictly tracks its reference signal, as given in Figure 7.16 (a). Moreover, the averaging and balancing control signals are stable over the entire period, with only minor fluctuations when the fault is initially generated, as indicated in Figures 7.16 (b) and (c).

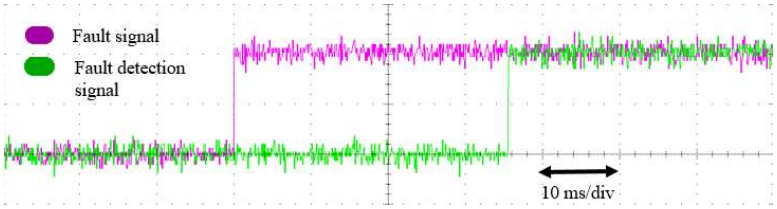
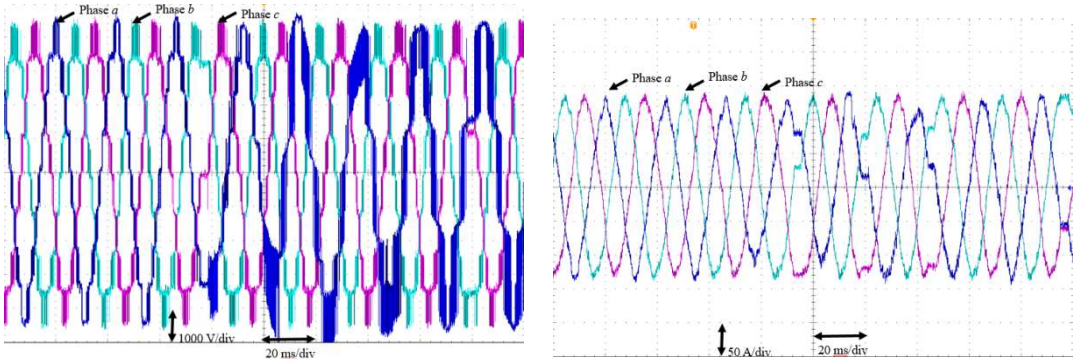
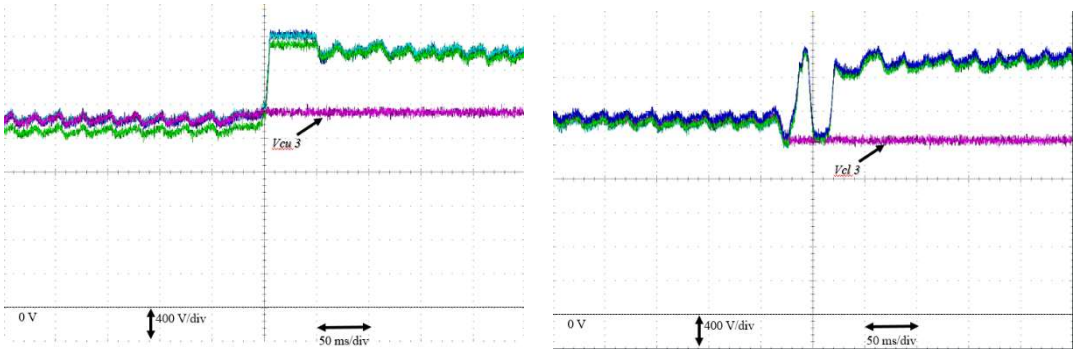


Figure 7.12: Dynamic performance of the proposed control under an open-circuit fault in a submodule.



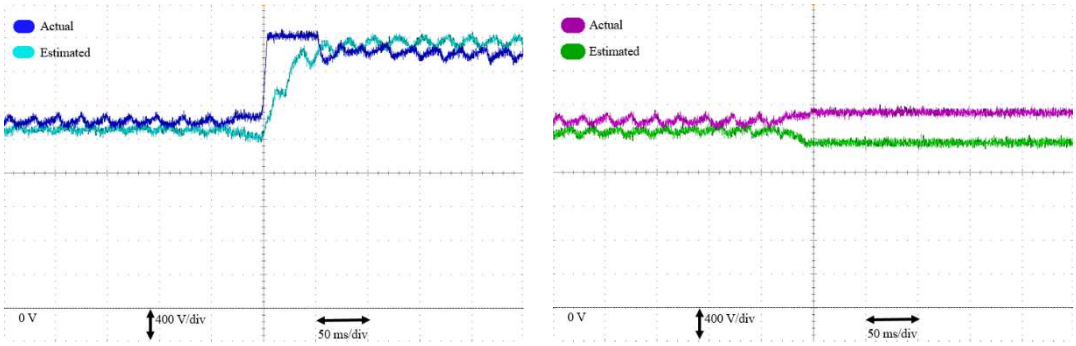
(a) (b)

Figure 7.13: Performance of the proposed control for an open-circuit fault: a) Three-phase voltages, b) three-phase load currents.



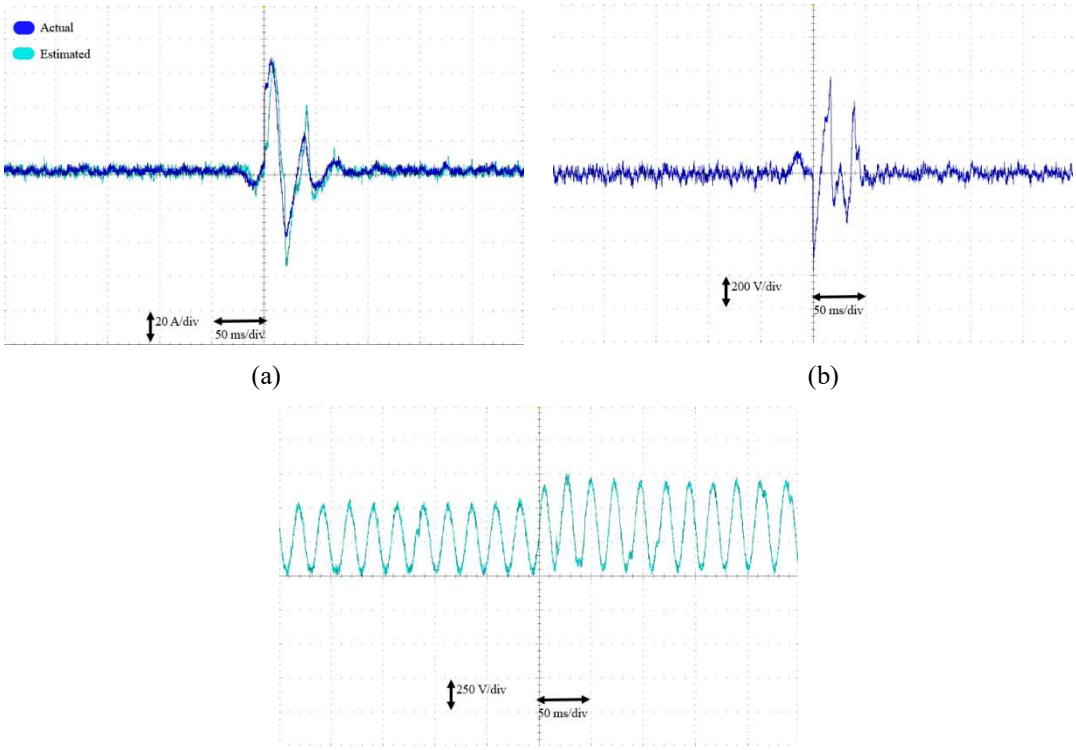
(a) (b)

Figure 7.14: Performance of the proposed control for an open-circuit fault: a) submodule voltages of upper arm in leg a, b) submodule voltages of lower arm in leg a.



(a) (b)

Figure 7.15: RLS-estimated signals in the upper arm of leg a under open-circuit fault: a) first submodule (healthy), b) third submodule (faulty).



(a) (b)

(c)

Figure 7.16: Action of the different controllers for leg a with enabling the proposed control for an open-circuit fault: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) modulating voltage reference for the first submodule of the upper arm.

7.5.3 Case 3: The performance of proposed control under IGBT short circuit fault

This case is similar to that presented in sub-section 6.4.2, with the lower IGBT of the third submodule being opened to resemble an open-circuit fault condition. The results are in contrast with PSCAD simulations. The FDU is able to detect the fault in less than 3.2 ms, which is higher that the PSCAD simulations by

only 1 ms, due to the real-time calculations of the FPGA controller, as demonstrated in Figure 7.17. After fault detection, the proposed FTCU performed the same actions mentioned in the previous case to maintain stability. These actions led to stable performance of the MMC before and after fault application. The quality of the output voltage and current was not affected, as shown in Figure 7.18. Moreover, the capacitor voltages of MMC submodules tracked their reference with only minor differences between each other, as illustrated in Figure 7.19. Again, the RLS estimation unit was able to accurately estimate capacitor voltages of all healthy MMCs with a very small amount of error. However, this was not the case for faulty submodules, as there was a considerable error between the RLS and ADALINE-estimated voltages, which assisted the FDU in its task. Figure 7.20 shows a sample for estimated voltages of one healthy submodule, and another one which is faulty. Furthermore, the proposed capacitor voltage balancing controller offers stable performance, which helps to reduce differential current, as given in Figure 7.21.

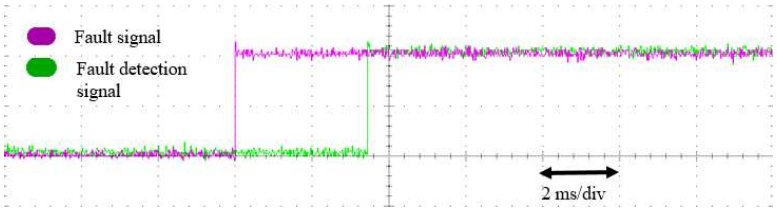


Figure 7.17: Dynamic performance of the proposed control under a short-circuit fault in a submodule.

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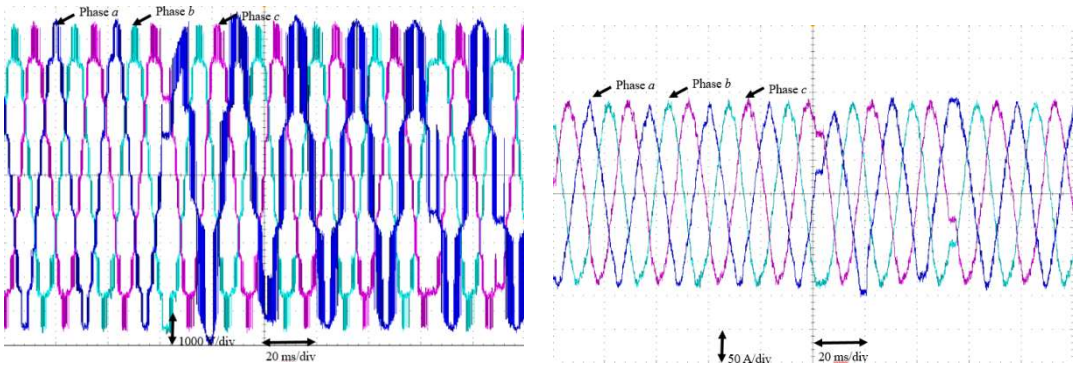
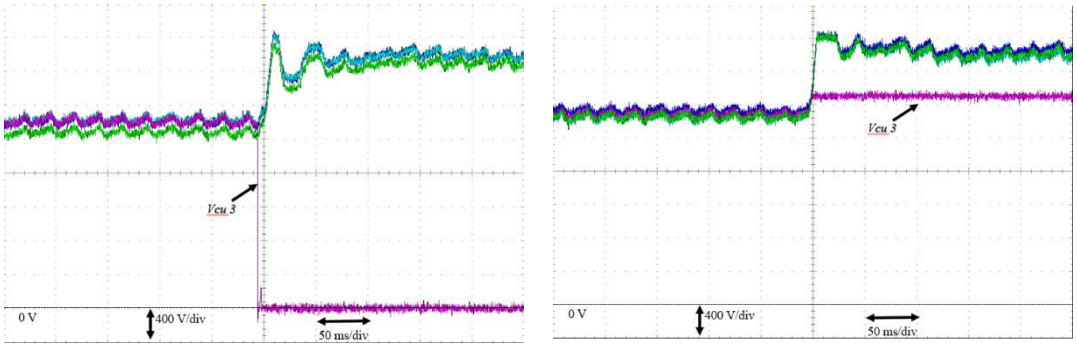


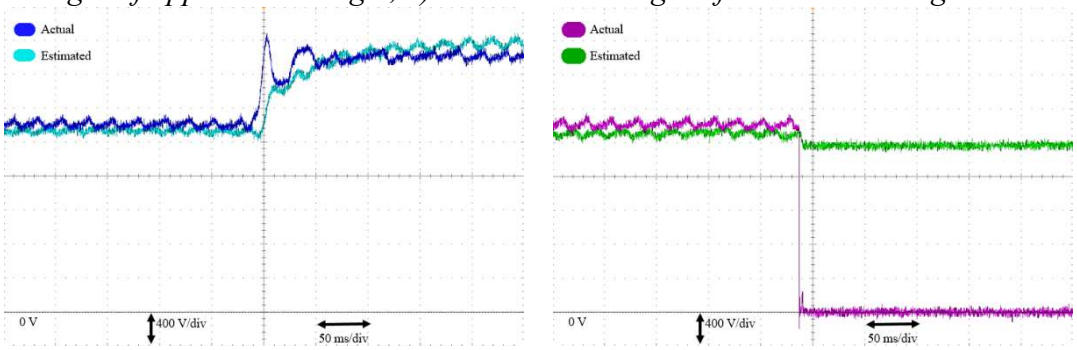
(a) (b)

Figure 7.18: Enabling the proposed control for a short-circuit fault: a) Three-phase voltages, b) three-phase load currents.



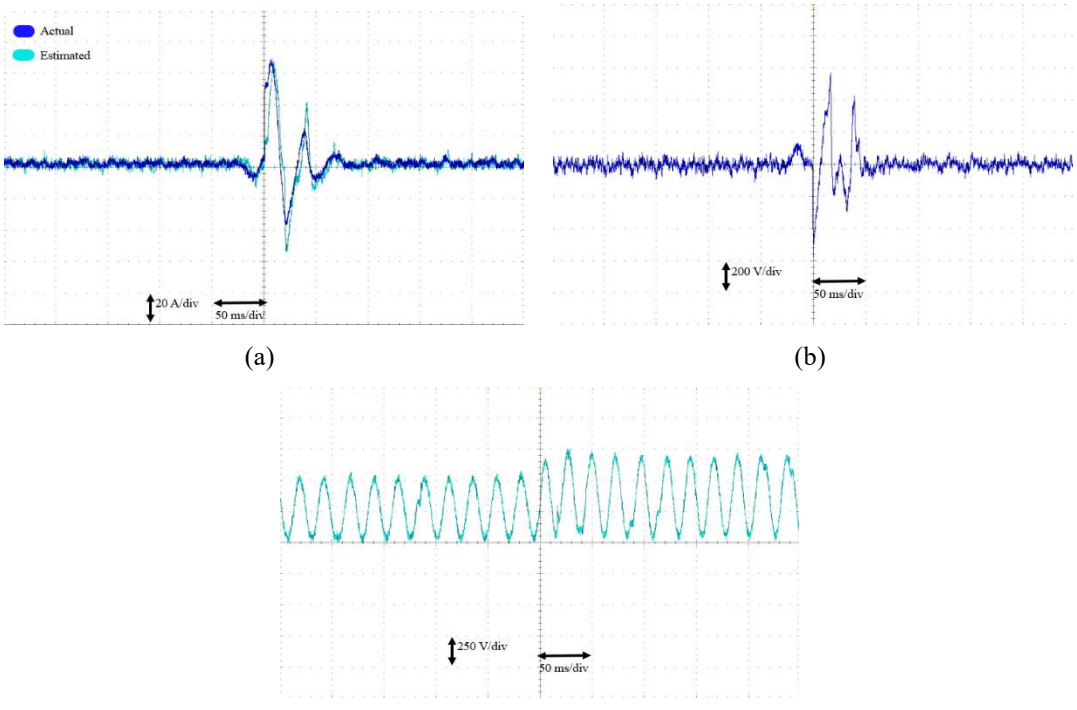
(a) (b)

Figure 7.19: Enabling the proposed control for a short-circuit fault: a) submodule voltages of upper arm in leg a, b) submodule voltages of lower arm in leg a.



(a) (b)

Figure 7.20. RLS-estimated signals in the upper arm of leg a under short circuit: a) first submodule (healthy), b) third submodule (faulty).



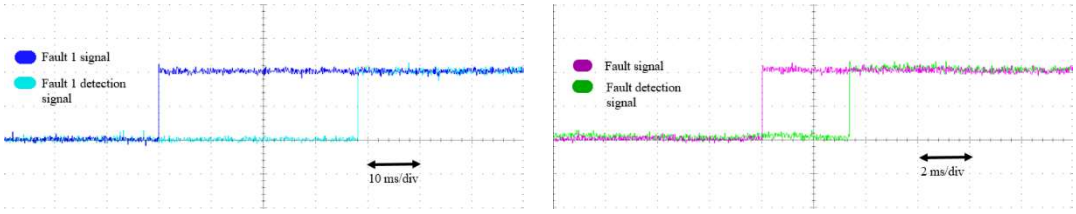
(a) (b)

(c)

Figure 7.21: Action of the different controllers for leg a with enabling the proposed control for a short-circuit fault: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) modulating voltage reference for the first submodule of the upper arm.

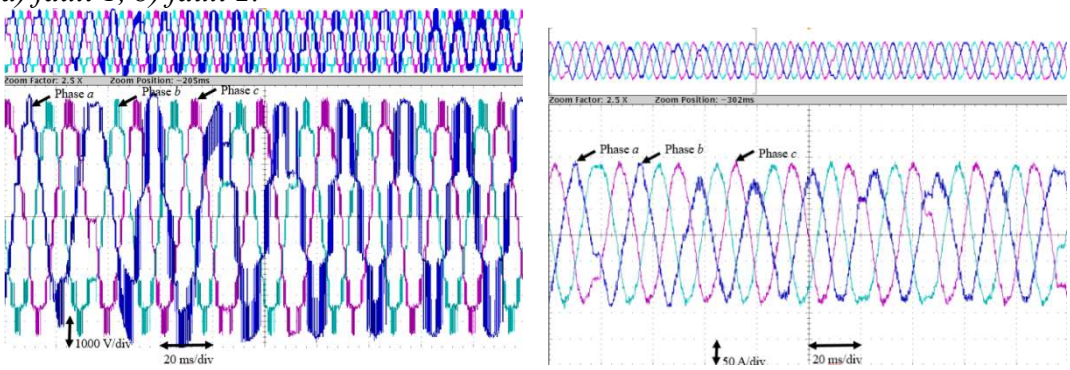
7.5.4 Case 4: The performance of the proposed control under multiple submodule faults

This case is identical to the PSCAD-offline simulated case presented in sub-section 6.4.3, and is devoted to studying the behaviour of the real-time physical behaviour of the proposed techniques in the case of having two faults. Firstly, an open-circuit fault is applied to the upper switch of the third submodule in. the upper arm of phase *a*, then after *0.3s* a short-circuit fault is applied to the first submodule in the lower arm of phase *a* while enabling the proposed FDU and FTCU. The FDU succeeds in detecting the first fault after 35.4 ms, as shown in Figure 7.22(a). Moreover, the FDU identifies the second fault after 3.2 ms, as shown in Figure 7.22 (b). The detection time of the two faults was similar to that in PSCAD-offline simulations, with very small deviation. Figures 7.23(a) and (b) portray the three-phase output voltages and currents, which are balanced even during the application of the two faults. The capacitor voltages of the remaining submodules of the upper and lower arms restore their balance at the new set value, as illustrated in Figures 7.24(a) and (b), respectively. Consequent to the detection of the first fault, the proposed FTCU isolates the faulty submodule in the upper arm, and its corresponding third submodule in the lower arm, in order to balance the energy between the two arms. Furthermore, the FTCU increases v_c^* from 2.25 kV to 3 kV, in order to compensate for the loss of two submodules. After the second fault is identified, the FTCU isolates the first submodule in the lower arm of phase *a*, which is faulty, and re-inserts the third submodule in the same arm, which is previously bypassed as a response from the FTCU against the first fault. Hence, the energy between the two arms is always balanced, and the capacitor voltages of the remaining submodules are regulated at the new set value, 3KV. The proposed RLS scheme accurately estimates the capacitor voltages during different operating conditions, as indicated in Figure 7.25(a). Figure 7.25(b) demonstrates that the FTCU succeeds in limiting the magnitude of the differential current, which tightly tracks its reference signal. Finally, the averaging and output voltage reference control signals are portrayed in Figures 7.26 (c) and (d), respectively. It is apparent that the proposed FTCU stabilizes the operation of the control loops during different types of faults. The results illustrate the satisfactory behaviour of the proposed control technique under different types of switch faults.



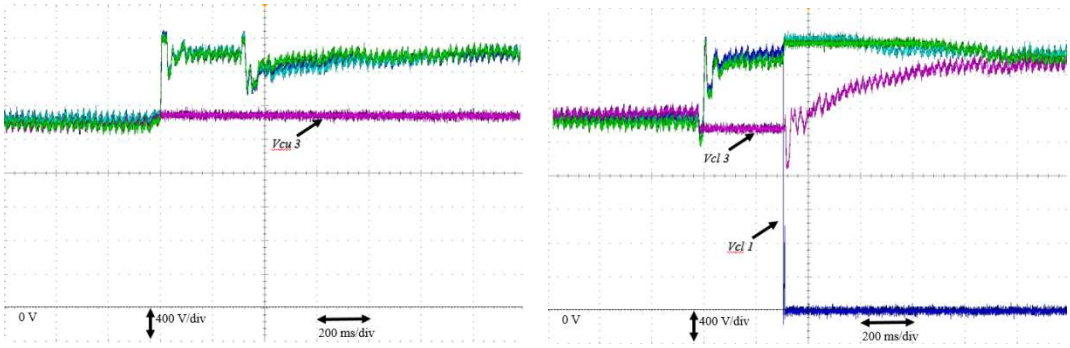
(a) (b)

Figure 7.22: Dynamic performance of the proposed control under multiple faults: a) fault 1, b) fault 2.



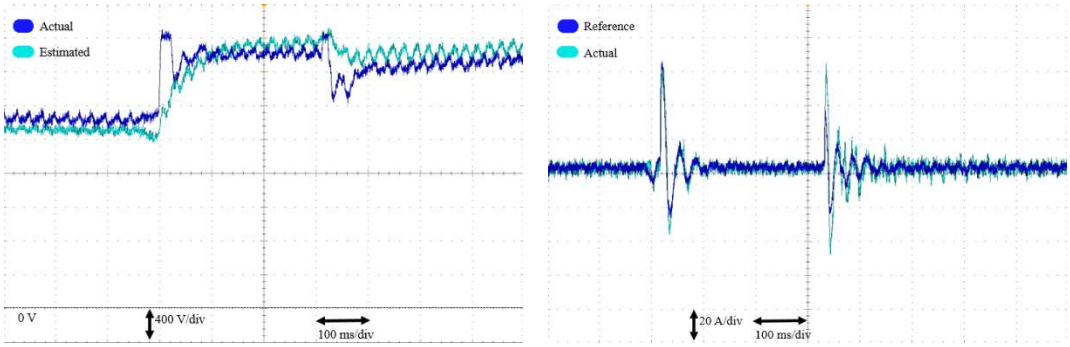
(a) (b)

Figure 7.23: The performance of the proposed control under multiple faults: a) Three-phase voltages, b) three-phase load currents.



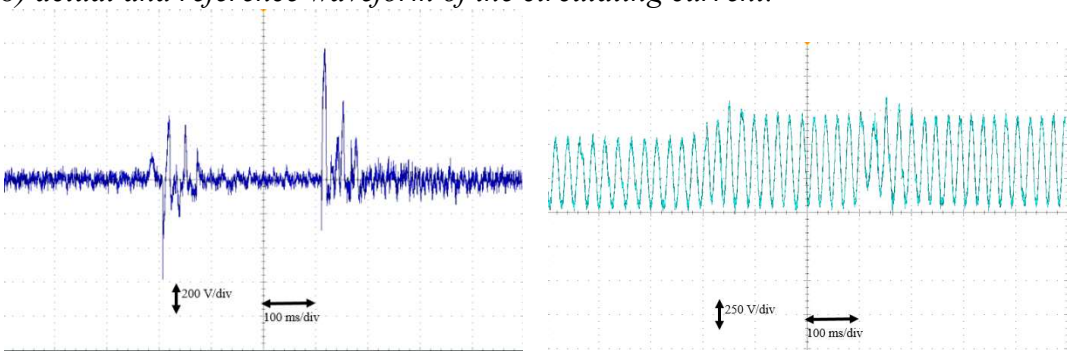
(a) (b)

Figure 7.24: The performance of the proposed control under multiple faults: a) submodule voltages of upper arm in leg a, b) submodule voltages of lower arm in leg a.



(a) (b)

Figure 7.25: Action of the different controllers for leg a with enabling the proposed control for multiple failure: a) The capacitor voltage estimation of submodule Vcu1, b) actual and reference waveform of the circulating current.



(a) (b)

Figure 7.26: Action of the different controllers for leg a with enabling the proposed control for multiple failure: a) averaging voltage reference, b) modulating voltage reference for the first submodule of the upper arm.

7.5.5 Case 5: The performance of the proposed control under cascading failures

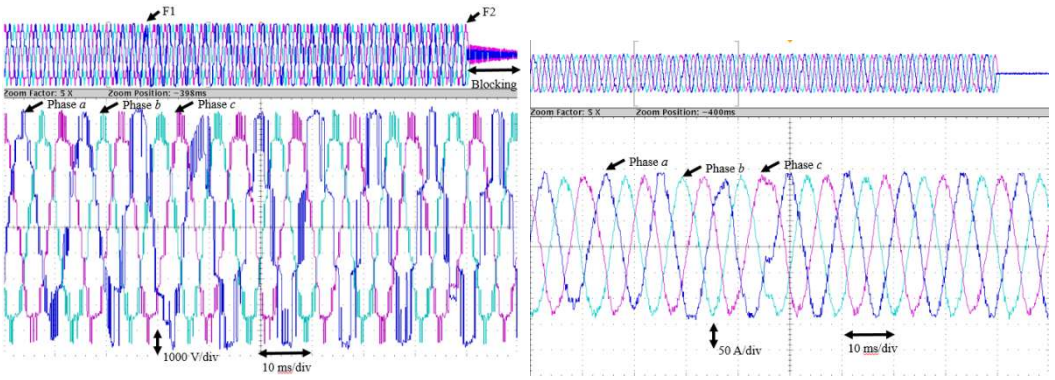
This case is identical to that presented in sub-section 6.4.4 under PSCAD-offline simulations for examining the real-time performance under cascading failures. A scenario of cascading failure is considered in this case study, in order to investigate the capabilities of the proposed control strategy. Firstly, an open-circuit fault is applied to the upper switch of the third SM in the upper arm of phase a. Then, after 0.5s, a short-circuit fault is applied to the fourth SM in the same arm. After 45 ms, the FDU successfully detects the open-circuit fault, as indicated in Figure 15(a). Instantaneously, the FTC sorting algorithm isolates the faulty SM in the upper arm, and its corresponding third SM in the lower arm, in order to balance the energy between the two arms. In addition, the proposed FTC increases v_c^* from 2.25 kV to

3 kV, and modifies the phase shift of the carrier waves from 45º to 60º to compensate for the loss of two SMs. The FDU detected the short-circuit fault after 3.3 ms.

The FTC sorting algorithm considers this condition as a cascading failure, since the percentage of faulty SMs in the upper arm of phase *a* reaches 25% of the total number of SMs. As a result, the FTC isolates the SMs in the three legs and blocks of the MMC. Figures 7.27 (a) and (b) portray the three-phase output voltages and currents, which are balanced even during the first fault. After the second fault, the three-phase voltages and currents are damped to zero, and the MMC is blocked. Figures 7.28 (a) and (b) illustrates that the capacitor voltages of the remaining SMs restore their balance at the new set value after the first fault. Following the second fault, the capacitors become floating, due to the converter blockage.

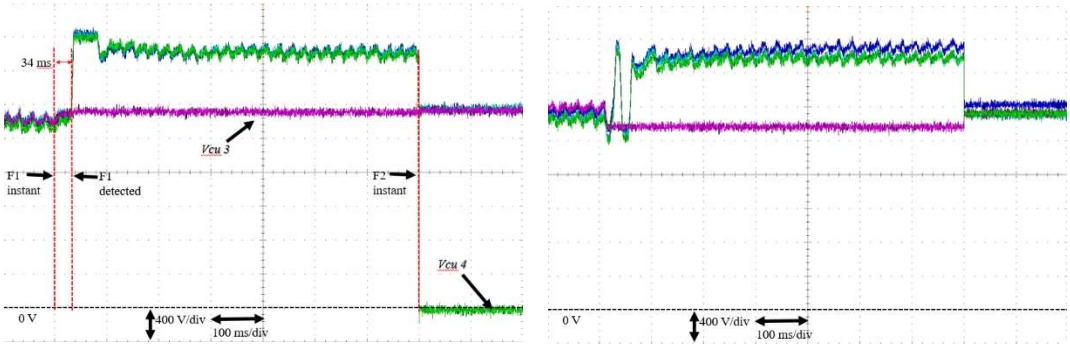
The proposed RLS scheme accurately estimates the capacitor voltages, as indicated in Figure 7.29 (a). It should be noted that after the second fault, where the MMC is blocked, the estimated capacitor voltages tend to zero, due to assigning zero switching signals to the SMs. Subsequently, the capacitors become floating and their voltages cannot be estimated. Figure 7.29 (b) shows that the proposed strategy succeeds in limiting the magnitude of the differential current, which tightly tracks its reference signal. Additionally, the averaging voltage reference, and the modulation signal for the first SM of the upper arm, are portrayed in Figures 7.30 (a) and (b), respectively.

The results demonstrate the accurate dynamic behaviour and fast response of the proposed FDU and FTC under cascading failure. The proposed strategy stabilizes the operation of the averaging and balancing control loops during SM faults.



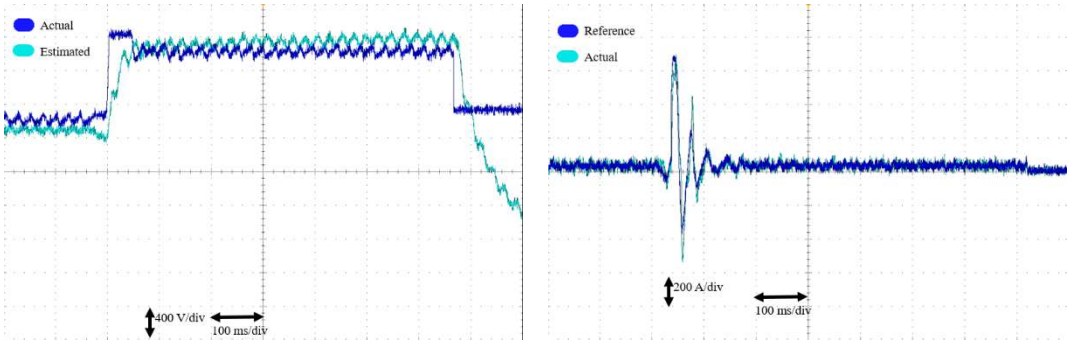
(a) (b)

Figure 7.27: The performance of the proposed strategy under cascading failure: a) three-phase voltages, b) three-phase load currents.



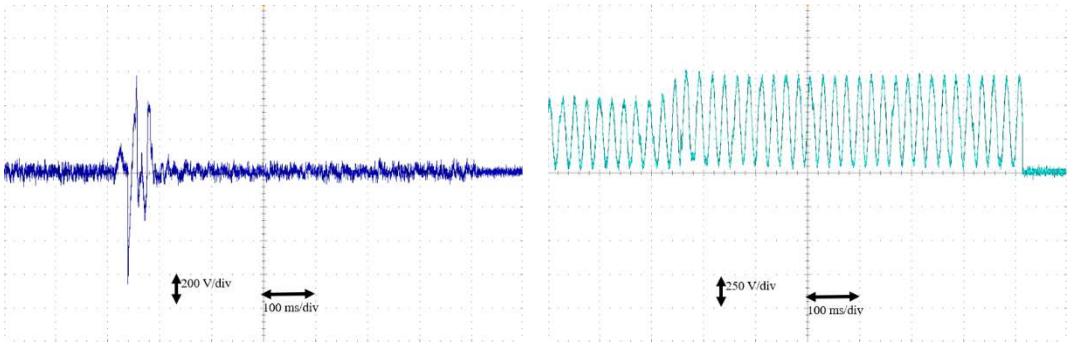
(a) (b)

Figure 7.28: The performance of the proposed strategy under cascading failure: a) capacitor voltages of the upper arm in phase a, b) capacitor voltages of the lower arm in phase a.



(a) (b)

Figure 7.29: Action of the different controllers for leg a: a) The capacitor voltage estimation of SM Vcu1, b) Actual and reference waveforms of the circulating current.



(a) (b)

Figure 7.30: Action of the different controllers for leg a under cascading failures: a) averaging voltage reference, b) Modulation signal for the first SM of the upper arm.

7.6 Chapter Summary

This chapter has presented the validation of the proposed capacitor voltage balancing, fault detection and fault tolerant control techniques using HIL real-time simulation. Based on the memory consumed in the FPGA controller used in the HIL platform, a study for the controller design in case of applying the proposed techniques for a MMC with 401 voltage levels is calculated, including the sizing of memory resources to investigate the suitability of the proposed techniques when applied to a MMC with high number of voltage levels. This study confirms that the proposed techniques are highly suitable for industrial implementation. Finally, HIL real-time results illustrate the robust behaviour of the proposed techniques, which are similar to PSCAD-offline simulations.

Chapter 8

Conclusion

8.1 Conclusion

This thesis presents two estimation units based on ADALINE and RLS algorithms for capacitor voltages of the submodules of the MMC. For each leg of the MMC, the proposed estimation unit requires only three sensors; one for the phase voltage and the others for the voltages across the arm reactors. Moreover, the proposed RLS estimation unit is integrated with a control strategy, in order to balance the voltages across the submodules of the MMC. Furthermore, the estimated capacitor voltages from the two techniques are utilized to detect and localize the open-circuit and short-circuit faults of submodule switches. Finally, it proposes a FTCU depending on a sorting algorithm, which is attached to the proposed capacitor voltage balancing and fault detection techniques, in order to form an integrated MMC inner controller. After isolating the faulty submodules, the proposed FTCU boosts the capacitor voltage, and modifies the phase shift between the carrier signals for the rest of submodules in the leg, in order to cope with the reduced number of effective submodules. The proposed integrated control strategy eliminates the need for direct measurements of capacitor voltages and their associated communication systems, which renders it suitable for implementing a low-cost centralized controller for the MMC with a large number of submodules. In addition, the proposed FDU and FTCU do not require any extra components, as they are based on the estimation algorithms that are simultaneously utilized for the proposed control of the MMC.

The fast response and accurate tracking of the proposed scheme for submodule capacitor voltage estimation are revealed from the results of offline simulations, as well as HIL real-time simulations, where the proposed control is tested under different dynamic conditions. Moreover, the proposed MMC controller succeeds in balancing the capacitor voltages. The accurate performance of the proposed FDU for detecting and localizing different faults, results from its hybrid processing, where the fault decision is not only based on the reduction on the estimated per-unit voltage, but also on the rate of change of the difference between the estimated voltages from the proposed ADALINE and RLS algorithms. Furthermore, the proposed FTCU succeeds in stabilizing the operation of the averaging and balancing control loops of the MMC under different types of faults. In addition, the circulating current tightly tracks its reference signal.

8.2 Summary of Contributions

The summaries of contributions achieved in the thesis are listed below:

- Conducting a detailed review of the fault detection and tolerance control of MMCs (Chapters 2 and 3). This review includes the structure, operation and modulation of MMCs. Moreover, common capacitor voltage balancing techniques proposed in the past are investigated. In addition, all MMC submodule faults are mapped with a particular focus on the consequences associated with each fault type. Finally, popular fault diagnosis and tolerance control techniques used for MMCs are also investigated, in order to determine the research areas that need to be further investigated

- Developing a capacitor voltage balancing technique for an MMC that depends on capacitor voltage estimation, without the need to measure the actual voltage in each submodule (Chapter 4), the proposed technique gives a better performance compared to other capacitor voltage techniques, since capacitor voltages are balanced under different operating conditions, keeping the output power free of distortions at a very low circulating current.

- Developing an improved fault diagnosis technique for detecting submodule faults which is able to detect and localize submodule faults without adding extra sensors or special power circuits, and without affecting the power quality of the MMC (Chapter 5), the proposed technique succeeds in detecting different submodule faults with a rapid response. Furthermore, it differentiates between fault events and outer system disturbances

- Developing a software fault tolerant control technique for controlling the MMC in the case of occurrence of any submodule fault (Chapter 6), the proposed technique does not require any redundant components. This means that costs are minimized, keeping the MMC secured during the fault incident, leading to increased MMC reliability, since its availability is increased.

8.3 Recommendations for Future Research

The following research points could be investigated in future:

- The stability of MMC-based HVDC grids could be investigated after applying the proposed MMC inner control, in order to assess the effect of fault tolerance in power system stability
- The proposed capacitor voltage balancing technique and FTCU uses the PS-PWM modulation technique. Other modulation techniques could be studied, in order to determine the most suitable switching algorithm for this application
- The proposed FDU is designed to detect faults inside power electronic devices. A condition monitoring unit for health monitoring of submodules could be investigated for the purpose of detecting faults inside submodule capacitors
- Another FDU for the detection of external DC faults could be attached to the proposed FDU, in order to offer an integrated FDU for detection of internal as well as external faults
- The proposed MMC inner control could be tested industrially, by applying various industrial operating conditions (e.g. EMI, noise, etc.).

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Appendix A

Modelling of Wind Energy Conversion Systems

This appendix describes the modelling process of wind energy conversion systems used in the simulation model which is presented in sub-section 4.3.2.

A.1 Modelling of the Wind Turbine

The wind turbine model is built according to the steady state characteristics of it. The power output is expressed as:

$$P_m = 0.5\rho A C_p v_w^3 \quad \text{(A.1)}$$

Where ρ is the air density, A is the effective area of the blade, C_p is the power coefficient of the turbine and v_w is the wind speed. The C_p needs to be modelled accurately as it is considered to be the governing factor in (1) since it determines the efficiency of the power converted from wind to mechanical [9]. The C_p is calculated from:

$$C_p = 0.22(116\lambda_1 - 0.4\beta - 5)e^{-12.5\lambda_1} \quad \text{(A.2)}$$

$$\lambda_1 = \frac{1}{\lambda+0.08} - \frac{0.035}{1+\beta^3} \quad \text{(A.3)}$$

where β is the pitch angle and λ is the tip speed ratio.

The output mechanical torque is given by:

$$T_m = \frac{P_m}{\omega_m} \quad \text{(A.4)}$$

where ω_m is the rotor angular speed.

A.2 Modelling of PMSG

A third order model is used to represent the PMSG on PSCAD/EMTDC software package. The mathematical equations of the PMSG model in the rotor frame are:

$$\frac{d}{dt}\begin{bmatrix} i_{ds}^e \\ i_{qs}^e \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_d} & \frac{L_q P \omega_m}{L_d} \\ -\frac{L_d P \omega_m}{L_q} & -\frac{R_s}{L_q} \end{bmatrix} \begin{bmatrix} i_{ds}^e \\ i_{qs}^e \end{bmatrix} - \begin{bmatrix} \frac{v_{ds}^e}{L_d} \\ \frac{v_{qs}^e - P\omega_m \psi_{pm}}{L_q} \end{bmatrix} \tag{A.5}$$

Where:

i_{ds}^e, i_{qs}^e are the stator current components.

v_{ds}^e, v_{qs}^e are the stator voltage components.

R_s is the stator resistance while L_d and L_q are the direct and quadrature components of the inductance.

P is the number of pole pairs and ψ_{pm} is the magnetic flux inside the PMSG.

The electromagnetic torque is given by:

$$T_e = \frac{3}{2} P(i_{qs}^e \psi_{pm} + (L_d - L_q) i_{qs}^e i_{ds}^e) \tag{A.6}$$

From (A1.4) and (A1.6) the electromechanical equation is written as:

$$T_m - T_e = J\frac{d\omega_m}{dt} + B\omega_m \tag{A.7}$$

A.3 Modelling of the DFIG

Induction machine dynamic operation modes have been described by means of a system of voltage differential equations for the stator and rotor coils respectively. The DFIG mathematical model expressed in unit values and $\alpha\beta$ coordinate system are as follows:

$$\frac{d\psi_{s\alpha}}{dt} = -\frac{1}{T_s^{'}}\psi_{s\alpha} + \frac{k_r}{T_s^{'}}\psi_{r\alpha} + u_{s\alpha}, \tag{A.8}$$

$$\frac{d\psi_{s\beta}}{dt} = -\frac{1}{T_s^{'}}\psi_{s\beta} + \frac{k_r}{T_s^{'}}\psi_{r\beta} + u_{s\beta}, \tag{A.9}$$

$$\frac{d\psi_{r\alpha}}{dt} = \frac{k_s}{T_r^{'}}\psi_{s\alpha} - \frac{1}{T_r^{'}}\psi_{r\alpha} - \omega\psi_{r\beta} + u_{r\alpha} \tag{A.10}$$

$$\frac{d\psi_{r\beta}}{dt} = \frac{k_s}{T_r^{'}}\psi_{s\beta} + \omega\psi_{r\alpha} - \frac{1}{T_r^{'}}\psi_{r\beta} + u_{r\beta}\,, \tag{A.11}$$

Rotor and stator feed voltage vector components are:

$$u_{s\alpha} = u_{sa}\,, \tag{A.12}$$

$$u_{s\beta} = \frac{1}{\sqrt{3}}\left(u_{sb} - u_{sc}\right), \tag{A.13}$$

$$u_{r\alpha} = u_{ra}\,, \tag{A.14}$$

$$u_{r\beta} = \frac{1}{\sqrt{3}}\left(u_{rb} - u_{rc}\right). \tag{A.15}$$

The stator and rotor current vector components, expressed by means of the known magnetic flux components, are as follows:

$$i_{s\alpha} = \frac{1}{L_s^{'}}\psi_{s\alpha} - \frac{k_s}{L_r^{'}}\psi_{r\alpha}\,, \tag{A.16}$$

$$i_{s\beta} = \frac{1}{L_s^{'}}\psi_{s\beta} - \frac{k_s}{L_r^{'}}\psi_{r\beta}\,, \tag{A.17}$$

$$i_{r\alpha} = -\frac{k_r}{L_s^{'}}\psi_{s\alpha} + \frac{1}{L_r^{'}}\psi_{r\alpha}, \tag{A.18}$$

$$i_{r\beta} = -\frac{k_r}{L_s^{'}}\psi_{s\beta} + \frac{1}{L_r^{'}}\psi_{r\beta}\,. \tag{A.19}$$

The generator electromagnetic moment, at the same time representing the input value of the wind turbine two-mass model, is:

$$m_e = \psi_{s\alpha} i_{s\beta} - \psi_{s\beta} i_{s\alpha}\,. \tag{A.20}$$

The following are the parametres as occurring in the equations from (A.8) to (A.19):

$$L_s^{'} = \sigma L_s\,, L_r^{'} = \sigma L_r\,, \sigma = 1 - \frac{L_m^2}{L_s L_r}\,, k_s = \frac{L_m}{L_s}\,, k_r = \frac{L_m}{L_r}\,,\ T_s^{'} = \frac{L_s^{'}}{R_s} \text{ and } T_r^{'} = \frac{L_r^{'}}{R_r}\,.$$

The induction generator stator active and reactive power momentary value is obtained by multiplying the stator voltage vector by conjugated-complex value of the stator current vector, as illustrated below:

$$p_{sa} = u_{s\alpha} i_{s\alpha} + u_{s\beta} i_{s\beta}\,, \tag{A.21}$$

$$p_{sr} = u_{s\beta} i_{s\alpha} - u_{s\alpha} i_{s\beta}\,. \tag{A.22}$$

The DFIG rotor active power momentary value may be calculated in a similar way:

$$p_{ra} = u_{r\alpha} i_{r\alpha} + u_{r\beta} i_{r\beta} . \quad \text{(A.23)}$$

The momentary value of the rotor reactive power equals zero.

The momentary values of the induction generator stator and rotor current may be obtained from the αβ coordinate system components by means of the following equations:

$$i_s = \sqrt{i_{s\alpha}^2 + i_{s\beta}^2} , \quad \text{(A.24)}$$

$$i_r = \sqrt{i_{r\alpha}^2 + i_{r\beta}^2} . \quad \text{(A.25)}$$

Losses in the generator coils stator and rotor DFIG are:

$$p_{Cu} = R_s i_s^2 + R_r i_r^2 . \quad \text{(A.26)}$$

A.4 Control of Active and Reactive Power Injected into the Grid

Controlling the flow of active and reactive powers in the grid is done by controlling both the DC and AC voltage at each terminal. The control system at each terminal is formed from five units as described in the following sub-sections.

A.4.1 Phase locked loop

The phase locked loop technique is responsible for synchronizing the AC voltage of the MMC with the grid voltage. This is done using a feed forward PI control loop which receives the quadrature axis voltage of the MMC AC terminals $V_{t\,q}$. The output of the PI controller is then added to the initial angular frequency ω_0. The output of the addition is passed through integrator resulting into the grid phase θ.

A.4.2 AC and DC voltage control loops

The active and reactive power control loops are very simple as they utilize two PI controllers to decide the values of the MMC direct and quadrature components of the desired MMC output current i_d^* and i_q^*.

A.4.3 Inner current loop

The inner current control loop is used to regulate the MMC output current based on the received references from the DC and AC control loops, the loop is designed based on the MMC dynamics of the AC side:

$$L_{grid}\frac{di_d}{dt} = i_q \omega L_{grid} - i_d R_{grid} + V_{t\,d} - V_{s\,d} \quad \text{(A.27)}$$

$$L_{grid}\frac{di_q}{dt} = -i_d \omega L_{grid} - i_q R_{grid} + V_{t\,q} - V_{s\,q} \quad \text{(A.28)}$$

Where L_{grid} and R_{grid} are the grid inductance and resistance. V_t is the MMC terminal voltage while V_s is the grid voltage.

According to (A.27) and (A.28), two PI controllers are added to regulate the i_d and i_q. The output of the two controllers is then added to the measured components of the grid voltage $V_{s\,d}$ and $V_{s\,q}$ forming two feed forward loops. The decoupled components of i_d and i_q are then subtracted from the two loops resulting in the reference terminal voltages V_{td}^* and V_{tq}^*. Figure A.1 shows the block diagram of the active and reactive power control.

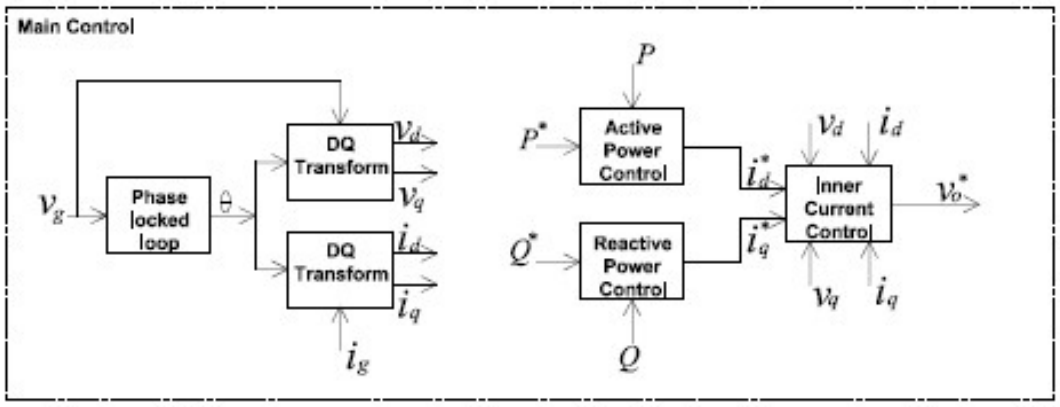


Figure A.1: Active and reactive power control.

Appendix B

Details of PSCAD Simulation Models

This appendix shows all details of the MMC simulation models, this include the following:

- The MMC submodule model
- The block of PS-PWM.
- The ADALINE programming function
- The RLS programming function
- The block of the proposed capacitor voltage balancing algorithm.
- The block of the proposed FDU.
- The block of the proposed FTCU.

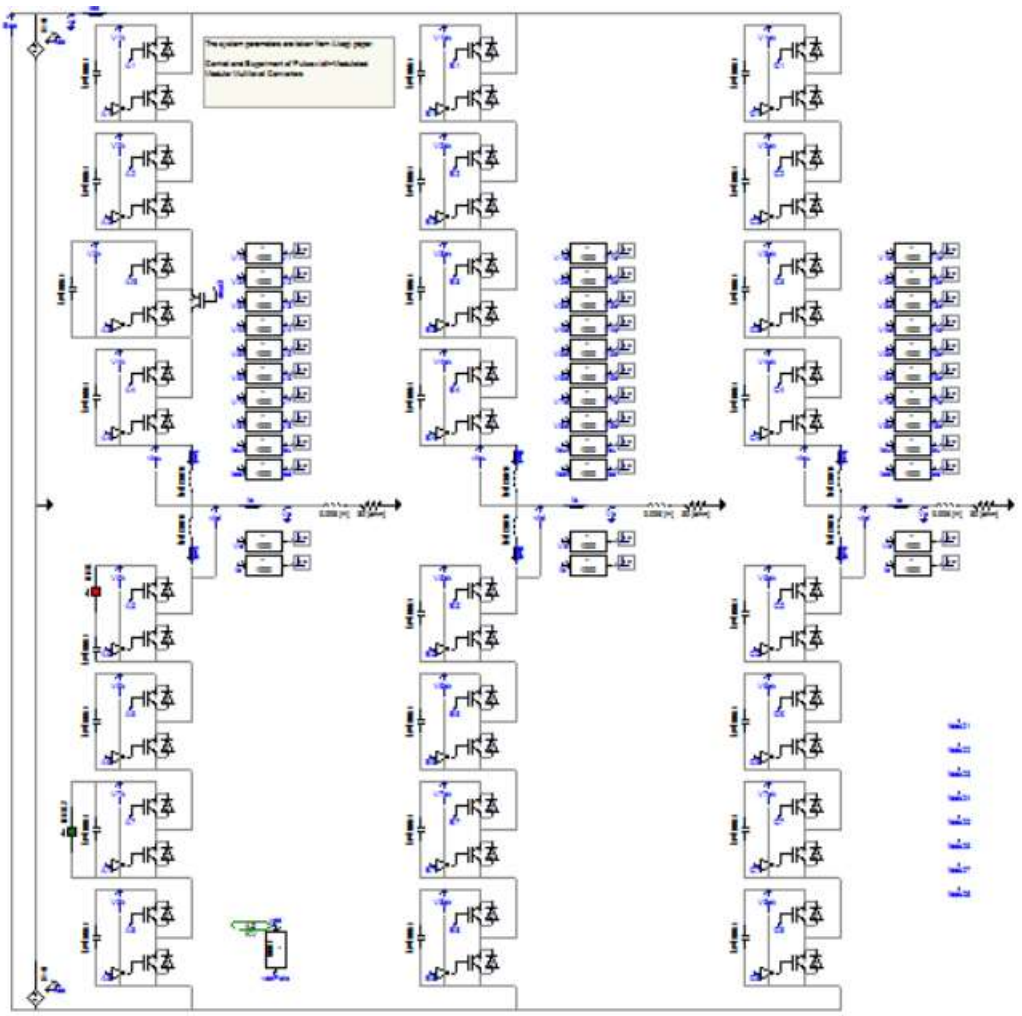


Figure B.1: The simulated 5 level MMC.

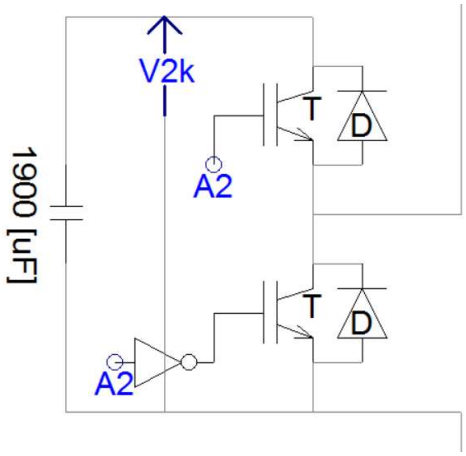


Figure B.2: The submodule model.

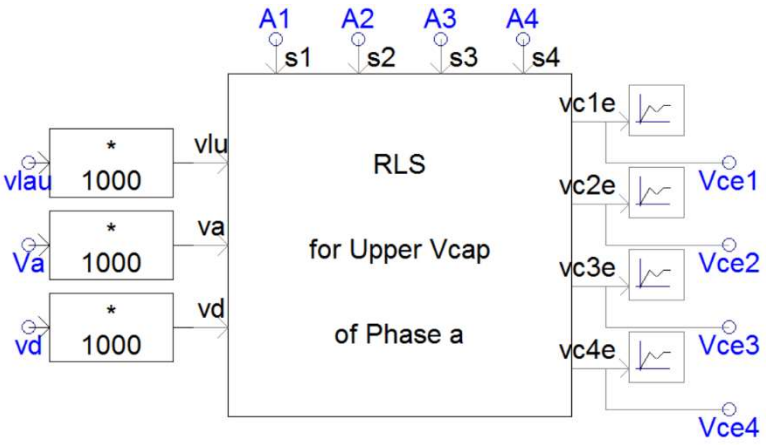


Figure B.3: The RLS programming block.

The following code is the RLS capacitor voltage balancing algorithm which is used in the RLS block (shown in Figure B.3):

```
! try
!2345678
        #LOCAL REAL auphi 4
        #LOCAL REAL auphip 4
        #LOCAL REAL aupphi 4
        #LOCAL REAL aup1 4
        #LOCAL REAL aup2 4
        #LOCAL REAL aup3 4
        #LOCAL REAL aup4 4
        #LOCAL REAL auth 4

       IF (TIME .EQ. 0) THEN
         cunter=1
          i=0
          DO AUK= 1, 4
           i=i+1
           auth(i) = 0
          aup1(i) = 0
          aup2(i) = 0
          aup3(i) = 0
          aup4(i) = 0
          END DO
          aup1(1) = 0.5
          aup2(2) = 0.5
          aup3(3) = 0.5
          aup4(4) = 0.5
       ENDIF

       auphi(1) = $s1
       auphi(2) = $s2
       auphi(3) = $s3
       auphi(4) = $s4

!IF (cunter .EQ. 1) THEN
!-----------------------p=(p-(p*phi*phi'*p/(la+phi'*p*phi)))/la;-------

          i=0             ! uphip = phi'*p
          DO AUK= 1, 4
           i=i+1

auphip(i)=(auphi(1)*aup1(i))+(auphi(2)*aup2(i))+(auphi(3)*aup3(i))+(auphi(4)*aup4(i
))
         END DO

          i=0             ! under = la+uphip*phi
          auunder=$landa
          DO AUK= 1, 4
           i=i+1
```

```
           auunder= auunder + (auphip(i)*auphi(i))
          END DO

          IF (auunder .GT. 0) THEN
!*****************************
          i=0           ! pphi=zero
          DO AUK= 1, 4
           i=i+1
           aupphi(i)=0
          END DO

          i=0           ! pphi=p*phi
          DO AUK= 1, 4
           i=i+1
           aupphi(1)=aupphi(1)+(aup1(i)*auphi(i))
           aupphi(2)=aupphi(2)+(aup2(i)*auphi(i))
           aupphi(3)=aupphi(3)+(aup3(i)*auphi(i))
           aupphi(4)=aupphi(4)+(aup4(i)*auphi(i))
          END DO

          i=0           ! p=(p-(upphi*uphip/under))/la;
          DO AUK= 1, 4
           i=i+1
           aup1(i)=(aup1(i)-(aupphi(1)*auphip(i)/auunder))/$landa
           aup2(i)=(aup2(i)-(aupphi(2)*auphip(i)/auunder))/$landa
           aup3(i)=(aup3(i)-(aupphi(3)*auphip(i)/auunder))/$landa
           aup4(i)=(aup4(i)-(aupphi(4)*auphip(i)/auunder))/$landa
          END DO
!-------------------------------------------------------------------------

!--------------------- th=th+p*phi*(y-phi'*th)  ------------------------

          i=0           ! c = y - phi'*th
          cau = ($vd)-($va)-($vlu)
          DO AUK= 1, 4
           i=i+1
           cau = cau - (auphi(i)*auth(i))
          END DO

          i=0           ! th = th + pphi*c
          DO AUK= 1, 4
           i=i+1
           auth(i) = auth(i) + (aupphi(i)*cau)
          END DO
!-------------------------------------------------------------------------
          ENDIF
!*****************************

         cunter=0
!       ENDIF
       cunter=cunter+1
       $vc1e = auth(1)
       $vc2e = auth(2)
       $vc3e = auth(3)
       $vc4e = auth(4)
```

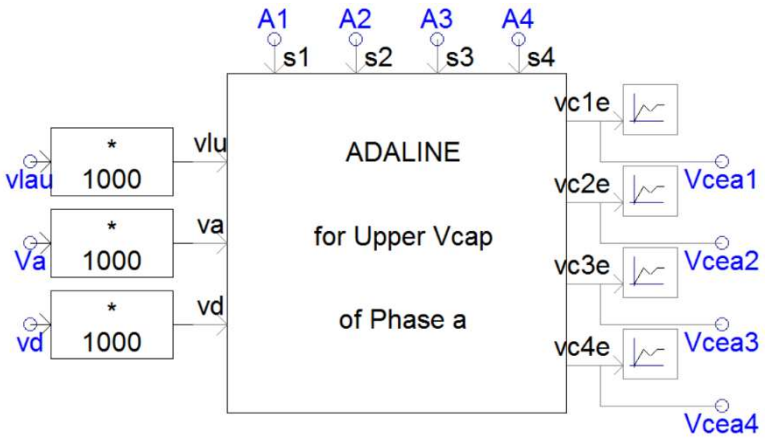
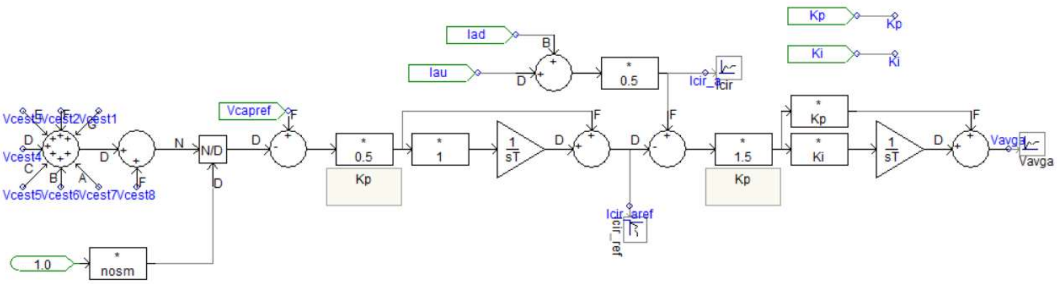


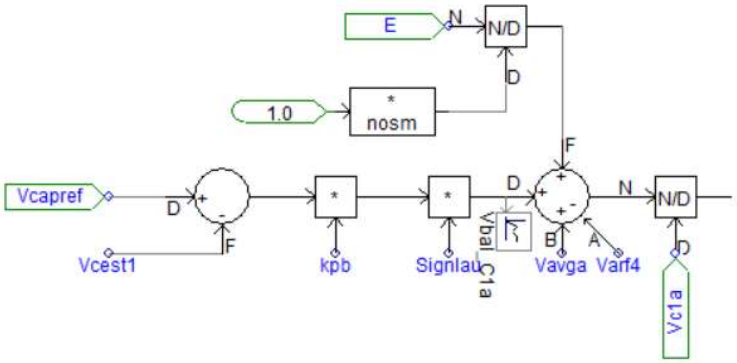
Figure B.4: The ADALINE programming block.

The following code is the ADALINE capacitor voltage balancing algorithm which is used in the ADALINE block (shown in Figure B.4):

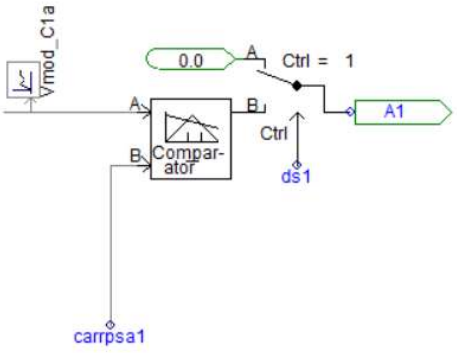
```
! try
!2345678
       IF (TIME .EQ. 0) THEN
         cunter=1
         w1 = 0
         w2 = 0
         w3 = 0
         w4 = 0
       ENDIF

!IF (cunter .EQ. 1) THEN
         yc = w1*($s1) + w2*($s2) + w3*($s3) + w4*($s4)
         E = ($s1)*($s1) + ($s2)*($s2) + ($s3)*($s3) + ($s4)*($s4)
          y = ($vd)-($va)-($vlu)
          IF (E .GT. 0) THEN
            c = ($alphh)*(y-yc)/E
            w1 = w1 + c*($s1)
            w2 = w2 + c*($s2)
            w3 = w3 + c*($s3)
            w4 = w4 + c*($s4)
          ENDIF
          cunter=0
!ENDIF
       cunter=cunter+1
       $vc1e = w1
       $vc2e = w2
       $vc3e = w3
       $vc4e = w4
```



(a)



(b)



(c)

Figure B.5: The block of the proposed capacitor voltage algorithm: a) The averaging controller, b) The balancing controller, c) The PS-PWM modulation technique.

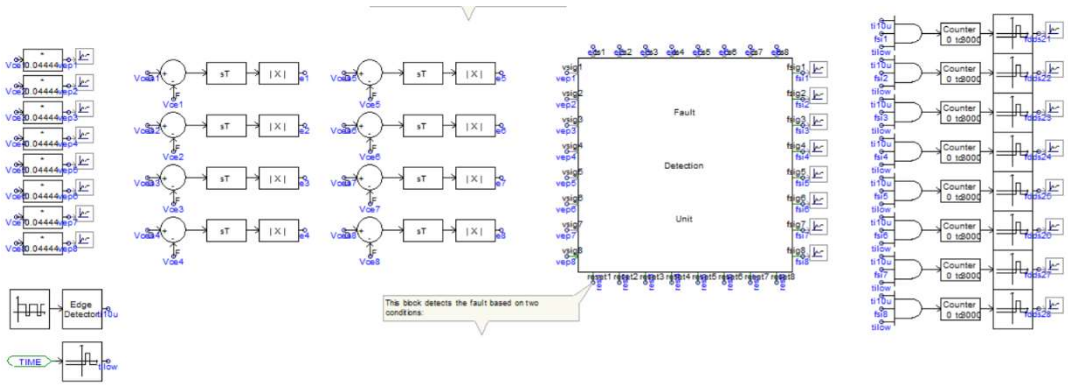


Figure B.6: The block of the proposed FDU.

The following code performs the necessary comparisons and decisions needed for the FDU block (shown in Figure B.6):

```
IF (($cs1 .GT. 200) .and. ($vsig1 .LT. 96)) THEN
$fsig1 = 1
$reset1 = 0
 ELSEIF ($vsig1 .GT. 96) THEN
 $fsig1 = 0
$reset1 = 1
 ENDIF

 IF (($cs2 .GT. 200) .and. ($vsig2 .LT. 96)) THEN
$fsig2 = 1
$reset2 = 0
 ELSEIF ($vsig2 .GT. 96) THEN
 $fsig2 = 0
$reset2 = 1
 ENDIF

 IF (($cs3 .GT. 200) .and. ($vsig3 .LT. 96)) THEN
$fsig3 = 1
$reset3 = 0
 ELSEIF ($vsig1 .GT. 96) THEN
 $fsig3 = 0
$reset3 = 1
 ENDIF

 IF (($cs4 .GT. 200) .and. ($vsig4 .LT. 96)) THEN
$fsig4 = 1
$reset4 = 0
 ELSEIF ($vsig4 .GT. 96) THEN
 $fsig4 = 0
$reset4 = 1
 ENDIF

 IF (($cs5 .GT. 200) .and. ($vsig5 .LT. 96)) THEN
$fsig5 = 1
$reset5 = 0
 ELSEIF ($vsig5 .GT. 96) THEN
 $fsig5 = 0
$reset5 = 1
 ENDIF

 IF (($cs6 .GT. 200) .and. ($vsig6 .LT. 96)) THEN
$fsig6 = 1
$reset6 = 0
 ELSEIF ($vsig1 .GT. 96) THEN
 $fsig6 = 0
$reset6 = 1
 ENDIF

 IF (($cs7 .GT. 200) .and. ($vsig7 .LT. 96)) THEN
$fsig7 = 1
$reset7 = 0
 ELSEIF ($vsig7 .GT. 96) THEN
```

```
$fsig7 = 0
$reset7 = 1
ENDIF

IF (($cs8 .GT. 200) .and. ($vsig8 .LT. 96)) THEN
$fsig8 = 1
$reset8 = 0
ELSEIF ($vsig8 .GT. 96) THEN
$fsig8 = 0
$reset8 = 1
ENDIF
```

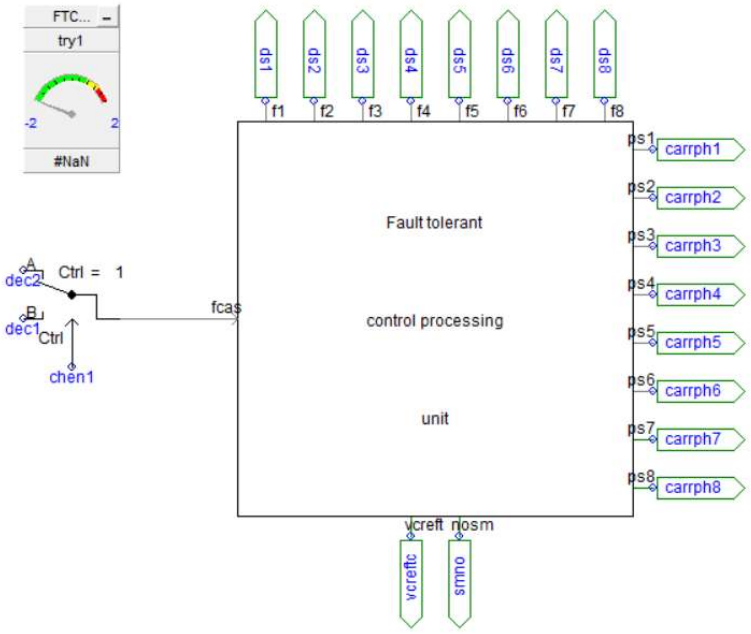


Figure B.7: The block of the proposed FDU.

The following code is the fault tolerant control sorting algorithm which is installed inside the FTCU (shown in Figure B.7):

```
IF($fcas .EQ. 0) THEN
$ps1 = 0
$ps2 = 90
$ps3 = 180
$ps4 = 270
$ps5 = 45
$ps6 = 135
$ps7 = 225
$ps8 = 315
$f1 = 0
$f2 = 0
$f3 = 0
$f4 = 0
$f5 = 0
$f6 = 0
$f7 = 0
$f8 = 0
$vcreft = 2250
$nosm = 8
ELSEIF($fcas .EQ. 18) THEN
$ps1 = 0
$ps2 = 120
$ps3 = 240
$ps4 = 270
$ps5 = 60
$ps6 = 180
$ps7 = 225
$ps8 = 300
$f1 = 0
$f2 = 0
```

```
$f3 = 0
$f4 = 1
$f5 = 0
$f6 = 0
$f7 = 1
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSEIF($fcas .EQ. 20) THEN
$ps1 = 0
$ps2 = 120
$ps3 = 240
$ps4 = 270
$ps5 = 60
$ps6 = 180
$ps7 = 180
$ps8 = 300
$f1 = 0
$f2 = 0
$f3 = 0
$f4 = 1
$f5 = 0
$f6 = 1
$f7 = 0
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSEIF($fcas .EQ. 24) THEN
$ps1 = 0
$ps2 = 120
$ps3 = 240
$ps4 = 270
$ps5 = 60
$ps6 = 60
$ps7 = 180
$ps8 = 300
$f1 = 0
$f2 = 0
$f3 = 0
$f4 = 1
$f5 = 1
$f6 = 0
$f7 = 0
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSEIF($fcas .EQ. 33) THEN
$ps1 = 0
$ps2 = 120
$ps3 = 240
$ps4 = 240
$ps5 = 60
$ps6 = 180
$ps7 = 300
$ps8 = 300
$f1 = 0
$f2 = 0
$f3 = 1
$f4 = 0
$f5 = 0
$f6 = 1
$f7 = 0
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSEIF($fcas .EQ. 36) THEN
$ps1 = 0
$ps2 = 120
$ps3 = 240
$ps4 = 240
$ps5 = 60
$ps6 = 180
$ps7 = 180
$ps8 = 300
$f1 = 0
$f2 = 0
$f3 = 1
```

```
 $f4 = 0
 $f5 = 0
 $f6 = 1
 $f7 = 0
 $f8 = 0
 $vcreft = 3000
 $nosm = 6
ELSEIF($fcas .EQ. 40) THEN
 $ps1 = 0
 $ps2 = 120
 $ps3 = 240
 $ps4 = 240
 $ps5 = 60
 $ps6 = 60
 $ps7 = 180
 $ps8 = 300
 $f1 = 0
 $f2 = 0
 $f3 = 1
 $f4 = 0
 $f5 = 1
 $f6 = 0
 $f7 = 0
 $f8 = 0
 $vcreft = 3000
 $nosm = 6
 ELSEIF($fcas .EQ. 65) THEN
 $ps1 = 0
 $ps2 = 120
 $ps3 = 120
 $ps4 = 240
 $ps5 = 60
 $ps6 = 180
 $ps7 = 300
 $ps8 = 300
 $f1 = 0
 $f2 = 1
 $f3 = 0
 $f4 = 0
 $f5 = 0
 $f6 = 0
 $f7 = 0
 $f8 = 1
 $vcreft = 3000
 $nosm = 6
ELSEIF($fcas .EQ. 66) THEN
 $ps1 = 0
 $ps2 = 120
 $ps3 = 120
 $ps4 = 240
 $ps5 = 60
 $ps6 = 180
 $ps7 = 300
 $ps8 = 300
 $f1 = 0
 $f2 = 1
 $f3 = 0
 $f4 = 0
 $f5 = 0
 $f6 = 0
 $f7 = 1
 $f8 = 0
 $vcreft = 3000
 $nosm = 6
 ELSEIF($fcas .EQ. 72) THEN
 $ps1 = 0
 $ps2 = 120
 $ps3 = 120
 $ps4 = 240
 $ps5 = 60
 $ps6 = 60
 $ps7 = 180
 $ps8 = 300
 $f1 = 0
 $f2 = 1
 $f3 = 0
 $f4 = 0
```

```
$f5 = 1
$f6 = 0
$f7 = 0
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSEIF($fcas .EQ. 129) THEN
$ps1 = 0
$ps2 = 0
$ps3 = 120
$ps4 = 240
$ps5 = 60
$ps6 = 180
$ps7 = 300
$ps8 = 300
$f1 = 1
$f2 = 0
$f3 = 0
$f4 = 0
$f5 = 0
$f6 = 0
$f7 = 0
$f8 = 1
$vcreft = 3000
$nosm = 6
ELSEIF($fcas .EQ. 130) THEN
$ps1 = 0
$ps2 = 0
$ps3 = 120
$ps4 = 240
$ps5 = 60
$ps6 = 180
$ps7 = 300
$ps8 = 300
$f1 = 1
$f2 = 0
$f3 = 0
$f4 = 0
$f5 = 0
$f6 = 0
$f7 = 1
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSEIF($fcas .EQ. 132) THEN
$ps1 = 0
$ps2 = 0
$ps3 = 120
$ps4 = 240
$ps5 = 60
$ps6 = 180
$ps7 = 180
$ps8 = 300
$f1 = 1
$f2 = 0
$f3 = 0
$f4 = 0
$f5 = 0
$f6 = 1
$f7 = 0
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSEIF(($fcas .EQ. 1) .or. ($fcas .EQ. 16) .or. ($fcas .EQ. 17)) THEN
$ps1 = 0
$ps2 = 120
$ps3 = 240
$ps4 = 240
$ps5 = 60
$ps6 = 180
$ps7 = 300
$ps8 = 300
$f1 = 0
$f2 = 0
$f3 = 1
$f4 = 0
$f5 = 0
```

```
$f6 = 0
$f7 = 0
$f8 = 1
$vcreft = 3000
$nosm = 6
ELSEIF(($fcas .EQ. 2) .or. ($fcas .EQ. 32) .or. ($fcas .EQ. 34)) THEN
$ps1 = 0
$ps2 = 120
$ps3 = 240
$ps4 = 240
$ps5 = 60
$ps6 = 180
$ps7 = 180
$ps8 = 300
$f1 = 0
$f2 = 0
$f3 = 1
$f4 = 0
$f5 = 0
$f6 = 0
$f7 = 1
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSEIF(($fcas .EQ. 4) .or. ($fcas .EQ. 64) .or. ($fcas .EQ. 68)) THEN
$ps1 = 0
$ps2 = 120
$ps3 = 120
$ps4 = 240
$ps5 = 60
$ps6 = 180
$ps7 = 180
$ps8 = 300
$f1 = 0
$f2 = 1
$f3 = 0
$f4 = 0
$f5 = 0
$f6 = 1
$f7 = 0
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSEIF(($fcas .EQ. 8) .or. ($fcas .EQ. 128) .or. ($fcas .EQ. 136)) THEN
$ps1 = 0
$ps2 = 0
$ps3 = 120
$ps4 = 240
$ps5 = 60
$ps6 = 60
$ps7 = 180
$ps8 = 300
$f1 = 1
$f2 = 0
$f3 = 0
$f4 = 0
$f5 = 1
$f6 = 0
$f7 = 0
$f8 = 0
$vcreft = 3000
$nosm = 6
ELSE
$ps1 = 0
$ps2 = 0
$ps3 = 120
$ps4 = 240
$ps5 = 60
$ps6 = 60
$ps7 = 180
$ps8 = 300
$f1 = 1
$f2 = 1
$f3 = 1
$f4 = 1
$f5 = 1
$f6 = 1
```

```
$f7 = 1
$f8 = 1
$vcreft = 0
$nosm = 0
ENDIF
```

Appendix C

Details of HIL Real-Time Simulations

This appendix shows all details of the MMC HIL real-time simulations. As mentioned in Chapter 7, the HIL real-time simulations is done through incorporating a physical FPGA controller (programmed using Labview) with a real-time digital simulator (programmed using RT-LAB/Simulink enviroment). Thus, the appendix is divided into two sections: the first shows the details of the RT-LAB/Simulink Model which has the MMC model, the fault simulation block, the proposed FTCU, the PS-PWM switching algorithm and the MMC voltages and currents monitoring console. While the second part shows the LABVIEW program which shows the ADALINE and RLS estimation blocks, the propsoed capacitor voltage balancing algorithm and the proposed FDU.

C.1 The RT-LAB/Simulink Real-time Simulation Model

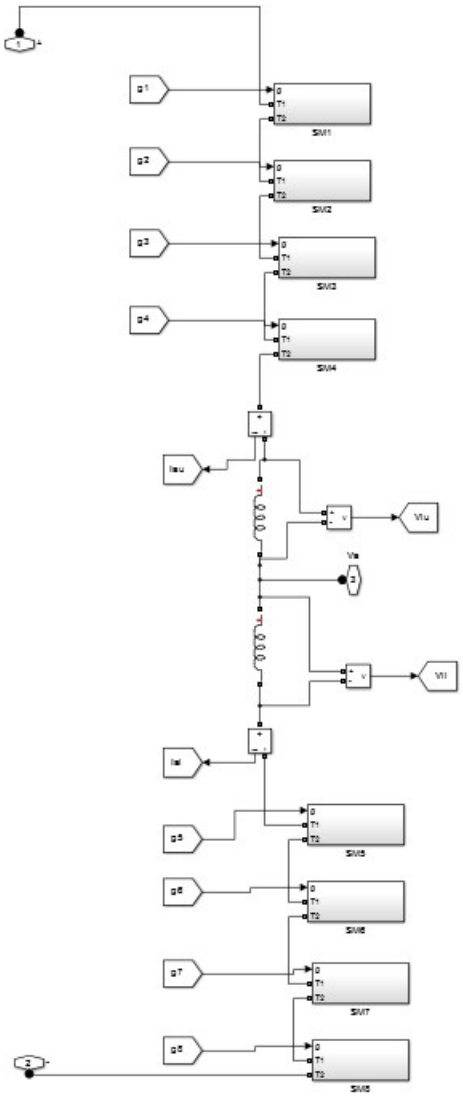


Figure C.1: The block of the proposed FDU for one leg.

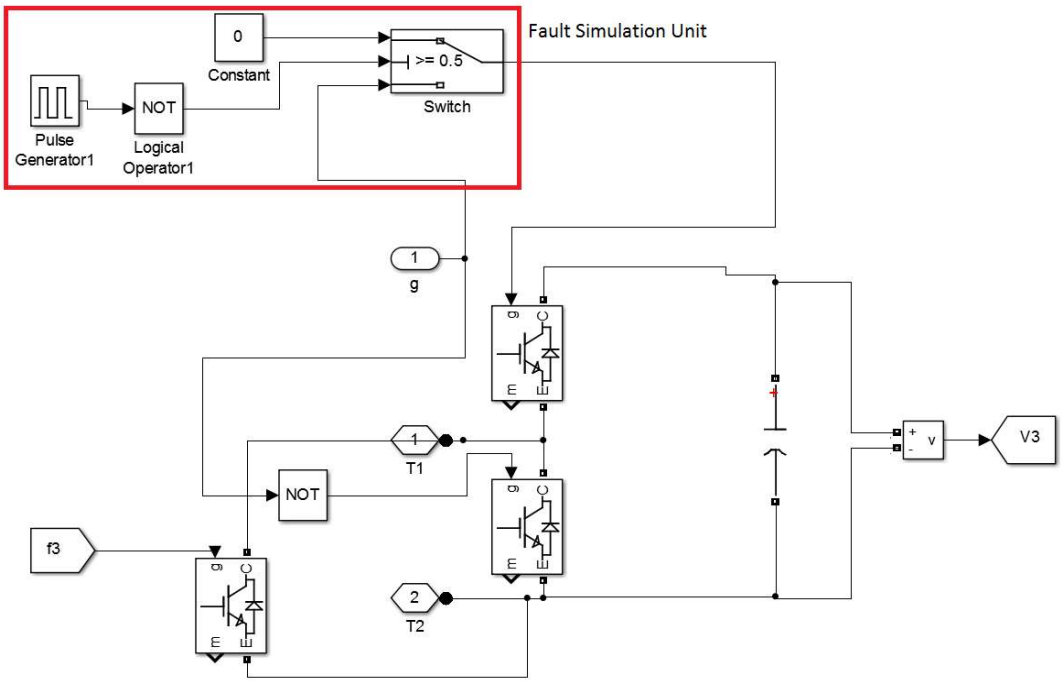


Figure C.2: The block of submodule including the fault simulation unit.

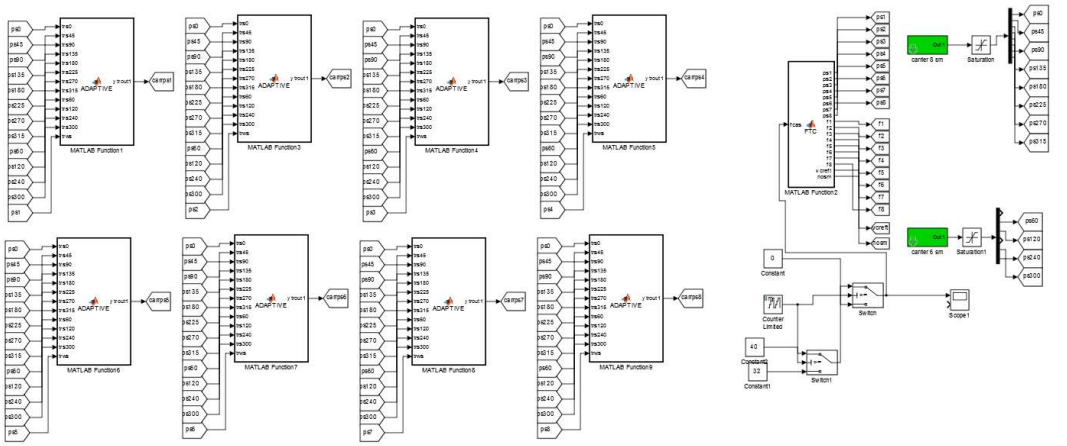


Figure C.3: The blocks of the proposed FTCU.

The following code is the fault tolerant control sorting algorithm which is installed inside a MATLAB function (as shown in Figure C.3):

```
function
[ps1,ps2,ps3,ps4,ps5,ps6,ps7,ps8,f1,f2,f3,f4,f5,f6,f7,f8,vcreft,no
sm]    = FTC(fcas)

if fcas==0
    ps1 = 0;
    ps2 = 90;
    ps3 = 180;
    ps4 = 270;
    ps5 = 45;
    ps6 = 135;
    ps7 = 225;
```

```
    ps8 = 315;
    f1 = 0;
    f2 = 0;
    f3 = 0;
    f4 = 0;
    f5 = 0;
    f6 = 0;
    f7 = 0;
    f8 = 0;
       vcreft = 2250;
    nosm = 8;
elseif fcas == 18
    ps1 = 0;
    ps2 = 120;
    ps3 = 240;
    ps4 = 270;
    ps5 = 60;
    ps6 = 180;
    ps7 = 225;
    ps8 = 300;
    f1 = 0;
    f2 = 0;
    f3 = 0;
    f4 = 1;
    f5 = 0;
    f6 = 0;
    f7 = 1;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 20
    ps1 = 0;
    ps2 = 120;
    ps3 = 240;
    ps4 = 270;
    ps5 = 60;
    ps6 = 180;
    ps7 = 180;
    ps8 = 300;
    f1 = 0;
    f2 = 0;
    f3 = 0;
    f4 = 1;
    f5 = 0;
    f6 = 1;
    f7 = 0;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 24
    ps1 = 0;
    ps2 = 120;
    ps3 = 240;
    ps4 = 270;
    ps5 = 60;
    ps6 = 60;
    ps7 = 180;
    ps8 = 300;
    f1 = 0;
    f2 = 0;
    f3 = 0;
```

```
    f4 = 1;
    f5 = 1;
    f6 = 0;
    f7 = 0;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 33;
    ps1 = 0;
    ps2 = 120;
    ps3 = 240;
    ps4 = 240;
    ps5 = 60;
    ps6 = 180;
    ps7 = 300;
    ps8 = 300;
    f1 = 0;
    f2 = 0;
    f3 = 1;
    f4 = 0;
    f5 = 0;
    f6 = 1;
    f7 = 0;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 36
    ps1 = 0;
    ps2 = 120;
    ps3 = 240;
    ps4 = 240;
    ps5 = 60;
    ps6 = 180;
    ps7 = 180;
    ps8 = 300;
    f1 = 0;
    f2 = 0;
    f3 = 1;
    f4 = 0;
    f5 = 0;
    f6 = 1;
    f7 = 0;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 40;
    ps1 = 0;
    ps2 = 120;
    ps3 = 240;
    ps4 = 240;
    ps5 = 60;
    ps6 = 60;
    ps7 = 180;
    ps8 = 300;
    f1 = 0;
    f2 = 0;
    f3 = 1;
    f4 = 0;
    f5 = 1;
    f6 = 0;
    f7 = 0;
```

```
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 65
    ps1 = 0;
    ps2 = 120;
    ps3 = 120;
    ps4 = 240;
    ps5 = 60;
    ps6 = 180;
    ps7 = 300;
    ps8 = 300;
    f1 = 0;
    f2 = 1;
    f3 = 0;
    f4 = 0;
    f5 = 0;
    f6 = 0;
    f7 = 0;
    f8 = 1;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 66
    ps1 = 0;
    ps2 = 120;
    ps3 = 120;
    ps4 = 240;
    ps5 = 60;
    ps6 = 180;
    ps7 = 300;
    ps8 = 300;
    f1 = 0;
    f2 = 1;
    f3 = 0;
    f4 = 0;
    f5 = 0;
    f6 = 0;
    f7 = 1;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 72
    ps1 = 0;
    ps2 = 120;
    ps3 = 120;
    ps4 = 240;
    ps5 = 60;
    ps6 = 60;
    ps7 = 180;
    ps8 = 300;
    f1 = 0;
    f2 = 1;
    f3 = 0;
    f4 = 0;
    f5 = 1;
    f6 = 0;
    f7 = 0;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 129
```

```
    ps1 = 0;
    ps2 = 0;
    ps3 = 120;
    ps4 = 240;
    ps5 = 60;
    ps6 = 180;
    ps7 = 300;
    ps8 = 300;
    f1 = 1;
    f2 = 0;
    f3 = 0;
    f4 = 0;
    f5 = 0;
    f6 = 0;
    f7 = 0;
    f8 = 1;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 130
    ps1 = 0;
    ps2 = 0;
    ps3 = 120;
    ps4 = 240;
    ps5 = 60;
    ps6 = 180;
    ps7 = 300;
    ps8 = 300;
    f1 = 1;
    f2 = 0;
    f3 = 0;
    f4 = 0;
    f5 = 0;
    f6 = 0;
    f7 = 1;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif fcas == 132
    ps1 = 0;
    ps2 = 0;
    ps3 = 120;
    ps4 = 240;
    ps5 = 60;
    ps6 = 180;
    ps7 = 180;
    ps8 = 300;
    f1 = 1;
    f2 = 0;
    f3 = 0;
    f4 = 0;
    f5 = 0;
    f6 = 1;
    f7 = 0;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif (fcas == 1) || (fcas == 16) || (fcas == 17)
    ps1 = 0;
    ps2 = 120;
    ps3 = 240;
    ps4 = 240;
```

```
    ps5 = 60;
    ps6 = 180;
    ps7 = 300;
    ps8 = 300;
    f1 = 0;
    f2 = 0;
    f3 = 1;
    f4 = 0;
    f5 = 0;
    f6 = 0;
    f7 = 0;
    f8 = 1;
    vcreft = 3000;
    nosm = 6;
elseif (fcas == 2) || (fcas == 32) || (fcas == 34)
    ps1 = 0;
    ps2 = 120;
    ps3 = 240;
    ps4 = 240;
    ps5 = 60;
    ps6 = 180;
    ps7 = 180;
    ps8 = 300;
    f1 = 0;
    f2 = 0;
    f3 = 1;
    f4 = 0;
    f5 = 0;
    f6 = 0;
    f7 = 1;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif (fcas == 4) || (fcas == 64) || (fcas == 68)
    ps1 = 0;
    ps2 = 120;
    ps3 = 120;
    ps4 = 240;
    ps5 = 60;
    ps6 = 180;
    ps7 = 180;
    ps8 = 300;
    f1 = 0;
    f2 = 1;
    f3 = 0;
    f4 = 0;
    f5 = 0;
    f6 = 1;
    f7 = 0;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
elseif (fcas == 8) || (fcas == 128) || (fcas == 136)
    ps1 = 0;
    ps2 = 0;
    ps3 = 120;
    ps4 = 240;
    ps5 = 60;
    ps6 = 60;
    ps7 = 180;
    ps8 = 300;
```

```
    f1 = 1;
    f2 = 0;
    f3 = 0;
    f4 = 0;
    f5 = 1;
    f6 = 0;
    f7 = 0;
    f8 = 0;
    vcreft = 3000;
    nosm = 6;
    else
    ps1 = 0;
    ps2 = 0;
    ps3 = 120;
    ps4 = 240;
    ps5 = 60;
    ps6 = 60;
    ps7 = 180;
    ps8 = 300;
    f1 = 1;
    f2 = 1;
    f3 = 1;
    f4 = 1;
    f5 = 1;
    f6 = 1;
    f7 = 1;
    f8 = 1;
    vcreft = 0;
    nosm = 1000000;
end
```

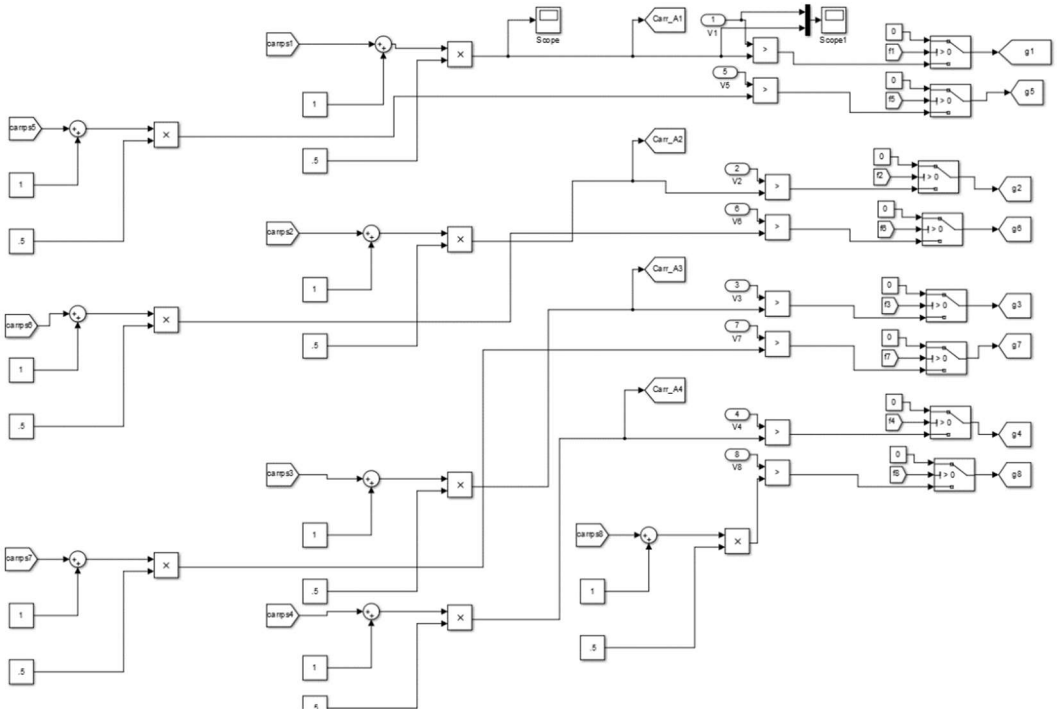


Figure C.4: The blocks of the PS-PWM switching algorithm.

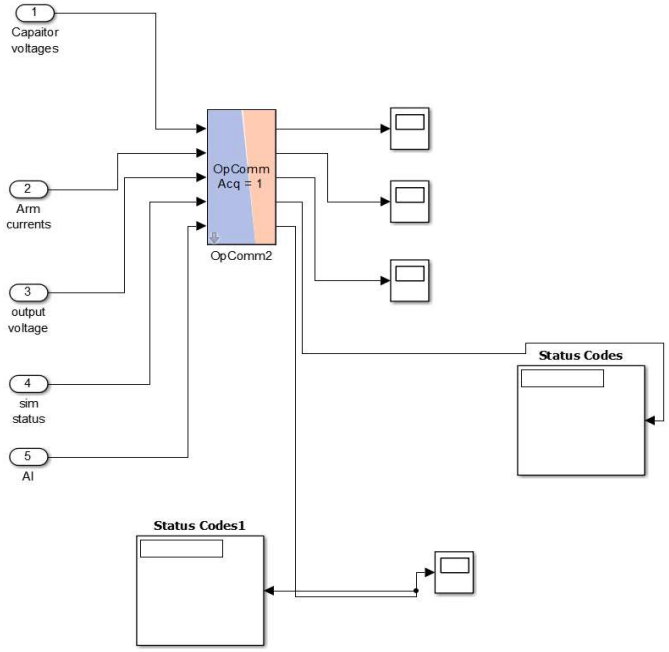


Figure C.5: The Monitoring console.

C.2 The cRIO/LABVIEW Programming Blocks

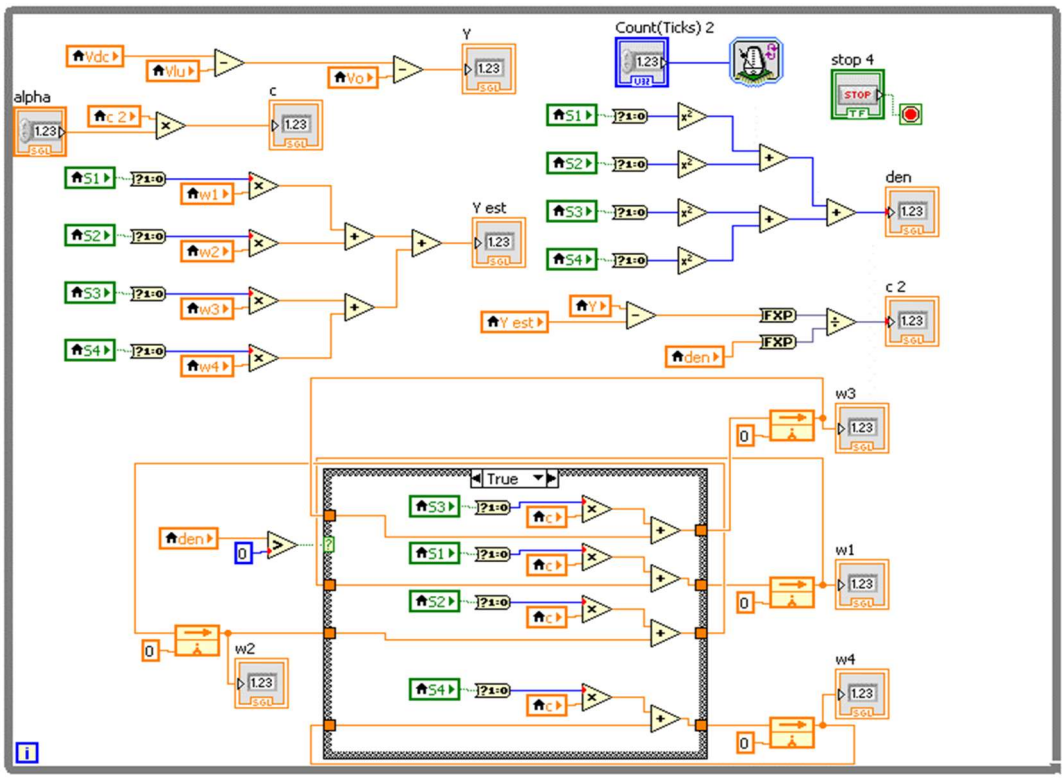


Figure C.6: The LABVIEW block of the ADALINE capacitor voltage estimation algorithm for one arm.

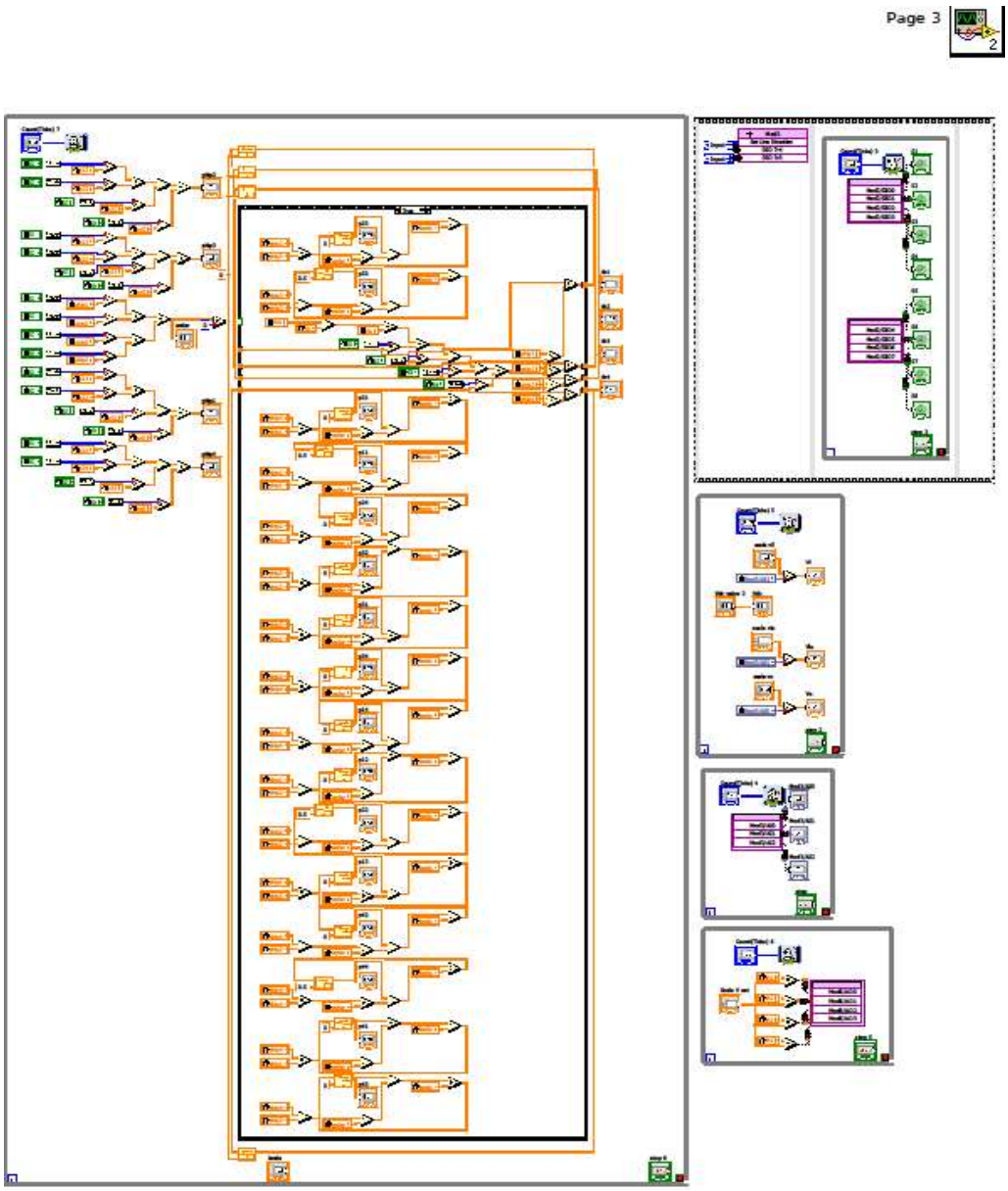


Figure C.7: The LABVIEW block of the RLS capacitor voltage estimation algorithm for one arm.

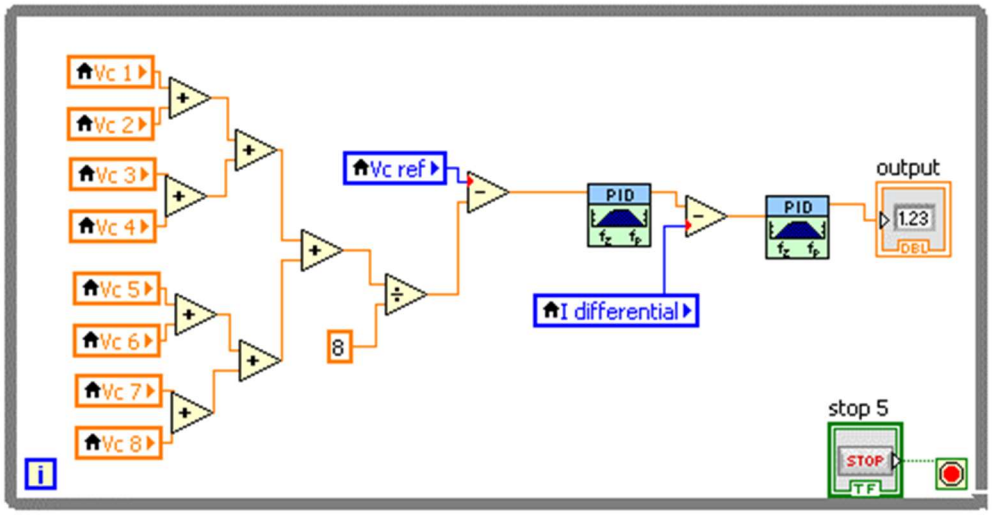


Figure C.8: The LABVIEW block of the averaging control for one leg.

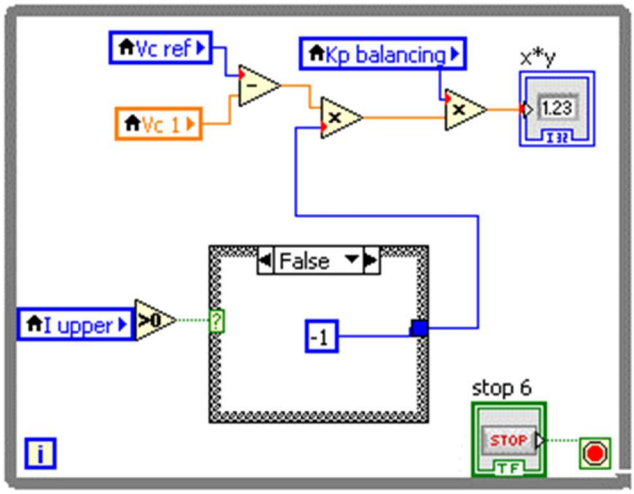


Figure C.9: The LABVIEW block of the balancing control for one submodule.

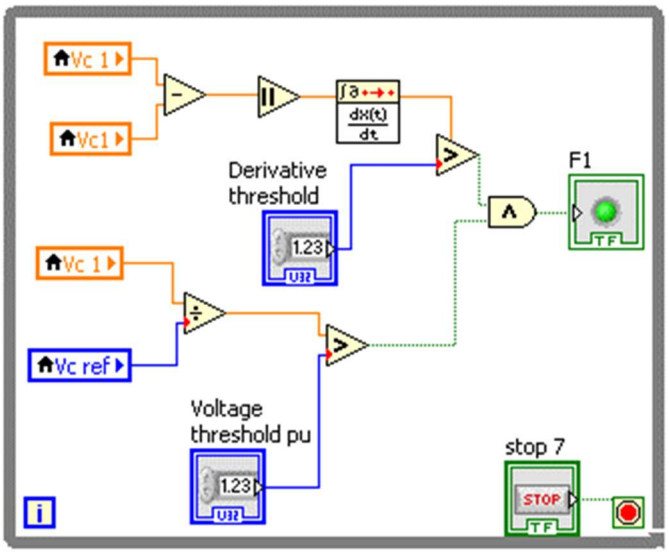


Figure C.10: The LABVIEW block of the proposed FDU (for one submodule).

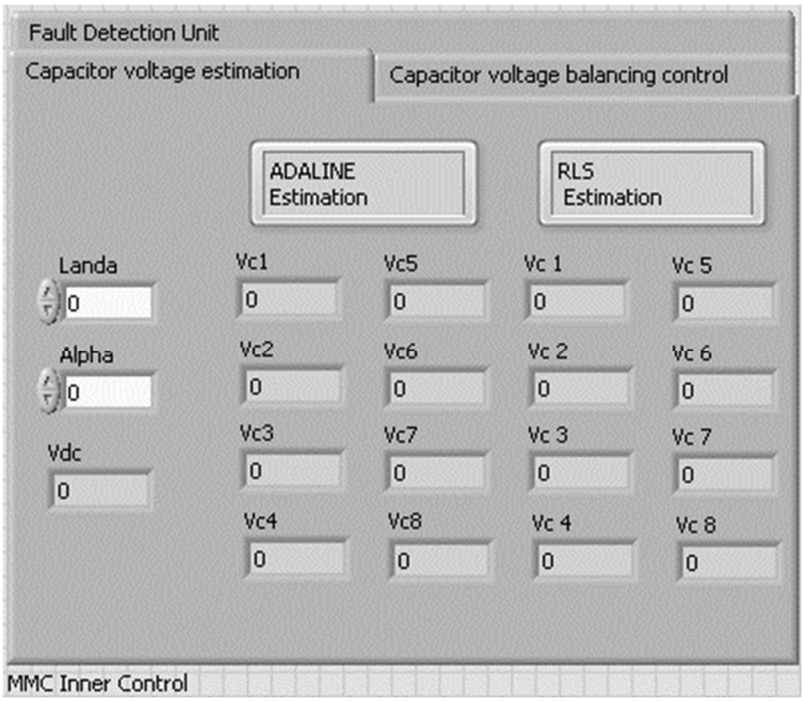


Figure C.11: The LABVIEW graphical user interface of the capacitor voltage estimation.

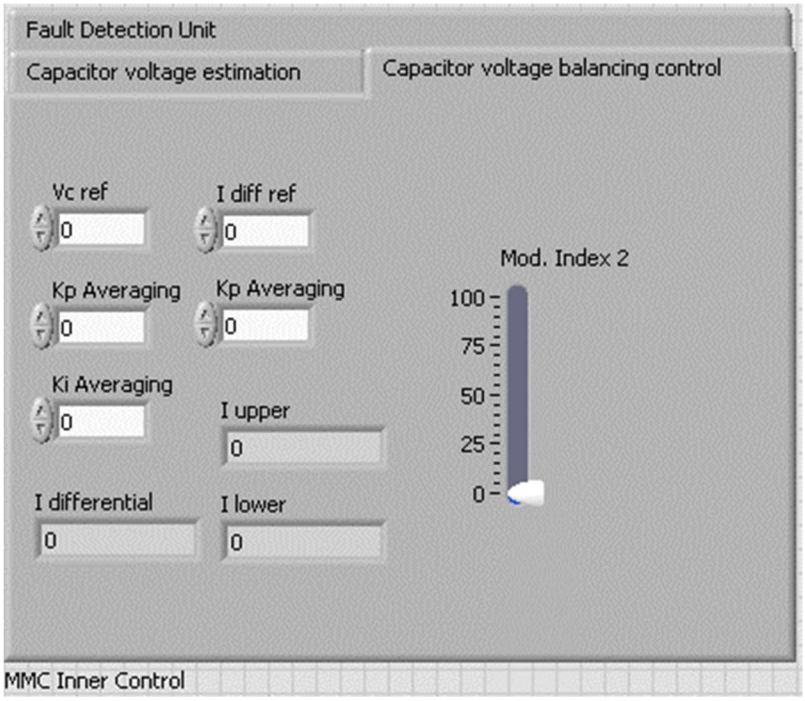


Figure C.12: The LABVIEW graphical user interface of the capacitor voltage balancing control.

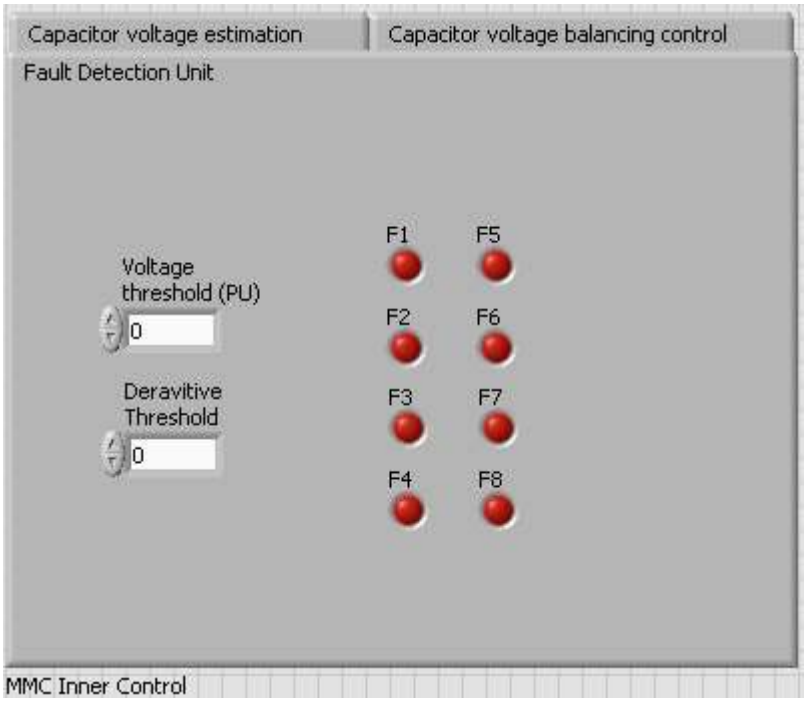


Figure C.13: The LABVIEW graphical user interface of the proposed FDU.

Appendix D

Selected Publications

Capacitor Voltage Balancing Strategy Based on Sub-module Capacitor Voltage Estimation for Modular Multilevel Converters

Mahmoud Abdelsalam, Mostafa Marei, *Senior Member, IEEE*, Sarath Tennakoon, *Member, IEEE*, and Alison Griffiths

***Abstract*—The modular multilevel converter (MMC) is expected to be used extensively in high-voltage direct current (HVDC) transmission networks because of its superior characteristics over the line-commutated converter (LCC). A key issue of concern is balancing sub-module capacitor voltages in the MMCs, which is critical for the correct operation of these converters. The majority of voltage balancing techniques proposed thus far require that the measurement of the capacitor voltages use a reliable measuring system. This can increase the capital cost of the converters. This paper presents a voltage balancing strategy based on capacitor voltage estimation using the adaptive linear neuron (ADALINE) algorithm. The proposed estimation unit requires only three voltage sensors per phase for the arm reactors and the output phase voltages. Measurements of sub-module capacitor voltages and associated communication links with the central controller are not needed. The proposed strategy can be applied to MMC systems that contain a large number of sub-modules. The method uses PSCAD/EMTDC, with particular focus on dynamic performance under a variety of operating conditions.**

***Index Terms*—Capacitor balancing, HVDC, MMC.**

I. Introduction

VOLTAGE source converters (VSCs) are being used increasingly in high-voltage direct current (HVDC) transmission systems over line-commutated converters (LCCs), particularly for connecting off shore wind farms. The advantages of using VSC include the ability to control active and reactive power independently, the ability to supply weak or passive networks, and VSC's lower space footprint. Although VSCs have many topologies, the modular multilevel converter (MMC) is considered the most suitable topology for high voltage applications, especially for power transmission and distribution. Their advantages include potential to eliminate harmonic filters with a sufficient number of voltage levels, elimination of the DC-link capacitor, and low switching losses [1], [2].

The MMC consists of sub-modules connected in a series, and forming a leg in each phase. The sub-module can be a half-bridge or a full-bridge and each sub-module has a capacitor that buffers the energy from the DC to the AC side and vice versa, thus eliminating the DC-link capacitor. As shown in Fig. 1, each phase leg is divided into two arms—upper and lower. Each arm has an identical number of sub-modules to generate balanced voltage between the two arms of each phase. Inductors are installed in arms to smoothen and filter the currents [3], [4].

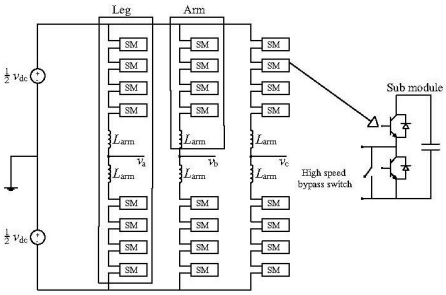


Fig. 1. Three-phase MMC topology and internal sub-module.

This paper presents a new voltage balancing control technique based on capacitor voltage estimation in place of traditional direct measurement. The main contribution of the proposed technique is the elimination of the communication burden used to send the voltage measurements from sub-modules to the central controller. As a result, not only the cost is reduced, but the wiring and associated problems are also minimized, which renders the proposed strategy attractive for the practical realization of a MMC with a large number of sub-modules. The proposed control technique has been evaluated using simulations where a number of case studies were conducted to test the dynamic performance under a variety of operating conditions. Section II shows the modeling of the

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MMC, including the mathematical representation and the switching algorithm. Section III shows the proposed balancing algorithm while presenting the capacitor voltage estimation technique. Section IV presents the simulation results with some discussions. Finally, a conclusion for the conducted work is presented in section V.

II. Modeling of MMC

Generally, the operation of the MMC depends on the switching of the sub-module IGBTs. The switching is performed by a switching algorithm, which generates the firing signals to each sub-module [5].

A. MMC Operating Modes

The MMC half bridge sub-module has four operation modes during which energy is transferred:

Mode 1: When S_1 is closed, S_2 is opened, and the arm has positive polarity. The current flows into the capacitor, charging it. The sub-module is then inserted. See Fig. 2(a).

Mode 2: When S_1 is opened, S_2 is closed, and the arm has positive polarity. The sub-module is bypassed, and the current flows towards the next sub-module, keeping the capacitor charge constant. The sub-module is then bypassed. See Fig. 2(b).

Mode 3: S_1 is closed, S_2 is opened, and the arm has negative polarity. The capacitor starts to discharge and then the sub-module is inserted. See Fig. 2(c).

Mode 4: When S_1 is opened, S_2 is closed, and the arm has negative polarity. The current flows towards the next module, keeping the capacitor charge constant, after which and the sub-module is bypassed. See Fig. 2(d).

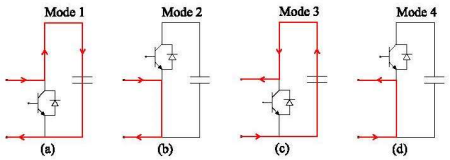

Fig. 2. Different operating modes of MMC sub-modules. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

B. Mathematical Model of MMC

For the purpose of designing an inner control system for the MMC, it is necessary to mathematically analyze the converter. The converter arms, shown in Fig. 3, are represented as variable capacitors connected in a series with arm resistance and inductance [6]. The number of sub-modules per arm and the switching frequency is assumed as infinite to simplify the analysis because of the perfect sinusoidal output voltage and total voltage balancing between arms. The arm capacitance insertion is represented with a modulation value $m_{\text{arm}\,x}$, where x may be u for upper arm or l for lower arm. The $m_{\text{arm}\,x}$ is varied from 0 to 1. For example, when $m_{\text{arm u}} = 0$, this indicates that all sub-modules in the upper arm are bypassed and when $m_{\text{arm l}} = 1$, this indicates that all sub-modules in the lower arm are inserted. The value $\Sigma v_{\text{C}x}$ is the sum of arm capacitor voltages. The arm voltage is given by:

$$v_x(t) = m_{\text{arm}\,x}(t).\Sigma v_{\text{C}x}. \tag{1}$$

The inserted arm capacitance is given by:

$$C_{\text{ins}\,x} = \frac{C_{\text{SM}}}{N.m_{\text{arm}\,x}(t)} \tag{2}$$

where C_{SM} is the capacitance of one sub-module and N is the number of sub-modules per arm. If the arm current is $i_x(t)$, the total capacitor voltage dynamics can be expressed by:

$$\frac{d\Sigma v_{\text{C}x}}{dt} = \frac{i_x(t)}{C_{\text{ins}\,x}}. \tag{3}$$

Substituting (2) in (3), the capacitor voltage dynamics can be expressed for the upper and lower arms by:

$$\frac{d\Sigma v_{\text{Cu}}}{dt} = \frac{N.m_{\text{arm u}}.i_{\text{u}}}{C_{\text{SM}}} \tag{4}$$

$$\frac{d\Sigma v_{\text{Cl}}}{dt} = \frac{N.m_{\text{arm l}}.i_{\text{l}}}{C_{\text{SM}}}. \tag{5}$$

The current i_{diff} is the differential current, which circulates between the phase legs. The circulating current of any phase is described as follows:

$$i_{\text{diff}} = \frac{i_{\text{u}} + i_{\text{l}}}{2}. \tag{6}$$

By performing the necessary circuit analysis, the output phase voltage v_{o} is given by:

$$v_{\text{o}} = \frac{v_{\text{dc}}}{2} - L_{\text{arm}}\frac{di_{\text{u}}}{dt} - m_{\text{arm u}}\Sigma v_{\text{Cu}} \tag{7}$$

$$v_{\text{o}} = -\frac{v_{\text{dc}}}{2} + L_{\text{arm}}\frac{di_{\text{l}}}{dt} + m_{\text{arm l}}\Sigma v_{\text{Cl}}. \tag{8}$$

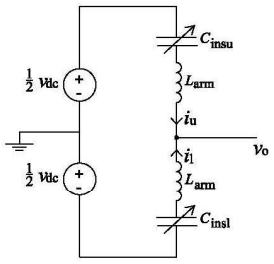

Fig. 3. The MMC average model.

C. MMC Switching Algorithm

Many switching algorithms have been proposed in the literature [7]–[10], and the modulation techniques that have been used can be divided into two main categories: 1) reference signal based and 2) carrier based. The phase shifted pulse width modulation (PS-PWM), which is one of the well-known

carrier based techniques, is utilized because of the following advantages [11]:

1) Ease of implementation;
2) lower losses due to reduced switching frequency; and
3) stable performance during dynamic changes.

In the PS-PWM technique, illustrated in Fig. 4, each sub-module has a dedicated triangular carrier waveform with the same magnitude, but with a different phase shift.

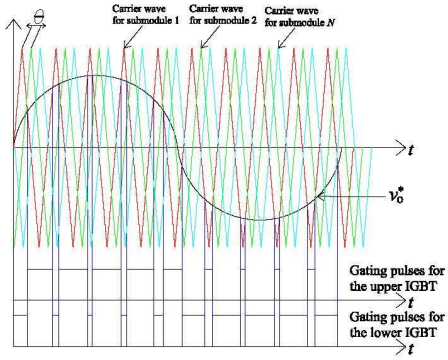

Fig. 4. The PS-PWM concept.

The switching signal for a sub-module results from comparing its corresponding carrier wave with the sinusoidal voltage reference signal v_{o}^{*}. The phase shift between each consecutive carrier signal is given by:

$$\theta = \frac{360}{N-1}. \tag{9}$$

III. Proposed Capacitor Voltage Estimation Technique

The voltage balancing process is vital for keeping the power quality at the standard level, as it significantly reduces the voltage ripples of the sub-module capacitors [12]–[14]. The proposed algorithm consists of three main stages:

1) Capacitor voltage estimation;
2) averaging control;
3) balancing control for capacitors' voltages.

A. Capacitor Voltage Estimation Technique

The capacitor voltage estimation is performed using the Adaptive Linear Neuron (ADALINE) algorithm. ADALINE is known for its efficiency and its rapid on-line tracking technique for dynamically changing voltage signals. It has been utilized in many applications because of its robust performance, low calculation burden, and accurate results [15], [16]. The ADALINE algorithm is formed by simple calculations that do not consume large computing time, which is very important in the application of capacitor voltage estimation. To estimate the capacitor voltages, the MMC governing equations given by (7) and (8) are rearranged and rewritten in the vector form as follows:

$$\frac{v_{\mathrm{dc}}}{2} - v_{\mathrm{o}} - v_{\mathrm{Lu}} = \begin{bmatrix} S_{\mathrm{u1}} & S_{\mathrm{u2}} & \dots & S_{\mathrm{u}N} \end{bmatrix} \begin{bmatrix} v_{\mathrm{cu1\_est}} \\ v_{\mathrm{cu2\_est}} \\ \vdots \\ v_{\mathrm{cu}N\_\mathrm{est}} \end{bmatrix} \tag{10}$$

$$\frac{v_{\mathrm{dc}}}{2} + v_{\mathrm{o}} - v_{\mathrm{Ll}} = \begin{bmatrix} S_{\mathrm{l1}} & S_{\mathrm{l2}} & \dots & S_{\mathrm{l}N} \end{bmatrix} \begin{bmatrix} v_{\mathrm{cl1\_est}} \\ v_{\mathrm{cl2\_est}} \\ \vdots \\ v_{\mathrm{cl}N\_\mathrm{est}} \end{bmatrix} \tag{11}$$

where S_{xi} is the switching state for the i^{th} sub-module, $v_{\mathrm{Lu}} = L_{\mathrm{arm}} \frac{di_{\mathrm{u}}}{dt}$, and $v_{\mathrm{Ll}} = L_{\mathrm{arm}} \frac{di_{\mathrm{l}}}{dt}$.

The ADALINE algorithm produces a linear combination of its input vector $X(k)$, which represents the switching state of each sub-module whether it is inserted or by-passed at time k, and it is written as follows:

$$\boldsymbol{X}(k) = \begin{bmatrix} S_{x1} & S_{x2} & \dots & S_{xN} \end{bmatrix}^{\mathrm{T}} \tag{12}$$

where the suffix T refers to the transpose operation. As shown in Fig. 5, the input vector is multiplied by the weight vector W, which resembles the estimated capacitor voltages, given in (10) and (11):

$$\boldsymbol{W}(k) = \begin{bmatrix} v_{\mathrm{cx1\_est}} & v_{\mathrm{cx2\_est}} & \dots & v_{\mathrm{cx}N\_\mathrm{est}} \end{bmatrix}. \tag{13}$$

This multiplication is performed to produce the predicted linear output $\hat{y}(k) = \boldsymbol{X}^{\mathrm{T}}\boldsymbol{W}(k)$. The next step is updating the weight vector using an adaptation algorithm called the Widrow-Hoff delta rule given by [17]:

$$\boldsymbol{W}(k+1) = \boldsymbol{W}(k) + \alpha \frac{\boldsymbol{X}(k)(y(k) - \hat{y}(k))}{\boldsymbol{X}(k)^{\mathrm{T}} \boldsymbol{X}(k)} \tag{14}$$

where α is the reduction factor and $y(k) = \frac{v_{\mathrm{dc}}}{2} \pm v_{\mathrm{o}} - v_{\mathrm{Lx}}$. The adaptation algorithm is responsible for adjusting the weighting vector, which represents the estimated capacitor voltages so that the linear output of the ADALINE, $\hat{y}(k)$ is equal to its target value $y(k)$. When the error between the measured signal $y(k)$ and the estimated signal $\hat{y}(k)$ converges to zero, the ADALINE algorithm decomposes the signal and estimates capacitor voltages.

It is observed that increasing the reduction factor α increases the convergence speed on account of losing stability as the prediction error may increase dramatically. This observation is a common behavior of the Widrow-Hoff delta rule for all the study cases. A practical value for the reduction factor α is 0.002 for this application. This value is determined based on minimizing the error to guarantee system stability [18]. It is worth mentioning that the proposed capacitor voltage estimation unit is based on three voltage sensors per phase to measure the voltage across the arm reactors and the output phase voltage. This action enables the implementation of a low-cost centralized controller for the MMC with large numbers of sub-modules, since voltage measurements of sub-modules and their associated communication links are eliminated.

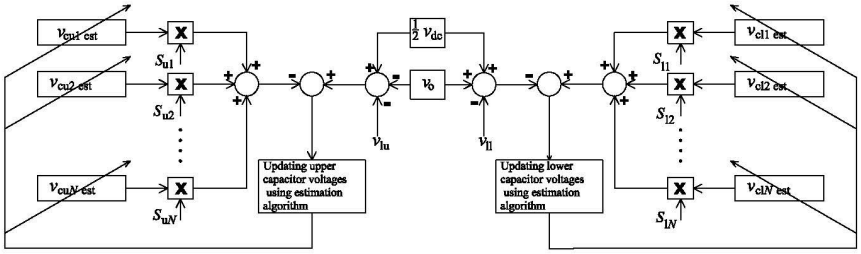

Fig. 5. Block diagram of the proposed capacitors voltages estimation unit based on the ADALINE algorithm.

B. Averaging Control

The concept of averaging control is responsible for controlling the average voltage across a complete leg. Averaging control is formed from two cascaded loops as shown in Fig. 6 [19]. The first loop is the voltage control loop where the estimated average voltage, $\hat{v}_{\text{avg}} = (\sum v_{\text{cu}_{\text{est}}} + \sum v_{\text{cl}_{\text{est}}})/2N$, is subtracted from the reference capacitor voltage, v_{C}^*, and the resultant error is processed through a PI controller to generate the reference signal for the differential current, i_{diff}^*. Another PI controller is utilized in the inner loop to regulate the differential current calculated from (6) at its reference signal. The action of the inner loop controller is the averaging voltage signal, v_{avg}^*.

C. Balancing Control for Capacitor Voltages

The balancing control method, presented in Fig. 7, is a centralized control system that generates reference signals for balancing the voltage across sub-module capacitors based on estimated voltages from the ADALINE processing unit. First, the controller subtracts the estimated capacitor voltage of each sub-module from the reference capacitor voltage, v_{C}^*. The resulting errors are passed to simple proportional (P) controllers. The outputs from the P-controllers are multiplied by the sign of their corresponding arm current to form reference signals for balancing the voltage across capacitors, $v_{\text{cul\_bal}}, \ldots, v_{\text{cuN\_bal}}, v_{\text{cll\_bal}}, \ldots, v_{\text{clN\_bal}}$. Finally, to form the modulating signal for a sub-module, which is

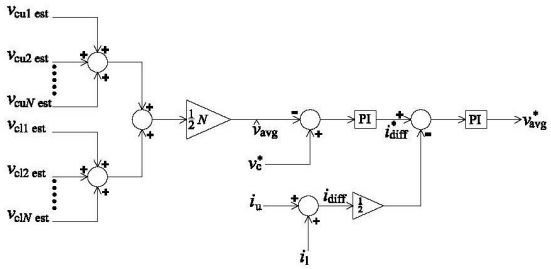

Fig. 6. Block diagram of the averaging controller.

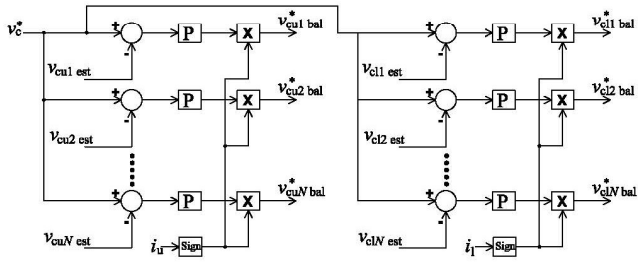

Fig. 7. Block diagram of the balancing controller.

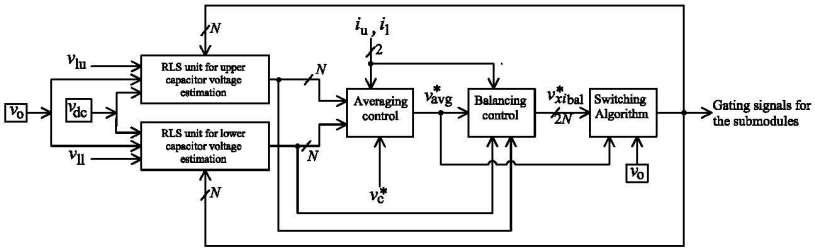

Fig. 8. Block diagram of the proposed MMC controller.

the balancing control signal for this sub-module, the average voltage command, v^*_{avg}, and the reference phase voltage, v^*_o, are all added. The PS-PWM technique is then utilized to generate the switching signals for the sub-modules of the MMC [20]. Fig. 8 illustrates a block diagram of the proposed integrated control system of the MMC. It is obvious that the proposed scheme eliminates the need for massive numbers of voltage sensors for the sub-module capacitors and their associated communication system with the central controllers. Consequently, the proposed strategy renders its application for an MMC system with a large number of sub-modules.

IV. Simulation Results and Discussions

The proposed control scheme for the MMC is simulated using PSCAD/EMTDC software package. The system parameters are shown in Table I. Different simulation cases are considered to examine the dynamic performance of the proposed control strategy for the MMC under different operating conditions. Primarily, the first task is dedicated to performance evaluation of the proposed ADALINE algorithm in order to estimate capacitor voltages used for controlling the MMC under dynamic reference phase voltage changing conditions. The second case is devoted to assessing the dynamic performance of the proposed control strategy during the boost operation of the MMC. Finally, the third case examines the capabilities of the proposed strategy for estimating capacitor voltages under fault conditions in a sub-module, and for determining the faulty sub-module.

TABLE I
MMC Model Parameters

Parameter	Value
Rated power	1 MW
Sub-module rated voltage	2,250 V
Rated DC voltage	4,500 V
Arm inductance	3 mH
Sub-module capacitance	1,900 μF
Number of sub-modules per leg	8
Load impedance	30 Ω, 6 mH

A. Dynamic Performance of the Proposed Capacitor Voltage Estimation Based Balancing Strategy

The purpose of this simulation case is to examine the performance of the proposed capacitor voltage estimation based control algorithm for the MMC under dynamic changes occuring in reference phase voltages. The reference capacitor voltage v^*_c is set at $v_{dc}/N = 2.25$ kV while the reference phase voltage signal v^*_o is dynamically changed from 0.7 p.u. to 1 p.u. at $t = 0.2$ s. First, the estimation units for capacitor voltages are disabled and the actual measurements are used in the control system. The three-phase voltages, currents, and capacitor voltages are shown in Fig. 9. A similar result to Fig. 9 is obtained in Fig. 10 where the proposed estimation unit for the capacitor voltages is enabled and utilized in the proposed control system shown in Fig. 8. As displayed in Fig. 10(a), the measured three-phase AC voltages follow their reference signals. As expected, only six sub-modules are utilized when $v^*_o = 0.7$ p.u., while all the sub-modules are involved when $v^*_o = 1$ p.u. The three-phase load currents are displayed in Fig. 10(b). Fig. 10(c) traces the capacitor voltages that are grouped in two main trajectories, one for the upper arm and the other for the lower arm. These two trajectories are out of phase and are identical to that presented in Fig. 9(c), where the measured capacitor voltages are used instead of their estimated signals in controlling the MMC. The proposed MMC controller succeeds

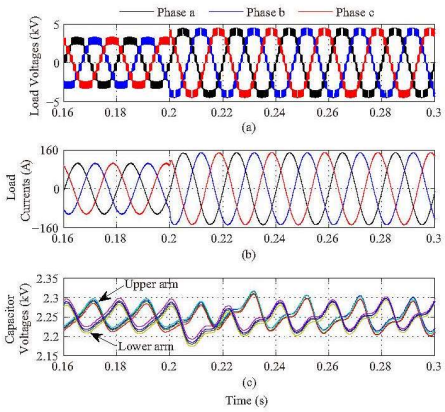

Fig. 9. Disabling the proposed estimation unit. (a) Three-phase voltages. (b) Three-phase load currents. (c) Voltages of leg a sub-modules.

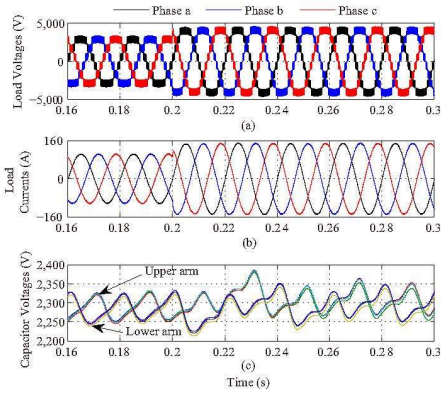

Fig. 10. Enabling the proposed estimation unit. (a) Three-phase voltages. (b) Three-phase load currents. (c) Voltages of leg a sub-modules.

in balancing the capacitor voltages at their reference value of 2.25 kV. Moreover, the estimated capacitor voltages and their corresponding actual measurements for the upper and lower arms are presented in Fig. 11 and Fig. 12, respectively.

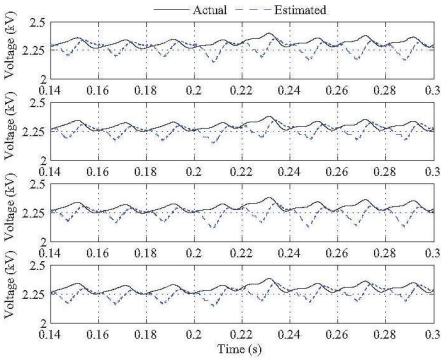

Fig. 11. Actual and estimated voltages of the upper arm sub-modules of phase a.

Fast tracking with accurate performance of the proposed ADALINE algorithm for estimating the sub-module capacitor voltages are evident. Furthermore, the circulating current is tightly tracking its reference signal, as demonstrated in Fig. 13(a). Fig. 13(b) and Fig. 13(c) illustrate the actions of the averaging controller in Fig. 6 and the balancing controller in Fig. 7 for the first sub-module at the upper arm $v^*_{\mathrm{cu1\,bal}}$, respectively. These results reveal efficient utilization of the proposed capacitor voltage estimation techniques for the MMC's control algorithm.

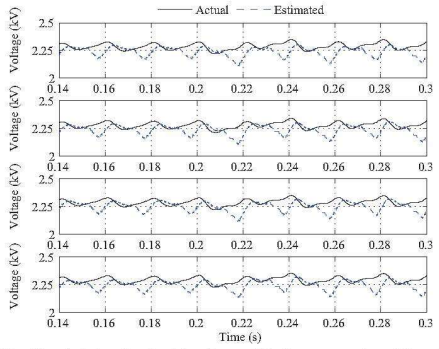

Fig. 12. Actual and estimated voltages of the lower arm sub-modules of phase a.

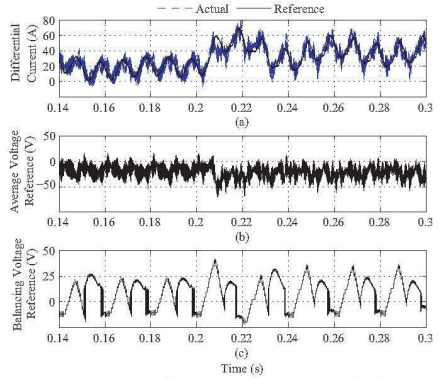

Fig. 13. Different controllers action for leg a. (a) Actual and reference waveform of the circulating current. (b) Averaging voltage reference. (c) Balancing voltage reference for the first sub-module of the upper arm.

B. Dynamic Performance During Boost Operation of MMC

In this test scenario, the reference phase voltage signal v^*_{o} is kept at 1 p.u., and the capacitor reference voltage command is increased from 2.25 kV to 2.5 kV at $t = 0.4$ s. Setting v^*_{c} at values higher than v_{dc}/N results in boost operation of the MMC, which is useful in compensating for the load voltage during sub-module faults.

Fig. 14(a) indicates increase in output three-phase voltages from the MMC at $t = 0.4$ s when the proposed controller succeeds in boosting and balancing the capacitor voltages at the new set value of 2.5 kV, as illustrated in Fig. 14(c). Yet again, the fast dynamics that tolerates error of the proposed capacitor voltage estimation units are revealed in Fig. 15 and Fig. 16 for the sub-modules at both upper and lower arms, respectively. Boosting the capacitor voltages increases the circulating current, and hence the balancing voltage signal escalates, as demonstrated in Fig. 17.

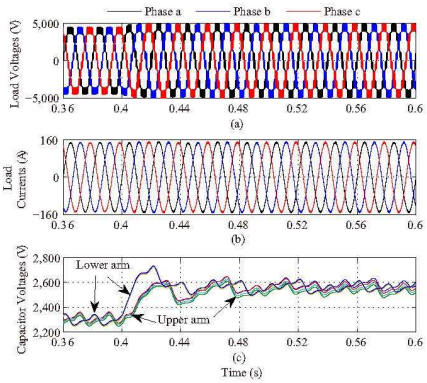

Fig. 14. Boost operation of the MMC. (a) Three-phase voltages. (b) Three-phase load currents. (c) Voltages of leg a sub-modules.

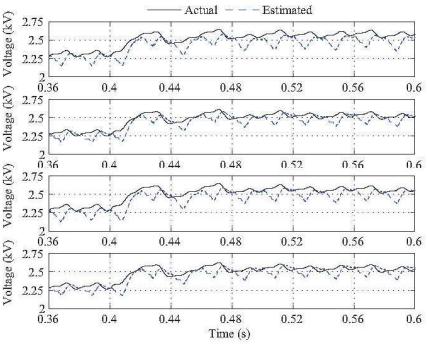

Fig. 15. Actual and estimated voltages of the upper arm sub-modules of phase a during the boost operation.

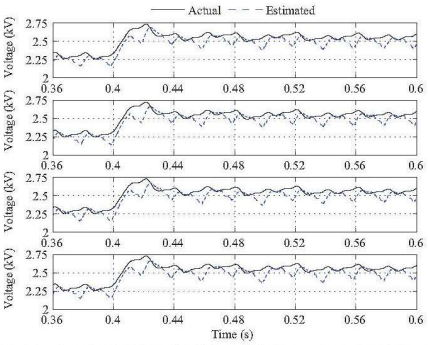

Fig. 16. Actual and estimated voltages of the lower arm sub-modules of phase a during boost operations.

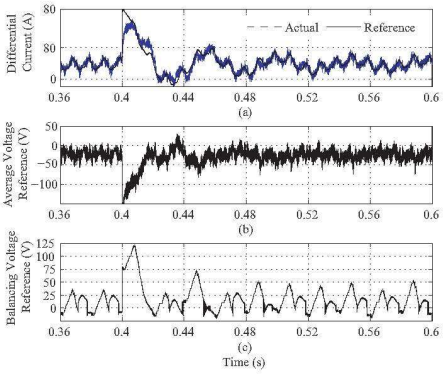

Fig. 17. Different controller actions for leg a during the boost operation. (a) Actual and reference waveform of the circulating current. (b) Averaging voltage reference. (c) Balancing voltage reference for the first sub-module of the upper arm.

C. Performance Under Sub-module Fault

This task is devoted to assessing the capabilities of the proposed strategy for estimating capacitor voltages under fault conditions in a sub-module. A short-circuit fault is programmed to strike the upper switch of the third sub-module in the upper arm of phase a at $t = 0.8$ s. As a result, the voltage and current of phase a are distorted, as shown in Fig. 18(a) and Fig. 18(b), respectively. Fig. 18(c) indicates the collapse of the DC voltage of the faulty sub-module to zero at the fault instance. Consequently, the voltages of the

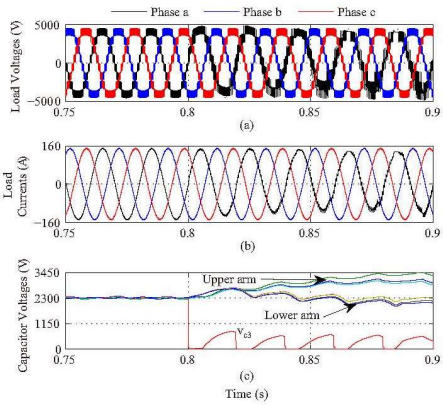

Fig. 18. Operation during a fault on the third sub-module of the upper arm. (a) Three-phase voltages. (b) Three-phase load currents. (c) Voltages of leg a sub-modules.

upper arm capacitors increase due to voltage drop in the faulty sub-module, while the voltages of the lower arm capacitors oscillate around the set value.

Fig. 19 and Fig. 20 demonstrate the fast dynamic response of the proposed ADALINE algorithm for estimating the DC voltages of different sub-modules. This result reveals that the proposed ADALINE algorithm succeeds in determining the faulty sub-module where the greatest deviation of the estimated capacitor voltage occurs. As a result, the proposed estimation unit is a candidate for sub-module fault detection and localization, which are essential tasks for fault-tolerant control of the MMC. During the fault, the circulating current, averaging, and balancing control signals oscillate with the power frequency component, as illustrated in Fig. 21.

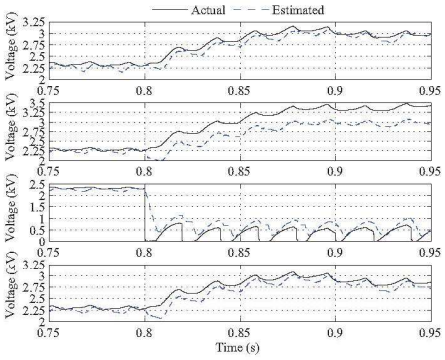

Fig. 19. Actual and estimated voltages of the upper arm sub-modules of phase a during a fault on the third sub-module of the upper arm.

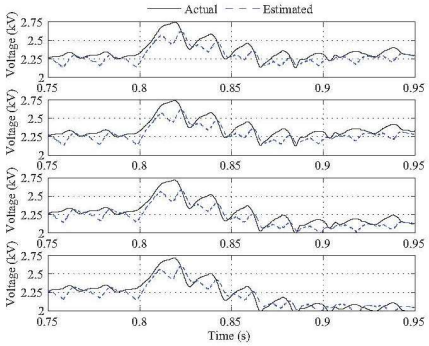

Fig. 20. Actual and estimated voltages of the lower arm sub-modules of phase a during a fault on the third sub-module of the upper arm.

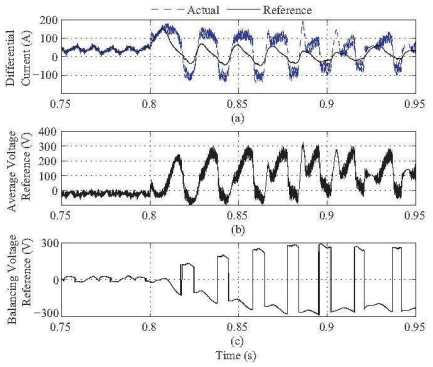

Fig. 21. Different controller actions for leg a during the faulty sub-module. (a) Actual and reference waveform of the circulating current. (b) Averaging voltage reference. (c) Balancing voltage reference for the first sub-module of the upper arm.

V. Conclusion

This paper presents an estimation unit based on the ADALINE algorithm for the sub-module DC voltages of the MMC. For each leg of the MMC, the proposed estimation unit requires only three sensors: one for the phase voltage and the other two for the voltages across the arm reactors. The proposed estimation unit is then integrated into a control strategy to balance the voltages across the sub-modules of the MMC. The proposed technique eliminates the need for direct measurement of capacitor voltages and associated communication systems, which renders it suitable for implementing a low-cost centralized controller for the MMC with a large number of sub-modules. The fast response and accurate tracking of the estimation unit under different dynamic conditions are validated in simulation results. Furthermore, the proposed MMC controller successfully balances the capacitor voltages at their set values even in boost operation mode. Finally, the circulating current is able to tightly track its reference signal, and the results demonstrate that the proposed ADALINE algorithm is able to successfully determine the faulty sub-module, which is required for implementing fault-tolerant control of the MMC.

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An Integrated Control Strategy with Fault Detection and Tolerant Control Capability Based on Capacitor Voltage Estimation for Modular Multi-Level Converters

Mahmoud Abdelsalam, *Member, IEEE*, Mostafa I. Marei, *Senior Member, IEEE* and Sarath Tennakoon, *Member, IEEE*

***Abstract*—Modular Multilevel Converter (MMC) will be extensively used in High-Voltage Direct Current (HVDC) transmission networks because of its superior characteristics over Line Commutated Converter (LCC). Increasing the reliability of the MMC is directly related to the balancing of the MMC sub-module capacitors voltages which guarantees the proper operation of the converter and lowers the stress on the sub-modules. This paper presents an adaptive voltage balancing strategy based on capacitor voltage estimation utilizing a hybrid ADALINE-RLS scheme. The proposed strategy eliminates the need of measuring sub-modules capacitor voltages and associated communication link with the central controller. Furthermore, the estimated capacitor voltages are utilized to detect and localize different types of sub-module faults. After isolating the faulty sub-modules, the proposed fault tolerant control unit (FTCU) modifies the parameters of the voltage balancing strategy to overcome the reduction of the active sub-modules. The dynamic performance of the proposed strategy is investigated, using PSCAD/EMTDC simulations and hardware in the loop (HIL) real-time simulations, under different normal and faulty operating conditions. The accuracy and the time response of the proposed fault detection and tolerant control units result in stabilizing the operation of the MMC under different types of faults. Consequently, the proposed integrated control strategy improves the reliability of the MMC.**

***Index Terms*—Balancing control, fault detection, fault tolerant control, modular multilevel converter, voltage estimation.**

I. Introduction

VOLTAGE Source Converters (VSC) are increasingly being used in high-voltage direct current (HVDC) transmission systems, in particular for the grid connection of off-shore wind farms, due to their advantages over the line commutated converters (LCC). These include: the ability to control active and reactive power independently, the ability to supply weak or passive networks and the lower footprint. Although the VSCs have many topologies, the modular multilevel converter (MMC) is considered to be the most suitable topology for high voltage applications, in particular for power transmission and distribution due to their features such as: the possibility to eliminate harmonic filters with a sufficient number of voltage levels, elimination of the dc-link capacitor and low switching losses [1][2].

The voltage balancing process is vital for proper operation of the MMC and to keep the power quality at the standard level [3-5]. Many capacitor voltage balancing techniques have been proposed in literature. However, few of them are considered to be practical and suitable for the control of industrial MMCs. One of the promising techniques is the arm energy control technique. The philosophy behind this technique is to control the energy stored in the whole leg and the difference of stored energy between the upper and lower arms [6]. Despite the accurate performance of this method, it suffers from many drawbacks such as distortion of the output current and the complexity of implementation due to large number of calculations. In addition, the arm energy control technique needs continuous measurements of large number of signals. Another capacitor voltage balancing strategy, proposed in [7], is based on regulating the capacitor voltage in each sub-module independently at the set value through monitoring the capacitor voltage of each sub-module [7]. Although the performance of this method is more attractive compared to the energy control, it has a main drawback of high value of differential current. Moreover, it needs the continuous measurements of capacitor voltages.

The reliability of MMC can be improved by implementing a voltage balancing strategy with fault detection and fault tolerant control capabilities that enable the converter to be operated under fail-to-safe operation principle with satisfactory performance [8][9]. Classifying the faults, which the MMC sub-modules may be subjected to, is considered to be the first step in implementing the fault detection and diagnosis algorithm. The sub-module is considered to be building unit in the MMC and it may be exposed to different fault types, that threaten the safety and reliability of the MMC, such as open-circuit or short-circuit faults of switches or capacitors [10] [11]. A survey presented in [12] states that 30% of failures caused in power electronic converters are due to the switching devices such as IGBTs and diodes. Based on this statement, the quick detection and localization of IGBT faults is a necessity and can significantly increase the reliability of the MMC. In [12], a hardware based technique is proposed for detecting IGBTs faults. This technique depends on measuring the rate of change of the collector current and comparing it with a pre-defined threshold. The cost of this method is extremely high since each IGBT has a sophisticated monitoring circuit [12]. Another method presented in literature depends on the charge rate of the gate voltage which offers a better sensitivity but still has a high cost impact due to the need of having a dedicated hardware circuit [13]. The artificial neural network (ANN) is used to analyze the historical data of the MMC output voltage and current. Although this method is based on computations and does not need extra physical components, its accuracy is not guaranteed if the voltage and current levels are changed due to dynamic changes. Moreover, the training of the ANN consumes a lot of effort and does not cover all cases [14].

The objective of the fault tolerant control system is to overcome the effect of the presence of faulty sub-module and restoring the stability of the power electronics converter with acceptable performance level. The concept of fault tolerant control is gaining a lot of research interest especially for the MMC, due to the vulnerability of the converter to various types of faults. Additionally, it is not accepted to disconnect the MMC during the operation to assure the security of supply [15]. The fault tolerant control system can be conducted by either using redundant sub-modules or redundant IGBTs as described in [16] and [17], respectively. In addition, other fault tolerant control techniques based on hardware circuits to modify the MMC control system are presented in [18].

The majority of the voltage balancing, fault detection and fault tolerant control techniques proposed in literature require reliable measurements of the capacitor voltages which increases the MMC cost. Moreover, there is no much research has been performed to provide centralized control systems for the MMC in normal and abnormal conditions and utilizes the concept of fault tolerance. This paper presents a new voltage balancing control technique with fault detection and fault tolerant control capability based on capacitors voltage estimation instead of direct measurement. The main contribution of the proposed technique is the elimination of the communication burden used to send the voltage measurements from sub-modules to the central controller. As a result, not only the cost is reduced, but the wiring and its associated problems is minimized which renders the proposed strategy attractive for the practical realization of a MMC with a large number of sub-modules. Another important contribution is that the central MMC controller has fault detection and tolerant control capability without the need of redundant sub-modules or adding special power circuit. Various case studies are conducted and presented to evaluate the dynamic performance of the proposed integrated control strategy under different operating conditions. The rest of this paper is organized as follows. The operation concept, the mathematical analysis and the switching algorithms of the MMC are described in section II. Section III presents two capacitor voltage estimation techniques that are used in the proposed MMC control system. The proposed capacitor voltage balancing technique is explained in section IV. Section V clarifies the proposed fault detection and tolerant control strategies. The results obtained from simulation and Hardware In the Loop (HIL) are provided with discussions in sections VI and VII, respectively. Finally, Section VIII concludes the paper.

II. The Operation Principle of MMC

Generally, the operation of the MMC depends on the switching of the sub-module IGBTs. The switching is performed through a switching algorithm which generates the firing signals to each sub-module [19].

A. The structure of the MMC

The MMC consists of sub-modules connected in series forming a leg in each phase. The sub-module can be a half-bridge or a full-bridge and each sub-module has a capacitor which buffers the energy from the dc to the ac side and vice versa, thus the dc-link capacitor is eliminated. A high speed bypass switch is connected to the output port of the sub-module to isolate it in case of fault occurrence. As shown in Fig.1, each phase leg is divided into two arms upper and lower. Each arm has an identical number of sub-modules to generate balanced voltage between the two arms of each phase. Inductors are installed in arms to smooth and filter the currents [20] [21].

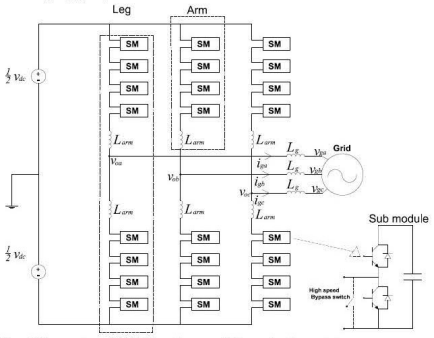

Fig. 1 Three-phase MMC topology and internal sub-module.

B. The MMC mathematical model

For the purpose of designing an inner control system for the MMC, it is necessary to mathematically analyze the converter. The converter arms are represented as variable capacitors connected in series with the arm resistance and inductance [6]. The number of sub-modules per arm and the switching frequency are assumed infinite to simplify the analysis because of the perfect sinusoidal output voltage and total voltage balancing between arms. The arm capacitance insertion is represented with a modulation value $m_{arm\,x}$, where x may be u for upper arm or l for lower arm. The $m_{arm\,x}$ is varied from 0 to 1. For example, when $m_{arm\,u} = 0$, this indicates that all sub-modules in the upper arm are bypassed and when $m_{arm\,l} = 1$, this indicates that all sub-modules in the lower arm are inserted. The value Σv_{Cx} is the sum of arm capacitors voltages. The arm voltage is given by:

$$v_x(t) = m_{arm\,x}(t).\Sigma v_{Cx} \quad (1)$$

The inserted arm capacitance is given by:

$$C_{insx} = \frac{C_{SM}}{N.m_{arm\,x}(t)} \quad (2)$$

where C_{SM} is the capacitance of one sub-module and N is the number of sub-modules per arm. If the arm current as $i_x(t)$, the total capacitor voltage dynamics can be expressed by:

$$\frac{d\Sigma v_{Cx}}{dt} = \frac{i_x(t)}{C_{ins\,x}} \quad (3)$$

Substituting (2) in (3), the capacitor voltage dynamics can be expressed for the upper and lower arms by:

$$\frac{d\Sigma v_{Cu}}{dt} = \frac{N.m_{arm\,u}.i_u}{C_{SM}} \quad (4)$$

$$\frac{d\Sigma v_{Cl}}{dt} = \frac{N.m_{arm\,l}.i_l}{C_{SM}} \quad (5)$$

The current i_{diff} is the differential current which circulates between the phase legs. The circulating current of any phase is described as follows:

$$i_{diff} = \frac{i_u + i_l}{2} \quad (6)$$

By performing the necessary circuit analysis, the output phase voltage v_o is given by:

$$v_o = \frac{v_{dc}}{2} - L_{arm}\frac{di_u}{dt} - m_{arm\,u}\Sigma v_{Cu} \quad (7)$$

$$v_o = -\frac{v_{dc}}{2} + L_{arm}\frac{di_l}{dt} + m_{arm\,l}\Sigma v_{Cl} \quad (8)$$

C. The MMC switching algorithm

Many switching algorithms have been proposed in literature [22-25]. The modulation techniques that has been used can be divided to two main categories: reference signal based and carrier based. The phase shifted pulse width modulation (PS-PWM), which is one of the well-known carrier based technique, is utilized due to its ease of implementation, reduced switching frequency and hence switching losses. Moreover, the PS-PWM is characterized by stable performance during dynamic changes [26].

In the PS-PWM technique, each sub-module has a dedicated triangular carrier waveform with the same magnitude but with a different phase shift. The switching signals for a sub-module result from comparing its corresponding carrier wave with the sinusoidal voltage reference signal v_o^*. The phase shift between each consecutive carrier signals is given by:

$$\theta = \frac{360}{N-1} \tag{9}$$

III. Estimation of Capacitor Voltages

The capacitor voltage estimation is the extremely important step of the proposed control strategy. Although the capacitor voltage estimation eliminates the use of direct measurements, it is a must to assure the estimation accuracy to avoid wrong control actions. Two capacitor voltage estimation techniques are presented. The first is achieved by using the adaptive linear neuron (ADALINE) algorithm which is needed in the proposed fault detection algorithm, while the second algorithm is the recursive least squares (RLS) algorithm which is used in the proposed capacitor voltage balancing control strategy and the proposed fault detection algorithm as well.

A. The capacitor voltage estimation using ADALINE technique

The capacitors voltages estimation is performed by utilizing the Adaptive Linear Neuron (ADALINE) algorithm. The ADALINE is known as being a very efficient and quick on-line tracking technique for the tracking of dynamically changing voltage signals. It is utilized in many applications because of its robust performance, low calculation burden and accurate results [27] [28]. The ADALINE algorithm is formed by simple calculations that do not consume large computing time which is very important in the application of capacitor voltage estimation. To estimate the capacitors voltages, the MMC governing equations given by (7) and (8) are rearranged and rewritten in the vector form as follows:

$$\frac{v_{dc}}{2} - v_o - v_{Lu} = [S_{u1} \quad S_{u2} \quad \dots \quad S_{uN}] \begin{bmatrix} v_{cu\_est} \\ v_{cu2_{est}} \\ \vdots \\ v_{cuN_{est}} \end{bmatrix} \tag{10}$$

$$\frac{v_{dc}}{2} + v_o - v_{Ll} = [S_{l1} \quad S_{l2} \quad \dots \quad S_{lN}] \begin{bmatrix} v_{cl1\_est} \\ v_{cl2\_est} \\ \vdots \\ v_{clN\_est} \end{bmatrix} \tag{11}$$

where S_{xi} is the switching state for the i^{th} sub-module, $v_{Lu} = L_{arm}\frac{di_u}{dt}$, and $v_{Ll} = L_{arm}\frac{di_l}{dt}$

To eliminate the effect of the arm inductance on the estimation accuracy, the arm inductor voltages are measured and used in (10) and (11) for the proposed capacitor voltage estimation techniques. In turn, the proposed capacitor voltage estimation unit does not require the knowledge of the circuit parameters.

The ADALINE algorithm produces a linear combination of its input vector $X(k)$ which represents the switching state vector $[S_{x1} \quad S_{x2} \quad \dots \quad S_{xN}]^T$ at time k, where the suffix T refers to the transpose operation. In this technique, the input vector is multiplied by the weight vector $W(k)$ which resembles the estimated capacitors voltages, given in (10) and (11), to produce the predicted linear output $\hat{y} = X^T W(k)$. The next step is computing the error signal and adjusting the weights to eliminate the error using the delta rule, also known as Widrow-Hoff learning rule, which is given by [29]:

$$W(k+1) = W(k) + \alpha \frac{X(k)(y(k) - \hat{y}(k))}{X(k)^T X(k)} \tag{12}$$

where α is the reduction factor, it is observed that increasing this factor increases the convergence speed on account of losing stability as the prediction error may increase dramatically. The reduction factor α is set at 0.002, for this application, to minimize the error and hence to guarantee system stability [30]. When the difference between the measured signal $y(k)$ and the estimated signal $\hat{y}(k)$ converges to zero, the ADALINE algorithm decomposes the signal and estimates the capacitors voltages. It is worth mentioned that the proposed capacitors voltages estimation unit is based on three voltage sensors per phase to measure the voltage across the arm reactors and the output phase voltage. This action enables the implementation of a low cost centralized controller for the MMC with a large number of sub-modules since the voltage measurement of sub-modules and their associated communication link are eliminated.

B. The capacitor voltage estimation using RLS technique

The fundamental RLS algorithm is formed by two basic equations. The first equation, given in (13), is to update the estimate vector $\hat{\theta}(k)$ of the sub-modules capacitor voltages, while the second equation is used to update the weighting matrix $P(k)$ as shown in (14).

$$\hat{\theta}(k) = \hat{\theta}(k-1) + P(k)\hat{\theta}(k)\left[y(k) - \phi(k)^T\hat{\theta}(k-1)\right] \tag{13}$$

$$P(k) = \frac{1}{\lambda}\left[P(k-1) - \frac{P(k-1)\phi(k)\phi(k)^T P(k-1)}{\lambda + \phi(k)^T P(k-1)\phi(k)}\right] \tag{14}$$

where $\phi(k)$ is the connection vector which represents the switching state vector $[S_{x1} \quad S_{x2} \quad \dots \quad S_{xN}]^T$ at time k and λ is the forgetting factor that controls the speed of updating the weight matrix in (14). The result of multiplying $\phi(k)^T$ by $\hat{\theta}(k-1)$ gives the predicted output, $\hat{y}$ [31]. This predicted signal is then subtracted from the measured signal and the error is used to update the estimate vector. When the estimation error approaches zero, the convergence is reached and the estimated sub-module capacitor voltages are ready. It is clear that the calculation burden of the RLS is slightly more than the ADALINE; however, the RLS is characterized by its fast dynamic response. Fig. 2 illustrates the general block diagram of the capacitor voltage estimation and the process of updating the capacitor voltages.

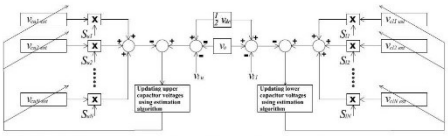

Fig.2: Block diagram of capacitor voltage estimation unit.

IV. The Proposed Control Strategy for the MMC

One of the main advantages of the proposed control strategy for the MMC is that it has the same structure for normal condition operation and for the proposed fault tolerant control. The proposed control strategy for the MMC is divided to two main controllers, the averaging controller and the balancing controller for the capacitors' voltages. The following subsections detail each controller.

A. The averaging controller

The averaging controller is formed from two cascaded loops that are responsible of controlling the average voltage across one leg [7]. As shown in Fig. 3, the outer loop sets the reference signal for the differential current, i^*_{diff}, using a simple PI controller to process the error between the estimated average voltage using the RLS algorithm, $\hat{v}_{avg} = (\sum v_{cui\ RLS} + \sum v_{cli\ RLS})/2N_{eff}$, and the desired reference capacitor voltage v^*_C, where N_{eff} is the number of effective sub-modules connected in the arm. The inner loop restrains the differential current, calculated from (6), at its reference signal by utilizing another PI controller that generates the averaging voltage signal, v^*_{avg}.

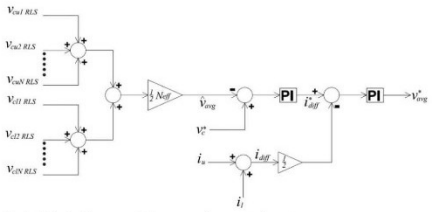

Fig.3: Block diagram of the averaging control system.

B. The balancing controller

The balancing controller is a centralized control system that generates reference signals to balance the voltage across the sub-modules capacitors based on the estimated voltages from the ADALINE processing unit as demonstrated in Fig. 4.

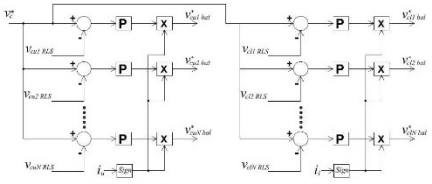

Fig.4: Block diagram of the balancing control loops.

Firstly, the error between the estimated capacitor voltage and the reference capacitor voltage is calculated for each sub-module. Simple proportional (P) controllers process these errors. The actions of the P-controllers are multiplied by the sign of their corresponding arm current to form reference signals for balancing the voltage across capacitors, v_{cul_bal}, … ,v_{cuN_bal}, v_{cll_bal}, … , v_{clN_bal}.

Finally, the modulating signal for a sub-module is formed by adding the balancing control signal for this sub-module, the average voltage command, v^*_{avg}, and the reference phase voltage, v^*_o, together. The PS-PWM technique is utilized to generate the switching signals for the sub-modules of the MMC [32]. Fig. 5illustrates a block diagram of the proposed integrated control system of the MMC. It is obvious that the proposed scheme eliminates the need of massive numbers of voltage sensors for the sub-module capacitors and their associated communication system with the central controllers. Consequently, the proposed strategy renders its application for a MMC system with a large number of sub-modules.

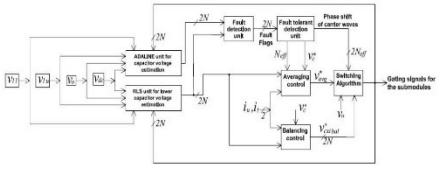

Fig.5: Block diagram of the proposed MMC control strategy.

V. The Proposed Fault Detection and Diagnosis Algorithm

The proposed fault detection algorithm, illustrated in Fig. 6, is designed based on the reduction percentage of the estimated per-unit voltage and the rate of change of the difference between the estimated voltages from the ADALINE and the RLS algorithms for each sub-module.

The proposed fault detection unit (FDU) receives the RLS estimated sub-module capacitor voltages $v_{cxi\ RLS}$ from the RLS algorithm, where $x = u$ or l and $i = 1,2,3\ldots..,N$. The estimated values are divided by the reference capacitor voltage v^*_C to obtain the per-unit values $v_{cxi\ RLS\ pu}$. Instantaneously, the error between the ADALINE and RLS estimated capacitor voltages of each sub-module is calculated and passed to a high speed differentiator to calculate the rate of change of the error signals $\frac{de_{xi}}{dt}$. It is worthy mentioned that the proposed FDU is based on the difference between the dynamic behaviors of the ADALINE and RLS algorithms results from their different natures. Consider the Widro-Hoff rule, (12), which is used for the ADALINE to update estimated voltages. At each iteration, the weighting vector $W(k+1)$ is updated by adding the error reduction component $\alpha\frac{X(k)(y(k)-\hat{y}(k))}{X(k)^T X(k)}$ to the previous value, $W(k)$. This action indicates that the ADALINE algorithm has no memory because of the independence of the Widro-Hoff rule on the accumulative value of weighting vector. Moreover, the reduction factor α controls the convergence speed; a high value of α increases the convergence period. Therefore, the ADALINE algorithm is characterized by fast tracking under sudden changes of the capacitor voltages. However, it needs relatively long time until reaching convergence. Unlike the ADALINE algorithm, the process of updating the weighting vector of the RLS algorithm depends on the accumulation of historic values of the capacitor voltages as demonstrated in equations (13) and (14). As a result, the RLS algorithm is characterized by lower convergence time when compared with the ADALINE algorithm. However, in the incident of having a sudden change in the capacitor voltage, which occurs during sub-module faults, the dynamic response of the RLS algorithm is slower than that of the ADALINE algorithm.

The next step is to check the estimated per-unit voltage signal, for each sub-module, whether it is higher than 85% or

not. If the comparison result is true, the sub-module is considered to be in healthy condition. Otherwise, the FDU compares the rate of change of the error signal with a predefined threshold which is selected based on the required sensitivity. If the rate of change of the error signal exceeds the threshold, the FDU considers the corresponding sub-module in faulty condition. However, a counter is used to ensure that the steadiness of the estimated signals for a continuous ten counts before indicating a faulty sub-module by setting its corresponding flag, f_i. It is worthy mentioned that the execution time of the proposed FDU is assumed 100 μs; hence the minimum detection time is 1 ms.

The reliability and robustness of the proposed FDU result from its hybrid operation where the fault decision is not only based on the reduction on the estimated per-unit voltage but also on the rate of change of the difference between the estimated voltages from the proposed ADALINE and RLS techniques. The difference between the dynamic behaviors of the two proposed estimation techniques results from their different adaption rules. Moreover, this method does not need any extra components or devices as it is based on the estimation algorithms that are simultaneously utilized in the proposed control of the MMC.

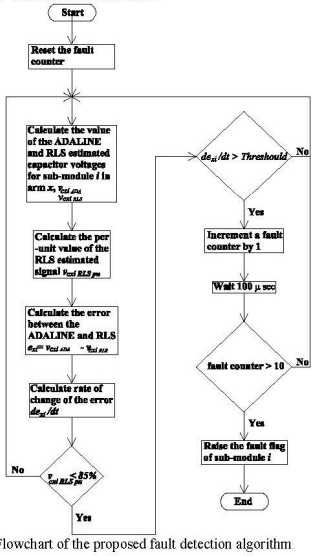

Fig.6: Flowchart of the proposed fault detection algorithm

VI. The Proposed Fault Tolerant Control Strategy

The proposed fault tolerant control unit (FTCU) has two main tasks: the first is to isolate the faulty sub-modules while the second is to modify the capacitor balancing algorithm. The proposed FTCU, presented in Fig. 7, utilizes the flags of the faulty sub-modules set by the FDU. Assume that there is a fault in one sub-module in the upper arm, the fault tolerant control strategy isolates the faulty sub-module and another one in the lower arm by activating the bypass switches and disabling their gating signals. The reason of isolating a healthy sub-module in the adjacent arm is to retrieve the energy balance between the two arms by equating the number of the activated sub-modules in the upper and lower arms.

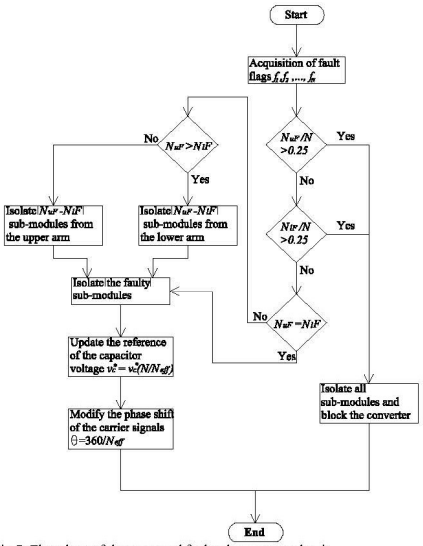

Fig.7: Flowchart of the proposed fault tolerant control unit.

As a result, the capacitor reference voltage v_C^* is boosted, by the gain $\frac{N}{N_{eff}}$, to compensate for the reduced number of sub-modules, while keeping the desired output voltage. At the same time, the proposed FTCU modifies the phase shift between the carrier signals for the rest of the sub-modules in the leg according to (9). This strategy is designed to permit the converter to continue its operation provided that the number of faulty sub-modules per arm does not reach a pre-defined value based on the number of sub-modules and the ratings of the devices. Otherwise, the control system considers the MMC suffering from cascading failure and in this case, it isolates all the sub-modules and deactivates the converter. It is important to mention that the sub-module capacitor must be carefully selected taking into consideration the worst case condition at which the maximum number of faulty sub-module can be tolerated. This can be done by calculating the maximum energy variation, the boosted up capacitor voltage level and the allowable voltage ripples and selecting the capacitor value from [33]:

$$C_{SM} > \frac{2\,\Delta e_{p\,max}}{N_{eff} V_c^2 \left(1+k_{ripple\,max}\right)^2} \quad (15)$$

where V_c is the rated capacitor voltage, $k_{ripple\,max}$ is the maximum allowable ripple percentage and $\Delta e_{p\,max}$ is the maximum energy variation.

VII. Simulation Results and Discussions

The proposed control scheme for the MMC is simulated using PSCAD/EMTDC software package. The system parameters are shown in Table 1. Different simulation cases are considered to examine the dynamic performance of the proposed control strategy for the MMC under different operating conditions. Moreover, the dynamic behavior of the proposed FDU is tested under different healthy and faulty condition. Primarily, the first task is dedicated to evaluate the performance of the proposed scheme based on the RLS

algorithm to estimate the capacitors voltages used to control the MMC under the dynamic reference phase voltage changing condition. The second case is devoted to assessing the dynamic performance of the proposed fault detection and fault tolerant control units during open-circuit fault in a sub-module. Finally, the third case examines the capabilities of the proposed FDU and FTCU to stabilize the operation of the proposed control strategy for the MMC under short-circuit fault in a sub-module.

TABLE I
MMC MODEL PARAMETERS

MMC model parameters	
Rated power	1 MW
Sub-module rated voltage	2250 V
Rated dc Voltage	9000 V
Arm inductance	3 mH
Sub-module capacitance	1900 µF
Number of sub-modules per leg	8

A. Performance under IGBT open circuit fault

This task is devoted to assess the capabilities of the proposed control strategy and FDU under IGBT open circuit fault in a sub-module. The upper switch of the third sub-module in the upper arm of phase *a* is intentionally opened at *t= 0.5s*. The fault detection and fault tolerant control units are enabled. The FDU succeeds to detect and localize the fault after 33 ms from its instant of activation as illustrated in Fig 8(a). With the slaw rate of increase of the capacitors voltages, the 33 ms period of detecting open-circuit fault is enough to guarantee the safety of the MMC. Once the fault of the third sub-module in the upper arm is detected, the FTCU isolates it and the third sub-module in the lower arm to balance the energy between the two arms. Furthermore, the FTCU increases the v_c^* from 2.25 kV to 3 kV, as shown in Fig. 8 (b), and adjusts the phase shift of the carrier waves from 45° to 60° to compensate for the loss of two isolated sub-modules. These actions are sufficient to tolerate the fault and restore the stability of the MMC control system as appear from the results of Fig. 9 (a) and (b) where the three-phase output voltages and currents are balanced. The capacitor voltages of the remaining sub-modules restore their balance around the new desired value set by the FTCU as indicated in Fig 9 (c). As expected, the capacitor voltages are slightly increased at the moment of fault detection, t = 0.533s. It is worth mentioned that the capacitor voltages of the isolated sub-modules freeze at their values when isolation occurs.

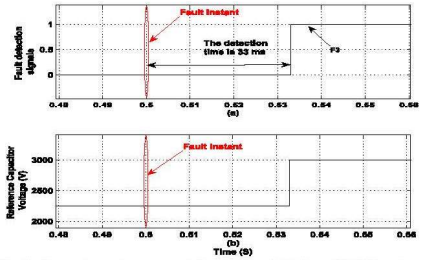

Fig. 8: Dynamic performance of the proposed FDU and FTCU under an open-circuit fault in a sub-module.

Fig. 10 and 11 indicate the actual and estimated capacitor voltages of the upper and lower arms of phase *a*, respectively. Both the ADALINE and RLS algorithms provide accurate estimate of the capacitor voltage, even during transient periods. It is obvious that the performance of the RLS algorithm is more accurate than that of the ADALINE algorithm for estimating the time-varying capacitor voltage signal. As indicated from (10) and (11), the estimation of the capacitor voltages is based on the switching signals. In turn, the proposed estimation algorithms cannot estimate the voltage of faulty or disabled sub-modules as indicated in Fig. 10(c) and Fig. 11(c). At the instant of open-switch fault, the difference between the estimated voltages from the ADALINE and the RLS algorithm increased and excites the proposed FDU to detect the fault quickly.

With the help of the FTCU, the averaging and balancing control loops are able to quickly overcome the consequences of fault and forces the differential current to reach its rated value prior the fault instant, as displayed in Fig. 12(a). Moreover, the averaging and balancing control signals retain their stability as illustrated in Fig. 12(b) and (c), respective

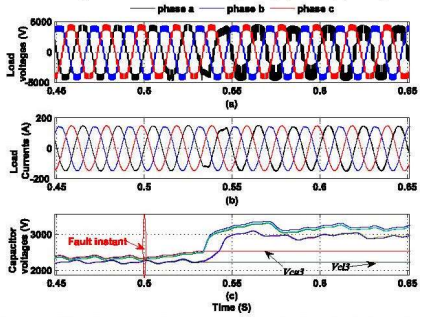

Fig. 9: Enabling the proposed FTCU for an open-circuit fault: a) Three-phase voltages, b) three- phase load currents, c) voltages of leg *a* sub-modules.

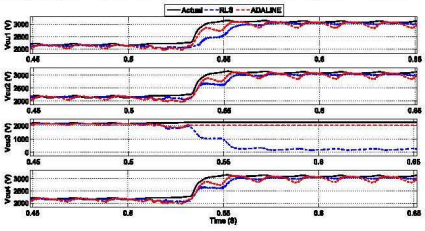

Fig. 10: Actual and estimated voltages of the upper arm sub-modules of phase *a*, under an open-circuit fault.

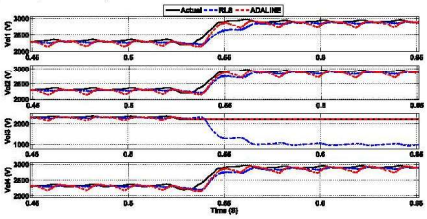

Fig. 11: Actual and estimated voltages of the lower arm sub-modules of phase *a*, under an open-circuit fault.

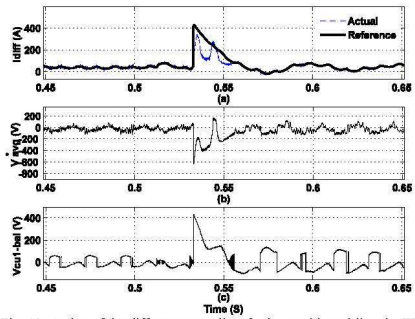

Fig. 12: Action of the different controllers for leg *a* with enabling the FTCU for an open-circuit fault: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first sub-module of the upper arm

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B. *Performance under IGBT short circuit fault*

This case is conducted to investigate the capabilities of the proposed control strategy and the FDU under IGBT short circuit fault in a sub-module. A short-circuit fault is applied to the upper switch of the third sub-module in the upper arm of phase *a* at *t= 0.5s* and the proposed FDU and FTCU are enabled. The FDU succeeds to detect and localize the short-circuit fault after 2.2 ms from its incidence as demonstrated in Fig 13 (a). This detection time is fast as the needed time for clearing short circuit faults must not exceed 5 ms [34]. At the instant of fault detection, the FTCU has isolated the faulty sub-module in the upper arm and its corresponding third sub-module in the lower arm to balance the energy between the two arms. Furthermore, the FTCU increases the v_c^* from 2.25 kV to 3 kV as displayed in Fig. 13 (b), and modifies the phase shift of the carrier waves from 45° to 60° to compensate for the loss of two sub-modules. Fig. 14 (a) and (b) show the three-phase output voltages and currents which are balanced. The capacitor voltages of the remaining sub-modules restore their balance at the new set value as illustrated in Fig 14(c).

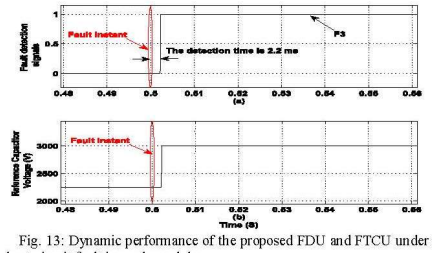


Fig. 13: Dynamic performance of the proposed FDU and FTCU under a short-circuit fault in a sub-module.

The proposed RLS and ADALINE algorithms are accurately estimating the capacitor voltages during the short-circuit fault for all healthy sub-modules as indicated in Fig. 15 and 16. Regarding the faulty sub-module, the RLS and ADALINE estimated signals are different and at the same time the RLS estimated voltage is by far below the voltage threshold. This helped the FDU to quickly detect the short-circuit fault condition. Fig. 17(a) shows that the FTCU stabilizes the operation of the averaging and balancing control loops which succeed to limit the magnitude of the differential current and to tightly track its reference. Additionally, the improved averaging and balancing control signals are portrayed in Fig. 17(b) and (c), respectively.

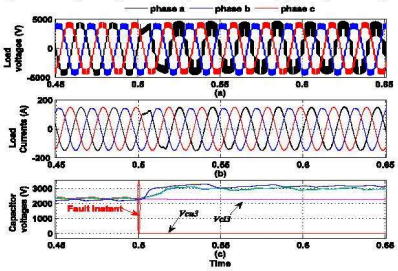


Fig. 14: Enabling the proposed FTCU for a short-circuit fault: a) Three-phase voltages, b) three- phase load currents, c) voltages of leg *a* sub-modules.

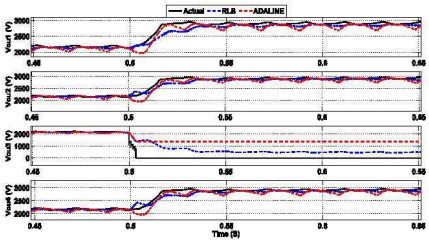


Fig. 15: Actual and estimated voltages of the upper arm sub-modules of phase *a*, under a short-circuit fault.

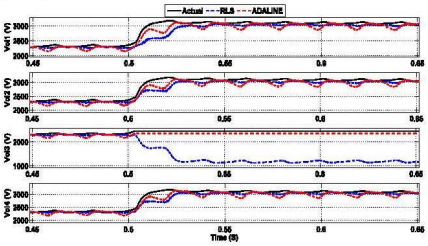


Fig. 16: Actual and estimated voltages of the lower arm sub-modules of phase *a*, under a short-circuit fault.

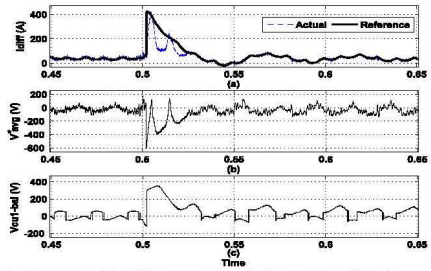
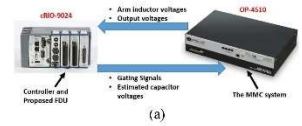


Fig. 17: Action of the different controllers for leg *a* with enabling the FTCU for a short-circuit fault: a) Actual and reference waveform of the circulating current, b) averaging voltage reference, c) balancing voltage reference for the first sub-module of the upper arm.

VIII. HARDWARE IN THE LOOP RESULTS

The HIL test platform is used to validate the proposed control method. This platform is based on the RT-LAB real-time simulation software. As shown in Fig. 18 (a), the platform consists of two main parts: the real-time digital simulator and the real-time physical controller.



(a)

(b)

Fig.18: The HIL platform system components: a) the block diagram of the HIL platform, b) the HIL test system.

The MMC with the parameters given in table I is simulated using the OP-4510 real-time digital simulator made by OPAL-RT with a CPU that operates at a time step of 25 µs. In addition, the real-time digital simulator provides the physical real time controller with needed measurements such as the ac-side voltages and currents, dc voltage, and arm currents. On the other hand, it receives gating signals for IGBTs from the physical controller. The real-time physical controller is a Virtex-5 LX based cRIO- 9024 FPGA controller, which operates at a time step of 25 ns, made by National Instruments and programmed using the LABVIEW software. The physical controller performs the proposed capacitor balancing, fault detection and tolerant control techniques, and the switching algorithm of the MMC. Fig 18 (b) illustrates the HIL test system where the gating signals and system measurements are exchanged through copper wires.

Firstly, an open-circuit fault is applied to the upper switch of the third sub-module in the upper arm of phase *a*, then after *0.3s* a short-circuit fault is applied to the first sub-module in the lower arm of phase *a* while enabling the proposed FDU and FTCU. The FDU succeeds to detect the first fault after 35.4ms as shown in Fig. 19(a). Moreover, the FDU identifies the second fault after 3.2ms as shown in Fig. 19 (b). Fig. 20(a) and (b) portray the three-phase output voltages and currents which are balanced even during the application of the two faults.

The capacitor voltages of the remaining sub-modules of the upper and lower arms restore their balance at the new set value as illustrated in Fig 21(a) and (b), respectively. Consequent to the detection of the first fault, the proposed FTCU isolates the faulty sub-module in the upper arm and its corresponding third sub-module in the lower arm to balance the energy between the two arms. Furthermore, the FTCU increases v_c^* from 2.25 kV to 3 kV to compensate for the loss of two sub-modules. After the second fault is identified, the FTCU isolates the first sub-module in the lower arm of phase *a*, which is faulty, and re-inserts the third sub-module in the same arm, which is previously bypassed as a response from the FTCU against the first fault. Hence, the energy between the two arms is always balanced and the capacitor voltages of the remaining sub-modules are regulated at the new set vale, 3KV.

The proposed RLS scheme accurately estimates the capacitor voltages during the different operating conditions as indicated in Fig. 22(a). Fig. 22(b) demonstrates that the FTCU succeeds to limit the magnitude of the differential current which is tightly tracking its reference signal. Finally, the averaging and output voltage reference control signals are portrayed in Fig. 23 (a) and (b), respectively. It is obvious that the proposed FTCU stabilizes the operation of the control loops during the different types of faults. The results explore the perfect behavior of the proposed control technique under different types of switch faults.

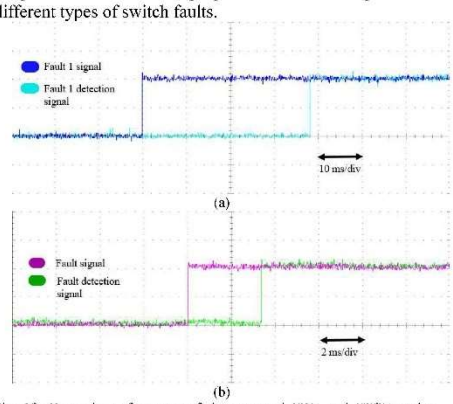


Fig. 19: Dynamic performance of the proposed FDU and FTCU under multiple faults: a) fault 1, b) fault 2.

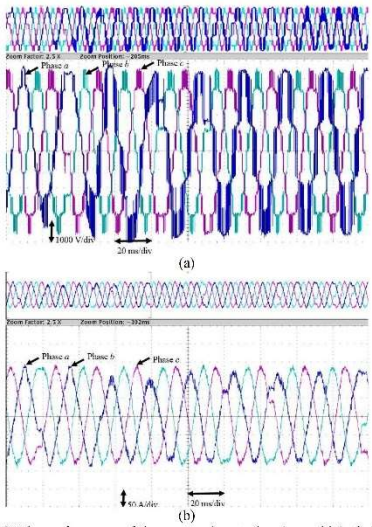


Fig. 20: The performance of the proposed control under multiple faults: a) Three-phase voltages, b) three- phase load currents.

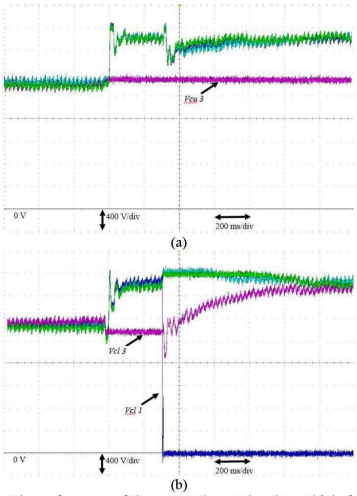


Fig. 21: The performance of the proposed control under multiple faults: a) sub-modules voltages of upper arm in leg *a*, b) sub-modules voltages of lower arm in leg *a*.

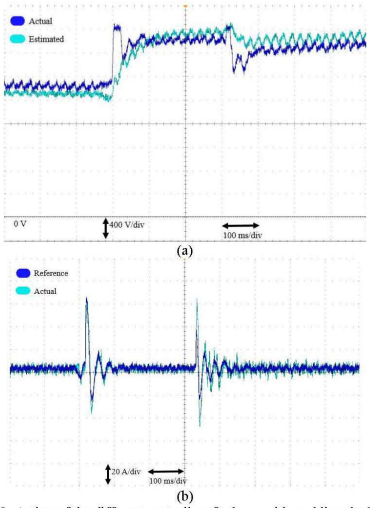


Fig. 22: Action of the different controllers for leg *a* with enabling the FTCU for multiple failure: a) The capacitor voltage estimation of sub-module *Vcu1*, b) Actual and reference waveform of the circulating current.

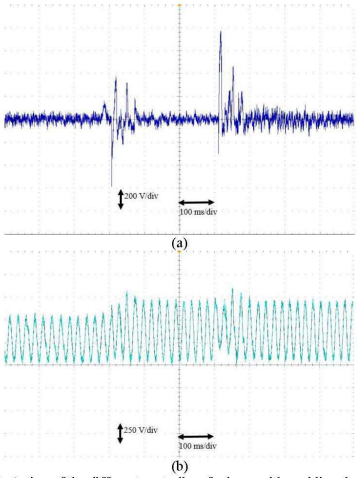


Fig. 23: Action of the different controllers for leg *a* with enabling the FTCU for multiple failure: a) averaging voltage reference, b) modulating voltage reference for the first sub-module of the upper arm.

IX. Conclusion

The paper presents two estimation units based on ADALINE and RLS algorithms for capacitor voltages of the sub-modules of the MMC. For each leg of the MMC, the proposed estimation unit requires only three sensors; one for the phase voltage and the others for the voltages across the arm reactors. Moreover, the proposed RLS estimation unit is integrated with a control strategy to balance the voltages across the sub-modules of the MMC. Furthermore, the estimated capacitor voltages from the two techniques are utilized to detect and localize the open-circuit and short-circuit faults of sub-module switches. After isolating the faulty sub-modules, the proposed FTCU boosts the capacitor voltage and modifies the phase shift between the carrier signals for the rest of sub-modules in the leg to cope with the reduced number of effective sub-modules. The proposed integrated control strategy eliminates the need for direct measurements of capacitors voltages and their associated communication system which renders it suitable for implementing a low cost centralized controller for the MMC with a large number of sub-modules. In addition, the proposed FDU and FTCU do not need any extra components as they are based on the estimation algorithms that are simultaneously utilized for the proposed control of the MMC.

The fast response and the accurate tracking of the proposed scheme for sub-modules capacitor voltage estimation are revealed from the simulation and the HIL results under different dynamic conditions. Moreover, the proposed MMC controller succeeds to balance the capacitors voltages. The accurate performance of the proposed FDU, for detecting and localizing different faults, results from its hybrid processing where the fault decision is not only based on the reduction on the estimated per-unit voltage but also on the rate of change of the difference between the estimated voltages from the proposed ADALINE and RLS algorithms. Furthermore, the proposed FTCU succeeds to stabilize the operation of the averaging and balancing control loops of the MMC under

different types of faults. In addition, the circulating current is tightly tracking its reference signal.

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Reliability Enhancement of Modular Multilevel Converter by Applying Fault Tolerant Control

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***Abstract*— Modular Multilevel Converters (MMC) are considered very suitable for the transmission of bulk power. Increasing the reliability of MMCs forms a real challenge since they are built from series connection of sub-modules. Applying the concept of fault tolerance to the MMC control system can significantly increase the reliability of the MMC as it will be available in normal as well as faulty conditions. This paper presents an analysis of the MMC reliability enhancement gained from applying different fault tolerant control techniques. The reliability is investigated through solving differential equations generated from Markov chains.**

Keywords—Markov chains; fault tolerant control; MMC.

I. INTRODUCTION

The fault tolerant control (FTC) system is the system which is able to perform its desired control functions at high level of stability and security during the occurrence of a certain fault. FTC systems are gaining the interest of many researchers in different research fields because of their ability to enhance the overall reliability of systems. FTC systems are classified into two main types: passive and active [1-3].

As shown in Fig. 1, active FTC system receives the continuous fault status from the FDU. Then at the fault condition, it re-configures the control system to a new system which isolates the faulty part of the system and maintains the stability of the plant. It is important to mention that the redesign process of the system is performed online which normally may allow some changes to desired control functions or degradation in the performance [4-5].

The main disadvantage of active FTC techniques is the slow response of them due to the time consumed on the fault detection and controller redesign. However, the main advantage of these techniques is their ability to detect wide range of faults [5].

In passive FTC, the controller is designed in the offline mode then it operates with fixed behavior during normal and abnormal conditions. Therefore, it should be designed such that it can tolerate the faults [6-7]. The main advantages of passive FTC techniques can be summarized in the following points:

- There is no need for the fault detection process as the system is working with the same parameters during normal as well as fault conditions.
- The response of them is very fast due to the elimination of FDU and the control redesign processes.

However, it is very difficult for one passive FTC system to detect different types of faults since they are designed in the offline mode [8].

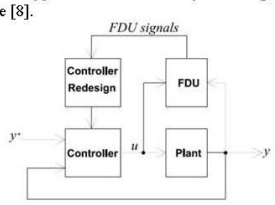

Fig. 1: Structure of active FTC.

According to the literature, there are different types of sub-module faults that can strike MMCs and affect their operation [9-10]. Since MMCs are used in important applications and at the same time they form a big investment, it is extremely important to detect these fault very quickly to protect the whole system from sudden failures. For this particular purpose, the sub-module faults are investigated in the following sub-sections. Moreover, popular fault detection techniques are discussed to find out the advantages and disadvantages of each method and pointing what is needed in the process of fault detection of MMCs.

MMCs should work at high level of reliability as they usually work in critical applications that do not have the luxury of losing the power transfer. Based on this fact, it is highly recommended to provide the control of the MMC with fault tolerance capability to make the MMC able from delivering the desired power during faulty conditions without the need to block the converter [11].

This paper presents an investigation of MMC reliability enhancement when two different fault tolerant control

techniques are used. The first technique is based on using redundant sub-modules while the second depends on modifying the control of the MMC during faults. Section II presents the operation concept of the MMC and its mathematical model. The reliability analysis using Markov chains of the MMC is illustrated in section III. Section IV shows the conclusion and major findings of the presented work.

II. Modular Multilevel Converters

A. The structure of MMCs

The MMC consists of sub-modules connected in series forming a leg in each phase. The sub-module can be a half-bridge or a full-bridge and each sub-module has a capacitor that buffers the energy from the dc to the ac side and vice versa; thus the dc-link capacitor is not required. A high-speed bypass switch is added to the output port of the sub-module to isolate the sub-module in case of a fault. As shown in Fig. 1, each phase leg is divided into two arms upper and lower. Each arm has identical numbers of sub-modules to generate balanced voltages in the two arms of each phase. Inductors are installed in arms to smooth and filter the currents [12-13].

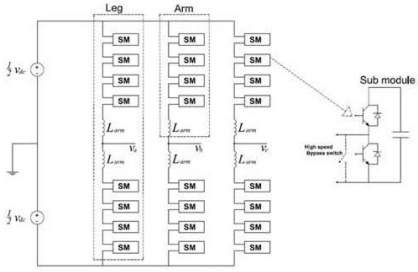

Fig. 1. The structure of the MMC.

B. MMC Operating Modes

The MMC half bridge sub-module has four operation modes during which energy is transferred:

Mode 1: When S1 is closed, S2 is opened, and the arm has positive polarity. The current flows into the capacitor, charging it. The sub-module is then inserted. See Fig. 2(a).

Mode 2: When S1 is opened, S2 is closed, and the arm has positive polarity. The sub-module is bypassed, and the current flows towards the next sub-module, keeping the capacitor charge constant. The sub-module is then bypassed. See Fig. 2(b).

Mode 3: S1 is closed, S2 is opened, and the arm has negative polarity. The capacitor starts to discharge and then the sub-module is inserted. See Fig. 2(c).

Mode 4: When S1 is opened, S2 is closed, and the arm has negative polarity. The current flows towards the next module, keeping the capacitor charge constant, after which and the sub-module is bypassed. See Fig. 2(d).

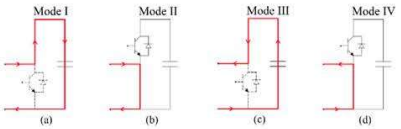

Fig. 2. Different operating modes of MMC sub-modules. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

C. Mathematical Model of MMC

For the purpose of designing an inner control system for the MMC, it is necessary to mathematically analyze the converter. The converter arms, shown in Fig. 3, are represented as variable capacitors connected in a series with arm resistance and inductance. The number of sub-modules per arm and the switching frequency is assumed as infinite to simplify the analysis because of the perfect sinusoidal output voltage and total voltage balancing between arms. The arm capacitance insertion is represented with a modulation value $m_{arm\,x}$, where x may be u for upper arm or l for lower arm. The $m_{arm\,x}$ is varied from 0 to 1. For example, when $m_{arm\,u} = 0$, this indicates that all sub-modules in the upper arm are bypassed and when $m_{arm\,l} = 1$, this indicates that all sub-modules in the lower arm are inserted. The value Σv_{Cx} is the sum of arm capacitor voltages. The arm voltage is given by:

$$v_x(t) = m_{arm\,x}(t).\Sigma v_{Cx}. \tag{1}$$

The inserted arm capacitance is given by:

$$C_{insx} = \frac{C_{SM}}{N.m_{arm\,x}(t)} \tag{2}$$

where C_{SM} is the capacitance of one sub-module and N is the number of sub-modules per arm. If the arm current is $i_x(t)$, the total capacitor voltage dynamics can be expressed by:

$$\frac{d\Sigma v_{Cx}}{dt} = \frac{i_x(t)}{C_{ins\,x}}. \tag{3}$$

Substituting (2) in (3), the capacitor voltage dynamics can be expressed for the upper and lower arms by:

$$\frac{d\Sigma v_{Cu}}{dt} = \frac{N.m_{arm\,u}.i_u}{C_{SM}} \tag{4}$$

$$\frac{d\Sigma v_{Cl}}{dt} = \frac{N.m_{arm\,l}.i_l}{C_{SM}} \tag{5}$$

The current i_{diff} is the differential current, which circulates between the phase legs. The circulating current of any phase is described as follows:

$$i_{diff} = \frac{i_u + i_l}{2}. \tag{6}$$

By performing the necessary circuit analysis, the output phase voltage v_o is given by:

$$v_o = \frac{v_{dc}}{2} - L_{arm}\frac{di_u}{dt} - m_{arm\,u}\,\Sigma v_{Cu} \tag{7}$$

$$v_o = -\frac{v_{dc}}{2} + L_{arm}\frac{di_l}{dt} + m_{arm\,l}\,\Sigma v_{Cl}. \tag{8}$$

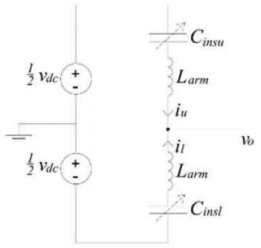

Fig. 3. The MMC average model.

III. MMC Reliability Analysis

A system failure can be represented by its probability to occur, this is done considering the process behavior as a random variable which receive its value from finite state space elements. To assess the reliability of the MMC, firstly the failure rate of the IGBT λ_0 should be assumed. The reliability function *R(t)* is the probability of success for the system which is expressed as:

$$R(t) = 1 - F(t) \quad (9)$$

Where *F(t)* is the probability of the system failure which is complementary to the *R(t)* and is given by:

$$F(t) = \int_0^t f(\tau)d\tau \quad (10)$$

Where *f(t)* is rate of change for the failure probability of a certain components, thus (10) can be rewritten as:

$$f(t) = \frac{dF(t)}{dt} \quad (11)$$

Another important definition is the mean time to failure (MTTF) which gives an indication for the expected life time of a component that cannot be repaired or maintained, the MTTF is expressed as:

$$MTTF = \int_0^\infty R(t)dt \quad (12)$$

For a system without a fault tolerant control, the MMC will fail if one sub-module suffers from a fault in either the upper or lower legs. To model the reliability of the converter in this case, a Markov chain is developed as shown in Fig. 4.

In this case the failure rate for one sub-module in a certain leg should equal:

$$\lambda_1 = (2N - 1)\lambda_0 \quad (13)$$

Where λ_0 is the failure rate of each IGBT switch.

Based on the Markov chain and from (13) substituting in (11), this gives:

$$\frac{dP_1}{dt} = -2\,\lambda_1\,P_1(t) \quad (14)$$

Solving the first order differential equation presented in (10), the reliability function can be expressed as:

$$R(t) = P_1(t) = e^{-2\,(2N-1)\lambda_0\,t} \quad (15)$$

From (15) substituting in (12), the mean time to failure is:

$$MTTF_{MMC\ without\ FTC} = \frac{1}{2\lambda_0}\left(\frac{1}{(2N-1)}\right) \quad (16)$$

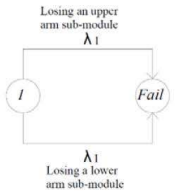

Fig. 4. Markov chain of the MMC without FTC.

IV. MMC Reliability Enhancment Using FTC

The enhancement of the MMC reliability is calculated while applying two FTC techniques. The first technique achieves the fault tolerance using redundant sub-modules while the second depends on modifying the control of the MMC without using redundant sub-modules.

A. FTC using redundant sub-modules

Regarding tolerating the fault using redundant sub-modules, the idea depends on disconnecting the faulty sub-module and inserting a new redundant sub-module without the disconnection of the MMC as shown in Fig. 4 [13-15].

The process of insertion of the redundant sub-modules is done using a strict control. At each triggering time, the control system identifies the state of each sub-module by the aid of a suitable fault detection algorithm. If any sub-module is subjected to high switching commutations or a fault, the control system bypasses the faulty sub-module and replaces it by a redundant sub-module [15].

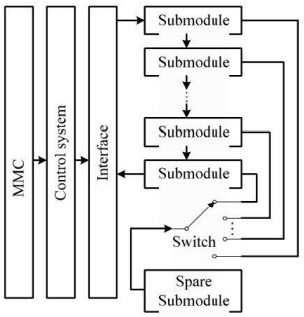

Fig. 4: Structure of MMC with redundant sub-modules.

In this case, the reliability of the MMC can be figured out from Fig. 5 which has two failure rates. The first failure rate when losing one sub-module, λ_1. While the second failure rate, λ_2 indicates losing two sub-modules in the same leg. In the sub-module redundant based FTC, each leg is assumed to be

equipped with one redundant sub-module. Thus, the sub-module failure rates are given by:

$$\lambda_1 = (\frac{2N-1}{2} + 1)\lambda_0 \quad (17)$$

$$\lambda_2 = (\frac{2N-1}{2})\lambda_0 \quad (18)$$

According to Markov chain, the failure probability of the first state is:

$$\frac{dP_1}{dt} = -\lambda_1 P_1(t) \quad (19)$$

Solving the differential equation given in (19) gives:

$$P_1(t) = e^{-(\frac{2N-1}{2}+1)\lambda_0 t} \quad (20)$$

Following the same way, the failure probability of state 2 gives:

$$\frac{dP_2}{dt} = \lambda_1 P_1(t) - \lambda_2 P_2(t) \quad (21)$$

Solving (21) gives:

$$P_2(t) = (\frac{2N-1}{2})(e^{-(\frac{2N-1}{2})\lambda_0 t} - e^{-(\frac{2N-1}{2}+1)\lambda_0 t}) \quad (22)$$

From (20) and (22), the probability of the fail state is the summation of $P_1(t)$ and $P_2(t)$:

$$R(t) = P_1(t) + P_2(t) = \left((\frac{1-2N}{2}) e^{-(\frac{2N-1}{2}+1)\lambda_0 t}\right) + (\frac{2N-1}{2})(e^{-(\frac{2N-1}{2})\lambda_0 t}) \quad (23)$$

From (23) substituting in (12), the MTTF is:

$$MTTF_{MMC\ with\ FTC\ 1} = \frac{1}{\lambda_0}\left(\frac{1-N}{N+1}\right) \quad (24)$$

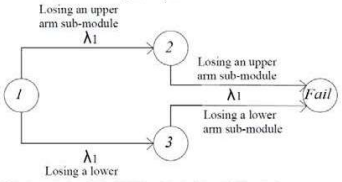

Fig. 5. Markov chain of the MMC with the first FTC technique.

B. *FTC based on modifing the MMC inner control*

Unlike the previous technique, the MMC is not equipped by redundant sub-modules. The MMC inner control modifies the control and isolates the faulty sub-modules. To simplify the calculations and give a sense for the results, the reliability calculations will be performed for the simulation model which incorporates four sub-modules per arm. In this particular case, the Markov reliability chain is developed as shown in Fig. 6. The Markov reliability chain shows that the MMC with the proposed FTCU have four possible finite states before reaching the failure state instead of one as shown in the previous section. The possible states are:

- State 1: The healthy state (no faulty sub-modules).
- State 2: Losing a sub-module in the upper arm.
- State 3: Losing a sub-module in the lower arm.
- State 4: Losing two sub-modules (one in the upper arm and one in the lower arm).
- Fail state: Losing two sub-modules in the upper arm or two sub-modules in the lower arm or both.

In this case, two failure rates should be presented λ_1 and λ_2. λ_1 is the failure rate of one sub-module and will be the same as calculated in (13). λ_2 is the failure rate for losing two sub-modules and should equal:

$$\lambda_2 = (2N-3)\lambda_0 \quad (25)$$

Based on the Markov chain, the probability for the first state $P1$ will remain the same as presented in (15). Regarding the probability of the second state $P2$, it can be expressed as follows:

$$\frac{dP_2}{dt} = -(\lambda_1 + \lambda_2)P_2(t) + \lambda_1 P_1(t) \quad (26)$$

From (26) substituting in (11), the solution of the differential equation gives:

$$P_2(t) = \frac{2N-3}{2}\left(e^{-(\lambda_1+\lambda_2)t} - e^{-2\lambda_1 t}\right) \quad (27)$$

$P_3(t)$ has the same probability of $P_2(t)$ since the conditions are the same.

Moving to the forth state probability, it is also can be emphasized from the Markov chain as follows:

$$\frac{dP_4}{dt} = -(2\lambda_2)P_4(t) + \lambda_1 P_2(t) + \lambda_1 P_3(t) \quad (28)$$

From (28) and substituting in (11), the solution of this differential equation is expressed as:

$$P_4(t) = \frac{(2N-3)^2}{4}\left(e^{-2\lambda_1 t} + e^{-2\lambda_2 t}\right) - \frac{(2N-3)^2}{2} e^{-(\lambda_1+\lambda_2)t} \quad (29)$$

The reliability function $R(t)$ is the summation of the four probabilities as follows

$$R(t) = P_1(t) + P_2(t) + P_3(t) + P_4(t)$$
$$= \left((2N-2) + \frac{(N-3)^2}{4}\right) e^{-2(2N-1)\lambda_0 t} + \left((2N-3) - \frac{(2N-3)^2}{4}\right) e^{-2(2N-2)\lambda_0 t} + \left(\frac{(2N-3)^2}{4}\right) e^{-2(2N-3)\lambda_0 t} \quad (30)$$

From (6.18) substituting in (6.8), the mean time to failure is:

$$MTTF_{MMC\ with\ FTC} = \frac{1}{2\lambda_0}\left(\frac{\left((2N-2)+\frac{(2N-3)^2}{4}\right)}{(2N-1)} + \frac{\left((2N-3)-\frac{(2N-3)^2}{4}\right)}{(2N-2)} + \frac{\left(\frac{(2N-3)^2}{4}\right)}{(2N-3)}\right) \quad (31)$$

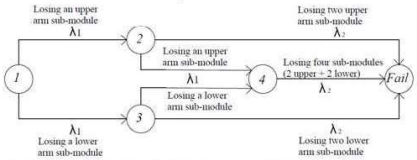

Fig. 6. Markov chain of the MMC with the second FTC technique.

V. Results and Discussions

To compare between the reliability before and after the application of the two fault tolerant control strategies, the reliability density functions presented in (15), (23) and (30) are plotted against time for five level MMC. The IGBT failure rate λ_0 is assumed to be $10^{-7}h^{-1}$ which is almost three years.

As shown in Fig. 7, the reliability density function is considerably enhanced which means that the rate of failure for the MMC has been decreased. This is also clearly appearing in table I where the MTTF has significantly increased when applying the two FTC strategies.

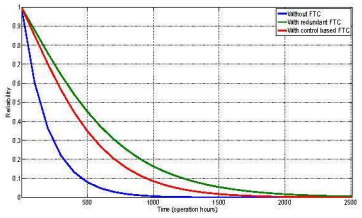

Fig.7: The reliability of the MMC using different FTC techniques.

TABLE I
COMPARISON BETWEEN MTTF ASSOCIATED WITH DIFFERENT FTC TECHNIQUES

CONDITION	MTTF (IN HOURS)
Without FTC	714285
With redundancy FTC	8750000
With control based FTC	163958335

VI. CONCLUSION

In this paper, the reliability of the MMC has been carefully studied and analized using Markov chains. The effect of using FTC on the MMC is investigated. Results showed that using the FTC concept will significantly increase the MTTF of the MMC which means that the MMC will be very reliable since it is availability has increased to contain normal and faulty operation conditions.

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Enhanced Approach for Modelling and Simulation of Modular Multilevel Converter Based Multiterminal DC Grids

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***Abstract*— Multi-terminal direct current (MTDC) grids are gaining the interest of many researchers because of their unique features that improve the transmission network functionality and reliability. Unlike two level and three level voltage source converters (VSC), modular multi-level converters (MMC) are suitable for the application of MTDC grids because of their generous advantages such as the elimination of DC link capacitor, the improved quality of the output power and the lower footprint. However, simulation of MMC based MTDC grids is a real challenge because of the huge computational burden due to the high number of sub-modules. This paper proposed a modeling approach for a four terminal MTDC grid which is based on average MMC models with 401 voltage levels. The control system structure which controls the power through the MTDC grid and the MMCs at each terminal is presented. The whole system is tested and simulated using PSCAD/EMTDC under different operating conditions to verify the validity and evaluate the performance of the proposed modelling approach.**

Keywords-MTDC; MMC; Power control; PSCAD

I. INTRODUCTION

The high voltage direct current (HVDC) transmission systems are currently involved in many projects especially for transmission systems that transmit bulk amounts of power for long distances. This is simply because of the reduced losses of HVDC compared to the high voltage alternating current (HVAC) transmission as shown in figure.1. Also the bipolar HVDC circuit is formed from two cables only compared to four cables in HVAC circuits. Moreover, the HVDC systems do not suffer from stability problems due to the absence of reactance effect which makes them have no distance limitations [1].

Instead of having many point to point transmission lines, MTDC grids are attractive for many applications such as: connecting different grids together, integration of off-shore wind energy to AC grids, etc [2]. Figure.2 shows a general diagram for a four terminal DC grid. The conversion from AC to DC and vice versa is performed using VSC which has different topologies. One of the promising topologies in HVDC transmission is the MMC because of the improved quality of the output power due to the sufficient number of voltage levels which eliminates the need of adding filtering equipment [3]. The modelling of the MMC based MTDC grids is necessary for studies and analysis purposes to enable the researchers and engineers to have better understanding of the operation and behavior of such networks. However, the modelling of the MMC is not an easy task since the number of sub-modules can be in hundreds which makes it very difficult to develop a detailed simulation model due to the excessive and massive computational burden [4]. To solve this problem, a suitable average model can be used to lower the calculations needed [5]. This paper presents a modelling approach for the simulation of four terminals DC grid using PSCAD/EMTDC simulation software, each terminal includes an average model for a 401 level MMC. Section II explains the MMC structure including the mathematical analysis for the developed average model while section III and IV introduce the control system structure which controls the power through the MTDC grid and the MMCs at each terminal, whereas, section V indicates an analysis of the results acquired under different operating conditions. Finally, section VI demonstrates the conclusion of the research verifying the main ideas based on the simulation results.

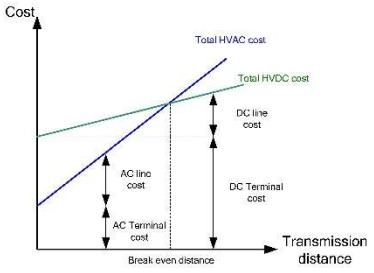


Figure. 1: Comparison between the losses associated with the HVAC and HVDC transmission lines

Figure. 2: A general diagram for a four terminal grid.

II. MODELLING OF THE MMC

A. MMC structure and operation modes

As demonstrated in figure.3, the MMC is formed from three legs, each leg is formed from two arms connected to each arm through arm inductors, these inductors are responsible for smoothing the arm currents. Each arm consists of series connected sub-modules which can be either full bridge or half bridge connected to a capacitor. The sub-module is considering to be the basic unit of the MMC as it exchanges the energy between the AC and DC sides of the converter. There are two main operation modes for the MMC as shown in table 1 [6].

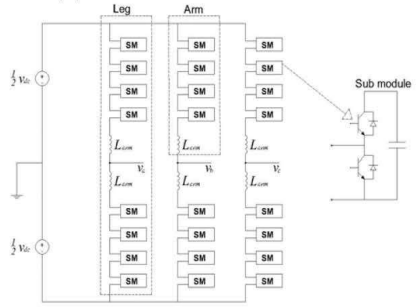


Figure.3. Three-phase MMC topology and internal sub-module.

TABLE I. MMC MODES OF OPERATION

Mode	I	II
S1	Switched on	Switched off
S2	Switched off	Switched on
Description	Output voltage from the sub-module has a positive polarity. The capacitor is charging/discharging, depending on the current direction.	The sub-module is bypassed and the current flows towards the next sub-module keeping the capacitor charge constant.

B. Mathematical representation of the average model

The average model used in the simulation depends on converting the detailed model of the sub-module to its thevenin equivalent. As shown in figure. 4, the voltage across the sub-module is given by identifying its equivalent resistance and voltage. The equivalent resistance can be expressed as shown below [5]:

$$R_{eq} = R_2\left(1 - \frac{R_2}{R_1+R_2+R_c}\right) \quad (1)$$

R_1 and R_2 are the resistances of the upper and lower IGBTs, when the IGBT is switched on, its resistance will equal the value of the on state resistance which is about 0.001 Ω compared to 100000 $k\Omega$ in the off state. R_c is the equivalent resistance of the sub-module capacitor having a capacitance of C, this resistance can be calculated using the following expression:

$$R_c = \frac{\Delta T}{2C} \quad (2)$$

Where ΔT is the time step of the simulation. The equivalent voltage of the sub-module thevenin model is given by:

$$V_{eq} = \frac{R_2}{R_1+R_2+R_c} V_{c\,eq} \quad (3)$$

$V_{c\,eq}$ is the equivalent voltage across the capacitor which is given by:

$$V_{c\,eq} = \left(\frac{\Delta T}{2C} I_c(t-\Delta T) + V_c(t-\Delta T)\right) \quad (4)$$

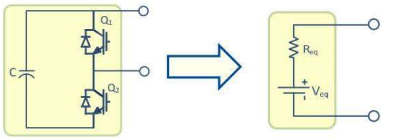


Figure. 3: Thevenin equivalent of the sub-module.

III. CONTROL OF ACTIVE AND REACTIE POWER THROUGH THE MTDC GRID

Controlling the flow of active and reactive powers in the grid is done by controlling both the DC and AC voltage at each terminal. The control system at each terminal is formed from five units as described in the following sub-sections.

A. Phase locked loop

The phase locked loop technique is responsible for synchronizing the AC voltage of the MMC with the grid voltage. This is done using a feed forward PI control loop which receives the quadrature axis voltage of the MMC AC terminals V_{tq}. The output of the PI controller is then added to the initial angular frequency ω_0. The output of the addition is passed through integrator resulting into the grid phase θ.

B. AC and DC voltage control loops

The active and reactive power control loops are very simple as they utilize two PI controllers to decide the values of the

MMC direct and quadrature components of the desired MMC output current i_d^* and i_q^*.

C. Inner current loop

The inner current control loop is used to regulate the MMC output current based on the received references from the DC and AC control loops, the loop is designed based on the MMC dynamics of the AC side:

$$L_{grid}\frac{di_d}{dt} = i_q\omega L_{grid} - i_d R_{grid} + V_{t\,d} - V_{s\,d} \quad (5)$$

$$L_{grid}\frac{di_q}{dt} = -i_d\omega L_{grid} - i_q R_{grid} + V_{t\,q} - V_{s\,q} \quad (6)$$

Where L_{grid} and R_{grid} are the grid inductance and resistance. V_t is the MMC terminal voltage while V_s is the grid voltage.

According to (5) and (6), two PI controllers are added to regulate the i_d and i_q. The output of the two controllers is then added to the measured components of the grid voltage $V_{s\,d}$ and $V_{s\,q}$ forming two feed forward loops. The decoupled components of i_d and i_q are then subtracted from the two loops resulting in the reference terminal voltages $V_{t\,d}^*$ and $V_{t\,q}^*$. Figure 4 shows the block diagram of the active and reactive power control [7].

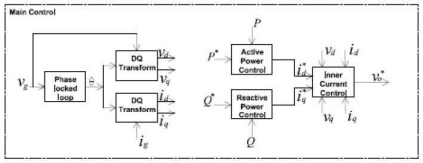


Figure. 4: Active and reactive power control.

IV. THE INNER CONTROL OF THE MMC

The inner control system of the MMC is responsible for achieving three important tasks: the first is balancing the voltage between the capacitors while the second is suppressing the differential current. The third task is the switching of the MMC.

A. Capacitor voltage balancing using the energy control

In this method, the capacitor voltages are balanced by controlling the total energy stored in the leg and the differential energy between the upper and lower arms [8]. For better understanding of this method, the energies of the upper and lower arms should be mathematically expressed as follows:

$$W_{Cx}^{\Sigma} = \Sigma C_{effx}\,(V_{Cx}^{\Sigma}) \quad (7)$$

Where x can be *u* for the upper arm or *l* for lower arm.

Differentiating equation (3.1), this gives:

$$\frac{dW_{Cu}^{\Sigma}}{dt} = (\frac{i_v}{2} + i_{diff})(\frac{V_{dc}}{2} - e_v - v_{diff}) \quad (8)$$

$$\frac{dW_{Cl}^{\Sigma}}{dt} = (\frac{i_v}{2} + i_{diff})(\frac{V_{dc}}{2} + e_v - v_{diff}) \quad (9)$$

From (8) and (9), the following equations express the total energy stored in the leg W_C^{Σ} and the energy difference between the arms W_C^{Δ} :

$$W_C^{\Sigma} = W_{Cu}^{\Sigma} + W_{Cl}^{\Sigma} \quad (10)$$

$$W_C^{\Delta} = W_{Cu}^{\Sigma} - W_{Cl}^{\Sigma} \quad (11)$$

Differentiating (10) and (11) and equalizing them with (8) and (9) gives:

$$\frac{dW_C^{\Sigma}}{dt} = \left(V_{dc} - 2v_{diff}\right)i_{diff} - e_v i_v \quad (12)$$

$$\frac{dW_C^{\Delta}}{dt} = \left(\frac{v_{dc}}{2} - v_{diff}\right)i_v - 2e_v i_{diff} \quad (12)$$

Where $v_{diff} = Ri_{diff} + L\frac{di_{diff}}{dt}$. Equation (11) and (12) shows that the differential current i_{diff} plays a major role in balancing the capacitor voltages of the MMC sub-modules. Based on this, the modulation signals can be expressed as:

$$m_u = \frac{\frac{V_{dc}}{2} - e_{v\,ref} - v_{diff\,ref}}{V_{Cu}^{\Sigma}} \quad (13)$$

$$m_l = \frac{\frac{V_{dc}}{2} + e_{v\,ref} - v_{diff\,ref}}{V_{Cl}^{\Sigma}} \quad (14)$$

Although the equation (13) and (14) look very simple, the direct application of them makes the converter unstable [9]. To maintain the stability of the converter, two control loops are needed as shown in figure 5. The first loop is a PI control loop which is responsible for enabling the total stored energy from following its reference, while the second loop is responsible for balancing the energy between the two arms, in other words for canceling W_C^{Δ}.

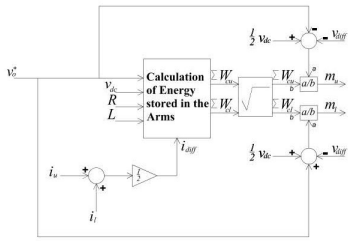


Figure. 5: Block diagram of the capacitor voltage balancing based on energy control.

B. Circulating current supressing control

The circulating current is a virtual current which circulates between the two arms; it can be expressed by:

$$i_{circ} = \frac{i_u + i_l}{2} \quad (15)$$

Where i_u and i_l are the arm currents. Having a high level of the circulating currents means that the MMC will be subjected to negative consequences such as the increased heat effect and electrical losses. Thus, it is a must to suppress the circulating current to a very small amount. This can be achieved by eliminating the double line frequency component

of it. Firstly, the three phase circulating current is transformed into the dq reference frame. Then the dq currents are subtracted from the reference value which is zero. The error signals are passed through two PI control loops and then the output signals are transformed to the three phase reference signals of the circulating voltage. Figure 6 shows the block diagram of the circulating current suppressing control.

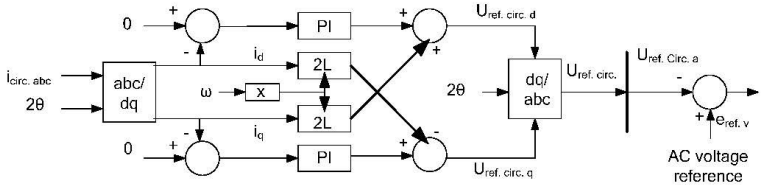


Figure. 6: Block diagram of the capacitor voltage balancing based on energy control.

V. Simulation Results and Discussions

A four terminal DC grid is simulated using PSCAD/EMTDC, each terminal contains an average model for 401 level MMC. The simulation parameters are found in table 2.

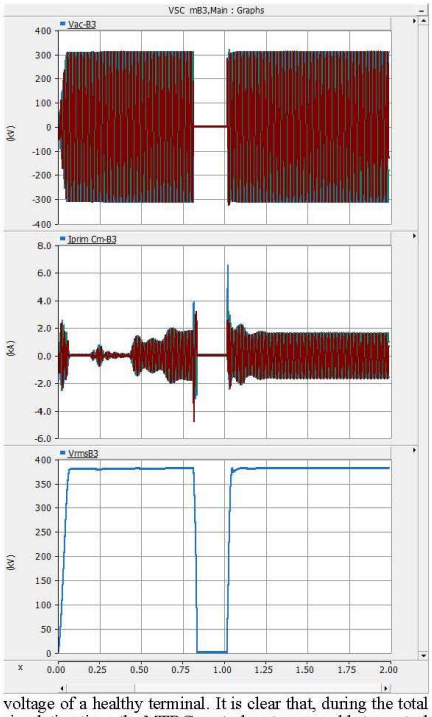
TABLE II. Parameters of the Simulated Four Terminals DC Grid

Parameter	Value
Rated AC voltage	380 kV
Rated DC voltage	400 kV
Rated power	10000 MW
MMC voltage levels	401 level
Arm inductance	15 mH
Sub-module capacitance	220 µF

The simulated case study is demonstrated to show the behavior of the MTDC and the reaction of different control systems under three conditions:

1. The start-up and system energization.
2. The normal operation mode.
3. The faulty condition.

Firstly the AC grids of the rectifier terminals start to inject active power towards the MMCs to build up the voltage of the DC link. Using the MTDC grid power control loops, the DC voltage reaches its rated level which is 400 kV and settles at this value after 0.6 sec. A three phase fault is applied to one terminal at the instant of 0.8 sec, then cleared at 1 sec. Figure 7 shows the three phase voltages, currents and the RMS voltage of the MMC where the three phase fault has been applied. It is obvious that the MTDC grid control succeeded to protect the converter since it was blocked in order to isolate the fault. After clearing the fault, the P-Q control loops started quickly to build the DC voltage again. Regarding other terminals, they regulated the DC voltage during the fault and at the same time did not contribute to the faulty terminal. Figure 8 shows the three phase voltages, currents and the RMS



voltage of a healthy terminal. It is clear that, during the total simulation time, the MTDC control system was able to control

the DC voltage during normal and faulty conditions as shown in figure 9.

Figure. 7: The MMC performance of the faulty terminal: a) Three phase voltages, b) three phase currents and c) The RMS voltage

Moreover, it has succeeded to control the flow of the power smoothly as demonstrated in figure 10. This also can be proven by figure 11 which shows how the direct and quadrature currents track their reference during the whole period. Regarding the MMC inner control, the capacitor voltages of all MMCs have been successfully balanced during the whole simulation period as presented in figure 12. In addition, the circulating currents have been suppressed to its minimum value to limit the conversion losses.

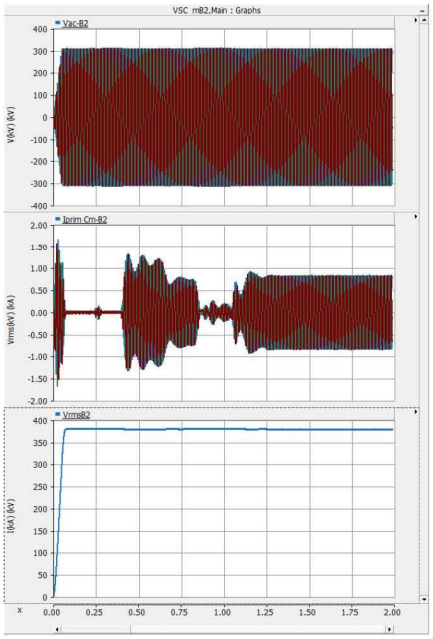


Figure. 8: The MMC performance of a healthy terminal: a) Three phase voltages, b) three phase currents and c) The RMS voltage

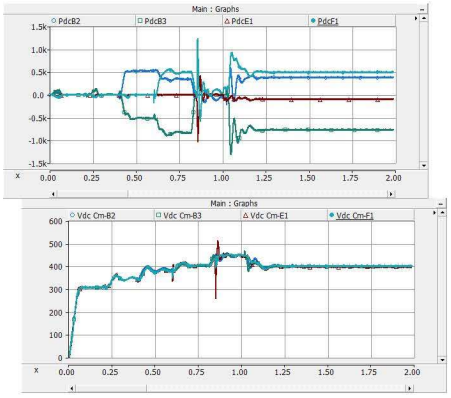


Figure. 9: The DC voltages of the four terminals.

Figure. 10: The active power of the four terminals

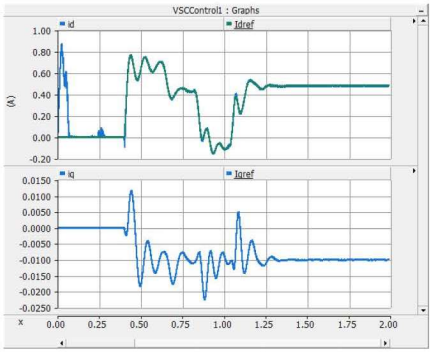


Figure. 11: The DQ currents versus their reference

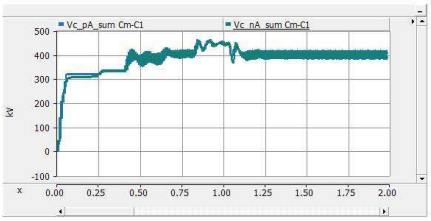


Figure. 12: The sub-module capacitor voltages of one MMC.

VI. Conclusion

This paper presents an enhanced modelling technique for a MMC based four terminal DC grid; where, each terminal includes an average model for a 401 level MMC. An average model for the MMC has been built to lower the computational burden. In addition, the power control including the inner control system of the MMC has been developed according to different industrial standards and physical projects in order to control the flow of active and reactive powers in the grid by controlling both the DC and AC voltage at each terminal. The control system at each terminal was formed from five units.

The simulation model was completed using PSCAD/EMTDC software package to evaluate the performance of the modeled DC network under various operating conditions. **Theoretical r**esults indicate an efficient behavior of the MTDC control loops during normal and faulty conditions providing a full safe to fail operation of the MMCs and guaranteeing a smooth power flow between the terminals. It can be concluded that the proposed model is suitable as a test platform for real MTDC projects and research purposes.

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