DC Line Protection for Multi-Terminal High Voltage DC (HVDC) Transmission Systems

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Certification

I, ***Monday Aideloje Ikhide***; hereby certify that the work contained in this thesis and titled:

"DC Line Protection for Multi-Terminal High Voltage DC (HVDC) Transmission Systems"

was carried out by myself under the supervision and guidance of the under listed supervisory team members:

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Dedication

... to my wife, Doreen and to my lovely kids: David, Daniella and Davina

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Abstract

The projected global energy shortage and concerns about greenhouse emissions have led to the significant developments in offshore wind farm projects around the globe. It is also envisaged that in the near future, a number of existing onshore converter stations and offshore stations will be interconnected to form a Multi-terminal (MT) HVDC systems, whereas protection issues remains a major challenge. This is largely due to the low inductance in DC network compared to AC interconnection which usually results in a sudden collapse in the DC voltage and rapid rise in the fault current thus reaching damaging levels in few milliseconds. Therefore faults in MT-HVDC system must be detected and cleared quickly before it reaches a damaging level; typically *4 – 6ms* (including circuit breaker opening time) following the inception of the fault. For this reason, transient based protection techniques are ideal candidates if the protection scheme must be reliable and dependable. Transient based protection algorithms utilises the higher frequency components of the fault generated signal to detect a fault, therefore making it possible to detect the fault while the fault current is still rising and well before the steady state. The traditional protection algorithms developed for conventional high voltage AC (HVAC) systems such as distance protection are steady state based and as such not suitable for the protection of MT-HVDC systems. Another major issue is selectivity as only the faulty section must be isolated in the event of a fault. This constitutes a major challenge considering the anticipated lengths of the cables. Traditional protection techniques developed for two-terminal HVDC systems are also not suitable for MT-HVDC since it will de-energise the entire network and other sub-grids connected to the main network. DC line protection devices which will operate at a sufficient speed and which will isolate only the faulty section in the event of a fault are therefore required to avoid a total system failure during short circuit. It is anticipated that it will be achieved

by the use of HVDC breakers, whereas the implementation and realisation of such circuit breakers still remain a major issue considering speed, complexity, losses and cost. However, two major vendors have proposed prototypes and hopefully these will be commercially available in the near future. The key issue still remains the development of a fast DC line fault detection algorithm; and it is on these premise that this research was undertaken. The work reported in this thesis is a novel time domain protection technique for application to HVDC grids.

The protection principle developed utilises the "*power*" and "*energy*" accompanying the associated travelling wave following the occurrence of a fault to distinguish between internal and external fault. Generally, either the "*power*" or "*energy*" can provide full discrimination between internal and external faults. For an internal fault, the associated forward and backward travelling wave power; or the forward and backward wave energy must exceed a pre-determined setting otherwise the fault is regarded as external. This characteristic differences is largely due to the DC inductor located at the boundaries which provides attenuation for the high frequency transient resulting from an external fault, hence making the power and energy for an internal fault to be significantly larger than that for external fault. The ratio between the forward and backward travelling wave power; or between the forward and backward travelling wave energy provides directional discrimination. For a forward directional fault (*FDF*) with respect to a local relay, this ratio must be less than unity. However, the ratio is greater than unity for reverse directional faults (*RDF*).

The resulting wave shape of the "*travelling wave power*" (TWP) components also led to the formulation of a novel protection algorithm utilising the wave shape *concavity*. For an internal fault, the second derivative of the resulting polynomial formed by the *TWP* must be negative, thereby indicating a "*concave-upwards"* parabola. However, for an

external fault, the second derivative of the resulting polynomial formed by the *TWP* components must be positive indicating a "*concave-downwards"* parabola.

The developed and proposed protection techniques and principles were validated against a full scale Modular Multi-level Converter (MMC) – based HVDC grid, and thereafter the protection algorithm was implemented in MATLAB. Wider cases of fault scenarios were considered including long distance remote internal fault and a *500*Ω high resistance remote internal fault. In all cases, both the pole-pole (*P-P*) and pole-ground (*P-G*) faults were investigated. The simulation results presented shows the suitability of the protection technique as the discrimination between internal and external faults was made within *1ms* following the application of the fault.

Following this, the protection algorithm was implemented on both a low-cost experimental platform utilising an Arduino *UNO ATmega328* Microcontroller and on a Compact RIO FPGA-based experimental platform utilising LAB-View. The experimental results obtained were consistent with those obtained by simulations.

An advantage of the proposed technique is that it is *non-unit* based and as such no communication delays are incurred. Furthermore, as it is time domain - based, it does not require complex mathematical computation and burden / DSP techniques; hence can easily be implemented since it will require less hardware resources which ultimately will result in minimal cost.

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List of Abbreviations

Acronyms	Meaning
AC	*Alternating current*
DC	*Direct current*
HVDC	*High voltage direct current*
HVAC	*High voltage alternating current*
MT-HVDC	*Multi-terminal high voltage direct current*
MMC	*Modular multi-level converter*
VSC	*Voltage source converter*
LCC	*Line commutated converter*
P-P	*Pole-to-Pole*
P-G	*Pole-to-Ground*
RDF	*Reverse directional fault*
FDF	*Forward directional fault*
FIF	*Forward internal fault*
FEF	*Forward external fault*
TWP	*Travelling wave power*
TWE	*Travelling wave energy*
FVTW	*Forward voltage travelling wave*
BVTW	*Backward voltage travelling wave*
FTWP	*Forward travelling wave power*
BTWP	*Backward travelling wave power*
FTWE	*Forward travelling wave energy*
BTWP	*Backward travelling wave energy*
TWBP	*Travelling wave based protection*
AC	*Alternating current*
DC	*Direct Current*
OTL	*Overhead transmission line*
RES	*Renewable energy resource*
SM	*Sub-module*
IGBT	*Insulated gate bipolar Transistor*
HB	*Half bridge*
FB	*Full Bridge*
DSP	*Digital signal processing*
FCL	*Fault current limiters*
Thr	*Threshold*
R	*Relay*
CB	*Circuit Breaker*

List of Symbols

Symbol	Meaning
di/dt	*Current derivative*
dv/dt	*Voltage derivative*
Zp	*Apparent Impedance*
Zr	*Reach point impedance*
L_f	*Fault distance*
F	*Fault*
Δi	*Incremental change in current*
Δv	*Incremental change in voltage*
v_p	*Peak voltage*
Ω	*Angular velocity*
Z	*Impedance*
R	*Resistance*
L	*Inductance*
C	*Capacitance*
c	*Velocity*
v_{do}	*No-load voltage*
R_{eq}	*Equivalent resistance*
L_{eq}	*Equivalent Inductance*
i_{sc}	*Short circuit current*
ω	*Angular velocity*
L_{arm}	*Arm inductance*
C_{SM}	*Sub-module capacitance*
V_{SM}	*Sub-module voltage*
N_{SM}	*Number of Sub-module*
R_f	*Fault resistance*
i_{DC}	*DC current*
$i_{DC(AV)}$	*Average DC current*
v_{DC}	*DC Voltage*
$v_{DC(AV)}$	*Average DC voltage*
L_{set}	*Setting inductance*
P_{FW}	*Forward traveling wave power*
P_{BW}	*Backward travelling wave energy*
E_{FW}	*Forward traveling wave energy*
E_{BW}	*Backward traveling wave energy*
ΔT	*Setting duration*
ΔT_{re}	*Protection reset element*
Δt	*Incremental change in time*
t_p	*Travel time of wave*
v_{BA}	*Backward voltage travelling wave with respect to terminal A*
v_{FA}	*Forward voltage travelling wave with respect to terminal A*
v_{BB}	*Backward voltage travelling wave with respect to terminal B*
v_{FB}	*Forward voltage travelling wave with respect to terminal B*
t_N	*Sampling Instant*
t_o	*Arrival time of the travelling wave at relay terminal*
t_f	*Time of occurrence of fault*

T_s	*Sampling Period*
t_w	*Window length*
E_r	*Travelling wave energy ratio*
P_r	*Travelling wave power ratio*
t_m	*Relay Measurement time*

Chapter 1

1 General Introduction

This chapter presents the outline of the research carried out on DC line protection for application to multi-terminal High Voltage DC (MT- HVDC) transmission systems, generally referred to as HVDC grids. It includes the background and motivation of the research, the significance of the research, the research scope and limitations, the research aim and objectives as well as the key technical contributions and achievements made. The chapter concludes with a brief outline, structure and organisation of the thesis.

1.1 Background and Motivation

The projected global energy shortage and concerns about greenhouse emissions have led to significant developments in renewable sources in the past decade. To this end, large offshore wind farms have attracted great attention in the last few years since it has been identified as the most promising renewable energy resource [1]. These offshore wind farms are likely to be of very high ratings and will be located further away from the shore than those in operation today. Researchers have also shown that the HVDC transmission technology will become attractive in this regard and likely to be the only feasible and viable option for the integration of these large offshore wind farms. Generally, HVDC transmission system can transport electric power economically and efficiently over longer

distance than the conventional High voltage AC (HVAC) transmission lines or cables [2]. This is due to the absence of capacitive charging and discharging of the cable capacitances, thus resulting in minimal loss. It is also envisaged that in the future, several offshore wind farms and existing onshore converter stations will be interconnected to form a MT-HVDC network, also termed "HVDC grids". Key advantages of HVDC grids includes optimal equipment utilisation, flexibility, reliability and cost reduction. It will also pave the way for energy trading amongst regional countries. However, the availability of fast fault detection algorithms remains a necessity for the secure and reliable operation of these proposed and future HVDC grids[3]–[6]. This is largely due to the characteristic differences in the fault current footprints between the short circuit currents associated with DC interconnections and those of AC interconnections.

Generally, DC fault current rises exponentially and propagates rapidly (resulting from the low inductance in DC systems compared to AC systems), thus reaching damaging levels in a few milliseconds. This implies that fault current interruption in DC networks must therefore be done very quickly than in AC systems since a fault in one part of the grid can consequently result in a total shut down of the entire network [4], [6]. This is an undesirable condition for the grid and hence must be avoided. On the contrary, the large system inductance in High Voltage Alternating Current (HVAC) interconnections limits the rate of propagation of the fault current thereby giving the protection systems sufficient time; typically, up to *60ms* [4] to detect, discriminate and clear the fault. However, this will not be the case for HVDC grids. Therefore, fault detection, discrimination and clearance in HVDC grids must be completed before the fault current reaches a high level to ensure that the faulty section is isolated in the event of faults whilst maintaining continuity of service delivery in the healthy section of the grid. The challenge is to isolate

the fault using the *single-ended* measurements without information from remote end terminal via communication links.

A possible arrangement of a four terminal HVDC grid consisting of five cable sections is shown in Figure 1.1. As shown, in the event of a DC short circuit or fault along cable section 1, only section 1-2 of the grid should be isolated, while maintaining continuity of service in cable sections 2, 3, 4 and 5.

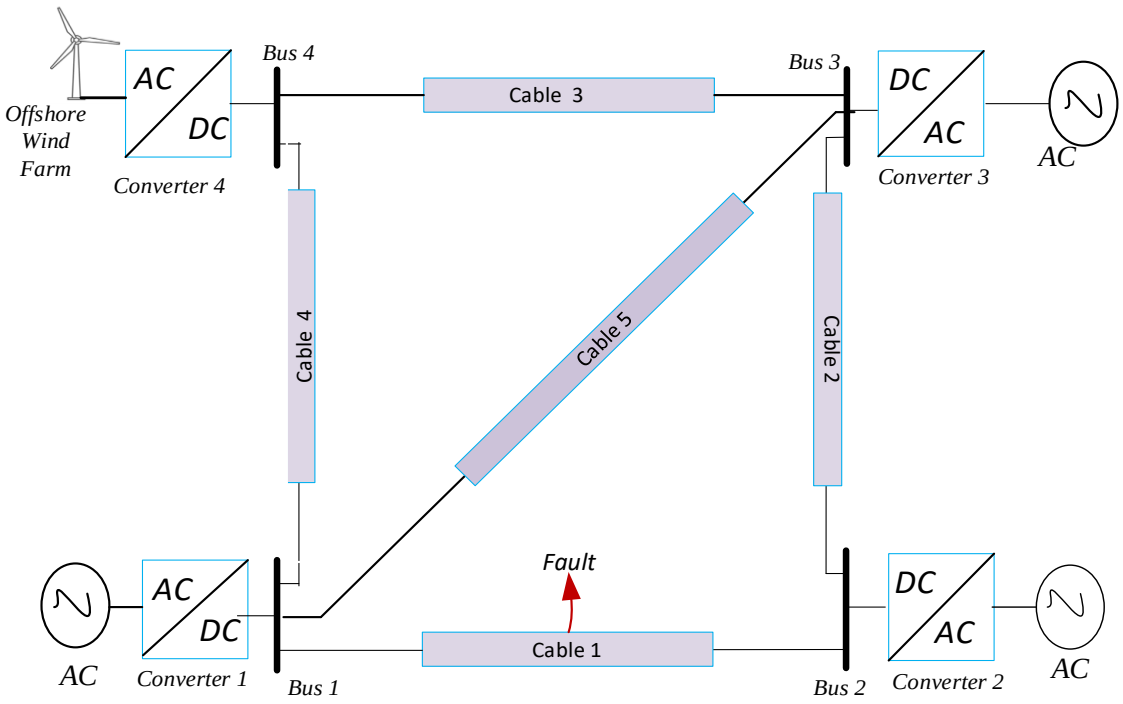


Fig. 1-1 *Conceptual four terminal mesh HVDC Grid*

The lack of zero crossings in DC system has also been a major issue in the development of HVDC circuit breakers for application to DC lines in the recent past. In AC networks, the current is periodically driven through zero (100 times a second for a *50Hz* network), and current zero is the ideal instant to interrupt the fault current. This is however not the case in DC networks due to the absence of zero crossings in DC current. Early attempts

made to develop mechanical HVDC breaker yielded limited results due to technical issues involved in generating artificial zero crossings of the current as well as a suitable method for dissipating the huge amount of energy[8]. However, at present, remarkable achievements have been made; as prototype HVDC breakers which combine electromechanical parts and power electronic switches have been proposed [9][10], and hopefully will be commercially available in the near future. However, the key issue still remains the development of fast fault detection algorithms for the protection of DC lines. It is against these backdrops that this research was carried out, with the following aim and objectives.

1.2 Aim and Objectives of the research

1.2.1 Aim

The aim of this research is to develop a fast, reliable and robust DC line protection scheme for application to HVDC grids. The objectives include:

1.2.2 Objectives

I. To investigate the fault scenarios in HVDC system in general with a focus on HVDC grids, and with the view to fully characterise the associated fault current following the occurrence of a fault on the grid.

II. To develop methods for the fast detection of fault currents in HVDC grids with a focus on short circuits along the DC links

III. To develop a novel protection algorithm for implementation on modern digital relays.

IV. To evaluate the algorithm and the protection scheme by off line and/or real time digital simulations

1.3 Significance of the Research

As indicated in section 1.1, a major issue in the development of HVDC grids is the rapid propagation of the fault current into the grid. In the light of this, two enablers for the realisation of HVDC grids have been identified. They are the availability of fast and robust HVDC breakers as well as intelligent fault detection algorithms. However, as two major vendors in the power utility sector have developed prototype HVDC breakers[9][10], it is therefore envisaged that commercial HVDC breakers will be available soon. This implies that the development of fast fault detection algorithm for implementation on micro-processor based relays is pre-eminent. Therefore, the significance of this research, which is the development of DC line protection algorithms, need not be over emphasised. Since no such protection algorithm exists at present (except at the research stage), this research addresses this challenge by developing a DC line protection algorithm for application to future and proposed HVDC grids.

1.4 Scope and Limitations of the Research

This research focuses on the characterisation and detection of faults (or short circuits) on the DC link in HVDC grids. For this purpose, two main types of DC short circuits were considered, namely pole-to-pole (*P*-*P*) faults; pole-to-ground (*P*-*G*) faults. Studies were carried out for wider cases of fault scenarios including varying fault distance and varying fault resistances. The effect of boundary characteristics such as the DC link inductors on the fault current and voltage profile was also investigated. The effect of lightning was not considered in this research as the DC links are assumed to be underground cables and as such not susceptible to lightning. It was assumed in this study that any transients on the AC side will be significantly attenuated and therefore downgraded before arriving at the relay terminals located on the DC link and as such will not operate. Also, fault

location techniques for DC grids are outside the scope of this research. However, some proposals utilising distance protection strategy have been included as a suggestion for future studies.

1.5 Research Methodology

The methodology adopted in this research project consists of extensive theoretical analysis, simulations and experimentations. The research started with an extensive literature search to keep abreast with the developments in AC and low voltage DC protection philosophy such as DC traction systems. Studies were also extended to two terminal HVDC systems in the first instance, and thereafter to HVDC grids. The aim of this was to fully characterise the fault current with a view to predicting the magnitude and rate of rise. Following this, a novel DC line protection technique utilising "*travelling wave power and energy*" was developed and validated.

The protection technique was implemented in MATLAB and validated on full scale *CIGRE*- four terminal mesh DC grid made available in PSCAD/EMTDC software. However, some modifications were made to the model to reflect the scenarios under consideration in this research. All simulations were carried out in PSCAD and the resulting data was exported to MATLAB work space for post-processing. Following this, the effectiveness of the proposed protection technique for deployment onto a micro-processor based relay was further investigated and proven on a low cost Arduino *UNO ATmega328* Microcontroller board utilising the MATLAB support package. Thereafter, a Compact-RIO FPGA-based experimental platform utilising LabView was also developed to ascertain the suitability of the protection algorithm in practical applications.

1.6 Research Contribution

Generally, the complex nature of future HVDC grids necessitate the need for protection algorithms which are fast in operation and while ensuring overall system security to prevent the converters from damage in the event of fault. It has been established that transient based and non-unit protection are ideal candidates for DC HVDC grids. The outcome of this research has led to the development of a novel DC line protection algorithm for application to HVDC grids. The protection algorithm which has been validated by simulations can easily be implemented in modern micro-processor based relay to provide an autonomous tripping in the event of fault. The protection algorithm does not involve complex mathematical computation and hence would require minimal hardware resources.

The protection principle is based on travelling wave propagation theory, where the "*power*" and "*energies*" developed by the associated travelling wave following the occurrence of fault were extracted for fault identification. In general, the following novel DC line protection technique for HVDC grids utilising travelling wave power/energy components were developed and validated.

i. Directional comparison technique utilising traveling wave power
ii. Directional comparison technique utilising travelling wave energy
iii. Internal fault identification technique utilising travelling wave power
iv. Internal fault identification technique utilising travelling wave energy
v. Internal fault identification technique utilising travelling wave power concavity
vi. A back-up protection principle utilising travelling wave power
vii. A back-up protection principle utilising travelling wave energy

Also, following fault characterisation on HVDC systems, the protection technique utilising current derivative (or *di/dt*) was extensively evaluated in the first instance. The studies carried on *di/dt* revealed some limitations in adopting it for the protection of HVDC grids. These include oscillations in the fault current profile as well as the requirement of a long time window, thereby making it inadequate for the protection of DC lines. These findings were disseminated at the 13th IET International Conference on Development in Power System Protection (DPSP), Edinburgh, 2015.

Generally, the following submission based on the key research contributions were made.

- M. Ikhide; S. Tennakoon; A. Griffiths; S. Subramanian; H. Ha, A. Adamczyk, "A transient based protection technique for future DC grids utilising travelling wave power"; IET Journal of Engineering, 2018 (Accepted for publication)
- M. Ikhide; S. Tennakoon; A. Griffiths; S. Subramanian; H. Ha, A. Adamczyk, "A transient based protection technique for future DC grids utilising travelling wave power"; 14th IET International Conference on Development in Power System Protection (DPSP), 12th – 15th March 2018, Belfast.
- M. Ikhide; S. Tennakoon; A. Griffiths; S. Subramanian; H. Ha "Limitations of *di/dt* Techniques in DC Line protection" 13th IET International Conference on Development in Power System Protection (DPSP), Edinburgh, March 2016.
- M. Ikhide; S. Tennakoon; A. Griffiths; S. Subramanian; H. Ha; "Fault detection in Multi-Terminal Modular Multilevel Converter (MMC) based High Voltage DC (HVDC) transmission system" Universities Power Engineering Conference (UPEC), 2015 50th International Universities, pp1-6, 2015.
- Poster presentation at 8th Universities High Voltage Network Colloquium, jointly hosted by Staffordshire University and *GE* Grid Solutions, Staffordshire University, 14th – 15th January 2015. (Runner up)

- Oral Presentation at the 9th Universities High Voltage Network Colloquium, Cardiff University 14th – 15th January 2016. (Presentation accessible online via: http://www.uhvnet.org.uk/uhvnet2016.html)

1.7 Thesis Overview and Structure

The thesis comprises nine chapters: (1) Introduction, (2) High voltage DC (HVDC) transmission and direct current (DC) grids, (3) Review of protection of DC and AC systems, (4) Fault characterisation in DC systems, (5) Investigation of *di/dt* based protection technique, (6) The theoretical analysis of the proposed travelling wave based protection (TWBP) technique principles, (7) Validation of the travelling wave based protection technique by simulations, (8) Proof-of-Concept (*P-o-C*) implementation of the travelling wave based protection technique and (9) Conclusions and future work.

Chapter one (1) is the introduction written for the sole purpose of introducing the reader to the thesis. It gives the background information, the problem statement, the research aim and objectives as well as the research contributions and achievements made.

In Chapter two (2), a review of HVDC transmission systems and DC grids in general is presented. These include the different topologies of HVDC transmission systems, configurations and technologies. Particular attention was given to the Modular Multilevel Converter (MMC)-based HVDC technology due to its numerous advantages over other types of HVDC converters such as flexibility in voltage control, scalability and amongst others. The development and key drivers for HVDC grids, including the technological gaps in realisation of HVDC is also presented.

In Chapter three (3), the protection systems for DC and AC systems are reviewed. This includes the nature of faults in DC systems and the constraints its interruption compared to the traditional AC systems such as zero crossing issues. The protection principles

applicable to low voltage DC systems such as DC traction systems were also extensively reviewed in Chapter 3. The protection techniques used in conventional HVAC transmissions, two – terminal HVDC systems as well as recent techniques and strategies proposed for HVDC grids that are documented in literature including their relative advantages and disadvantages were also extensively studied in Chapter three (3).

In Chapter four (4), studies carried out on the fault characterisation in DC systems are presented. These include analysis of short circuit in DC traction systems as well as in HVDC systems. Particular attention was given to the fault characterisation in MMC based HVDC systems since modern HVDC grids will be based on this configuration. The simulation results based full scale MMC based HVDC grid is also presented. Simulation results for varying fault distances and fault resistances including the effect of DC link inductors on the resulting current and voltage profile are also presented. The characteristic differences between a *P-P* and *P-G* faults are also detailed in Chapter four (4).

The results and findings of the studies carried out on *di/dt* based protection technique are presented in Chapter five (5). The main conclusion of the work was that the *di/dt* protection technique alone cannot provide adequate protection for the DC line due to the oscillation in the fault current profile as well as the requirement of long window length.

In Chapter six (6), the proposed travelling wave based protection (TWBP) principles technique is presented. The chapter starts with a brief overview of the fundamentals of TWBP principles including derived expressions for the voltage and current travelling wave. Thereafter the derived expression for the proposed protection principles utilising travelling wave power and energy are presented.

In Chapter seven (7), the proposed TWBP technique for HVDC grids was validated based on PSCAD/EMTDC simulations is presented. The results considering wider cases of fault scenarios including long distance/high resistance faults are also presented. The

characteristic differences between a forward directional fault (FDF) and a reverse directional fault (RDF) as well as that between an internal fault and external fault were established.

In Chapter eight (8), the proposed TWBP technique was implemented both on a low cost experimental platform using *ATmega328* Microcontroller as well as in a Compact RIO experimental platform.

The thesis concludes with Chapter nine (9) with some recommendation for future work.

Chapter 2

2 High Voltage DC Transmission (HVDC) and Direct Current (DC) Grids

2.1 Introduction

In this chapter, a review of High Voltage DC (HVDC) transmission systems and direct current (DC) grids are presented. It starts with an overview of HVDC transmission systems in general including the different modes of connections and topologies. Following this, DC grids are introduced. This includes the technical and economic advantages derived from DC grids as well as the key drivers towards its development. To ascertain the most efficient and suitable HVDC converter technologies for offshore wind farm integration, the Line Commutated Converter (LCC) and the Voltage Source Converter (VSC) technologies were extensively researched. Attention was given to the Modular multi-level Converter (MMC) type VSCs. The chapter concludes with an overview of the technical and economic challenges in developing and realising DC grids.

2.2 HVDC Transmission Systems

HVDC is a system interconnecting two AC networks and utilises power electronics technology to convert AC voltage to DC voltage, and vice versa. HVDC links are suitable for integrating offshore wind farms to onshore substations, supplying oil and gas offshore

platforms as well as interconnecting power grids in different countries as well as reinforcing existing networks [2][11][12].

2.2.1 Advantages of HVDC over HVAC

Generally, for long distance power transmission, HVDC system is the preferred option due to its technical and economic advantages, which are [2][11]

- absence of capacitive charging and discharging on the DC lines/cables thus enabling the bulk transport of electricity over long distances,
- interconnection of grids by enabling the exchange of power between two asynchronous systems (two networks of different frequencies)
- prevention of cascading disturbances between connected AC networks, by so doing improving quality and stability as well as maximising network performance
- controllable power transfer between different nodes in an electricity market

Furthermore, conventional HVAC systems require three cables whereas HVDC require two cables to transport power, thus reducing transmission costs as well as minimising losses. In an analogous way, modern HVDC cables are designed to have reduced weight and dimensions, which results in higher power density [13]. This implies that the power that can be transported per kilogramme of cable in HVDC *light* cables is higher than in HVAC cables[13]. A comparison of the losses and cost associated with HVDC and HVAC transmission systems is shown in Figure 2.1. Figure 2.1(a) shows a comparison of the losses in 1200km overhead transmission line using HVAC and HVDC transmission systems. However, in terms of investment costs, the initial capital cost for HVDC transmission system is higher than that for HVAC system. This is largely due to the cost of the converters and other associated devices such as filters. However, as shown in Figure. 2.1(b), for over a critical distance, the HVDC systems becomes more economical

than HVAC system. The breakeven point for this is approximately 50km for cables and 700km – 800km for overhead transmission line (OTL) [12].

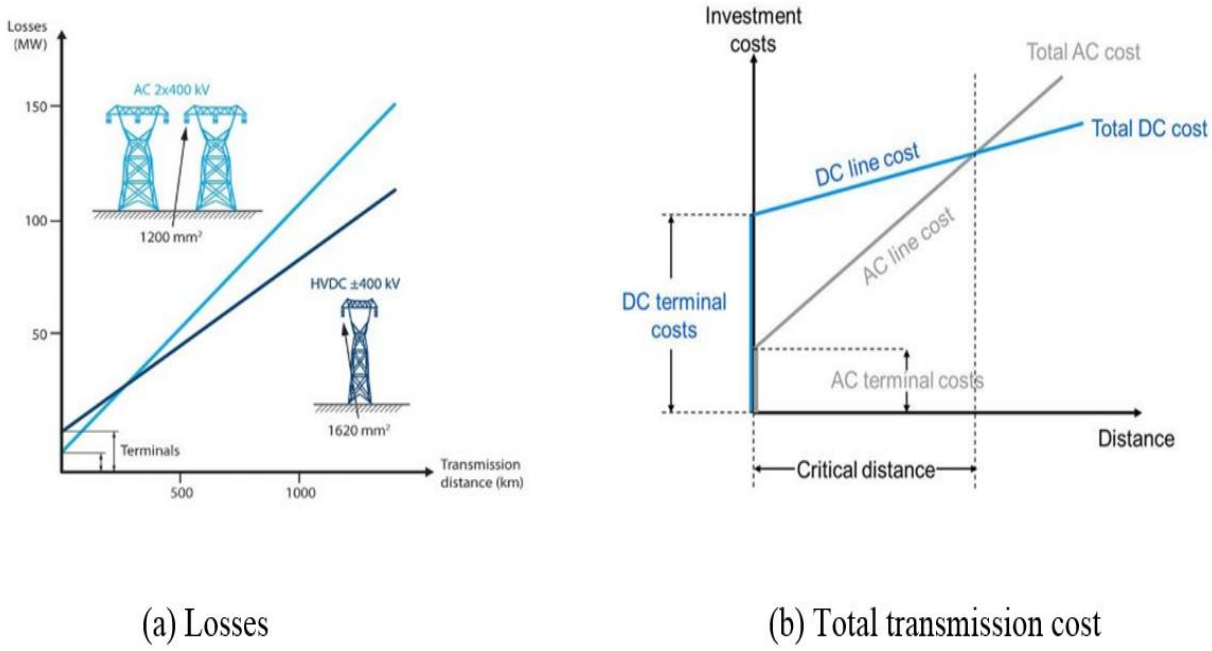


Fig. 2-1 *HVDC versus HVAC Transmission Systems* [12].

2.2.2 HVDC Connections

In terms of connections, HVDC system can generally be classified as *back-to-back, point–to-point connections.*

The back–to-back connection: This is used to interconnect two transmission systems of different and incompatible electrical parameters (such as voltage level, frequency or short-circuit power level) and at zero transmission distance (the rectifier and inverter are in the same place). Once the system is interconnected, the two systems' daily and seasonal cost differences can also be optimised[14]. Generally, back-to-back HVDC connections serves the following purposes[14], [15].

- Interconnecting asynchronous high-voltage power systems.
- Stabilising weak AC links

- Supplying more active power to other AC system with limited short circuit capacity
- For grid power flow control within synchronous AC system
- limiting the spread of cascading faults as well as providing increased system flexibility relative to new generation requirements

A schematic diagram of the back-to-back HVDC system is shown in Figure 2.2. Practical example of back-to-back connected HVDC systems is the 500 MW back-to-back HVDC station in the central Indian state of Madhya Pradesh interconnecting the 400 kV AC system of the Northern and Western regions (Figure 2.3).

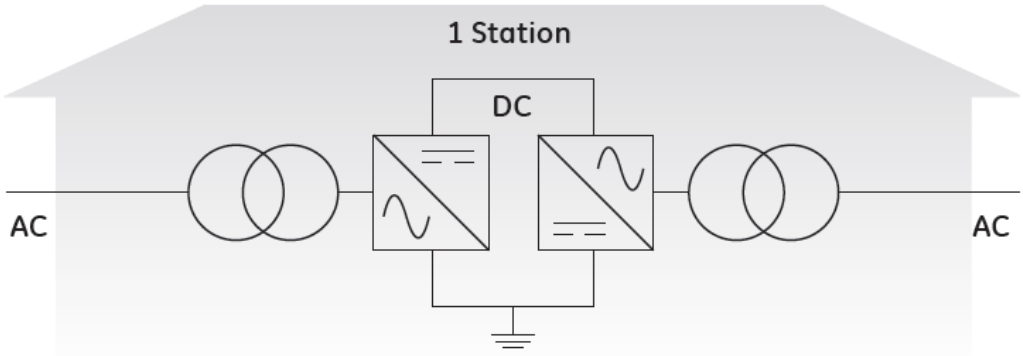


Fig. 2-2 *Back-to-Back HVDC transmission systems*[14]

Other examples include:

- the connection between Brazil and Argentina, located in *Garabi* and with a rating of 2,200MW interconnecting the 400kV AC networks on both sides[16].
- the 2,000MW England–France interconnector linking the British and French transmission systems[17].

- the 1,000MW *BritNed* interconnector linking Britain and The Netherlands[18].

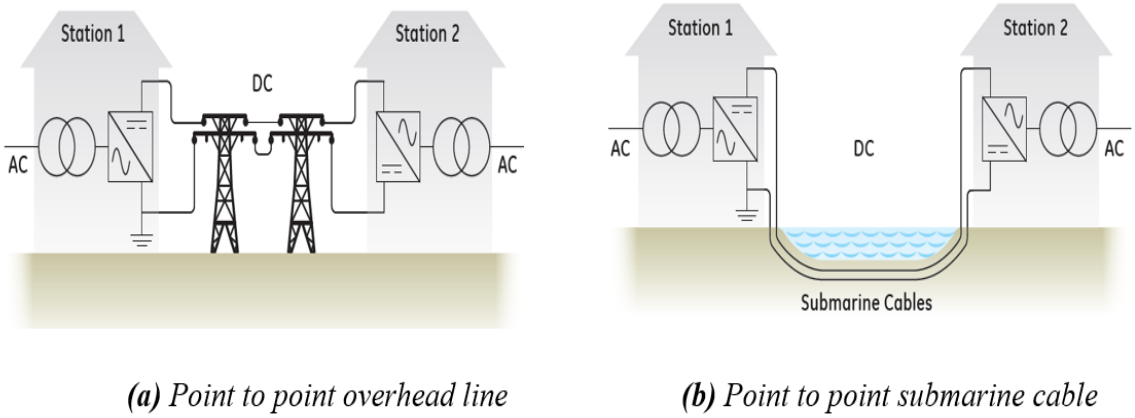
Fig. 2-3 *500 MW back-to-back HVDC station in the central Indian state of Madhya Pradesh*

The point-to-point connection: This is used to transmit power over long distances, typically from one location/region to another. The schematic diagram is shown in Figure 2.4. Other possible connections of HVDC systems which have attracted attentions in recent years are *multi-terminal connections* and *DC grids*. In both cases the DC link interconnects more than two converter stations thus ensuring more flexibility than the two-terminal connection. DC grids can either be in the form of a *radial connection* or in a meshed form. Details of their configurations including their relative advantages and disadvantages are presented in section 2.4

2.2.3 HVDC Configurations

In terms of topology, HVDC converter can be classified into two categories viz: *monopolar* and *bipolar* configuration (Figure 2.5). However, for this study, it is classified as follows.

- *Asymmetrical monopole configuration*
- *Symmetrical monopole configuration*
- *Bipolar configuration*



***(a)** Point to point overhead line* ***(b)** Point to point submarine cable*

Fig. 2-4 *Point-to-point HVDC transmission systems*[14].

***(a)** Monopolar configuration* ***(b)** Bipolar configuration*

Fig. 2-5 *HVDC configurations*[15]

As shown in Figure 2.6, a system is said to be in an asymmetrical monopole mode when one conductor is at a high potential relative to the other (and generally at a ground potential). However, in a symmetrical monopole operation, both conductors are at a high potential with one being positive and the other negative.

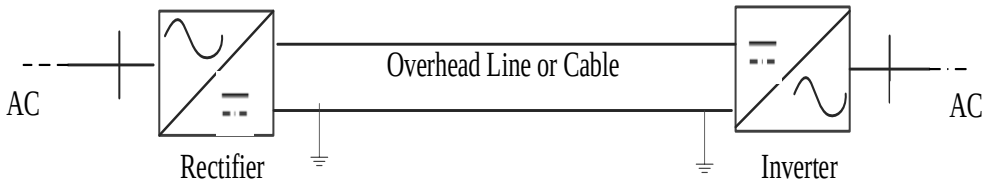


Fig. 2-6 *Asymmetrical monopole HVDC transmission Systems*

In a symmetrical monopole configuration (Figure 2.7), each converter produces symmetrical voltage under steady state operating condition. A high impedance earth path is provided via the AC side of the converter. As the DC side is not directly connected to ground, the impedance to earth is high [19].

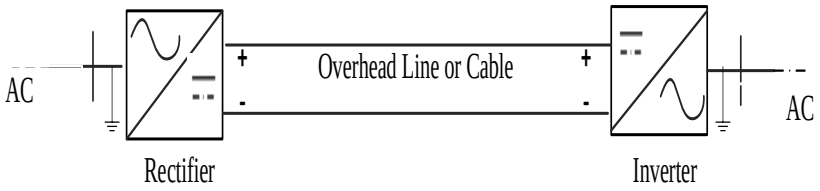


Fig. 2-7 *Symmetrical monopole HVDC transmission systems*

Generally, monopolar HVDC configuration is used for power ratings up to 1500 MW [15]. However, two asymmetrical monopole converters can be connected in series to form a bipolar configuration, with a metallic or ground return providing a return path and having the capability of ensuring continuity of service when a pole is out of service. The general schematic diagram is shown in Figure 2.8. This arrangement gives two independent DC networks, each capable of half power transfer capacity.

Under normal operating conditions, power flows through the lines/cables and negligible current flows through the return path (earth electrode). Generally, they are used when the required transmission capacity exceeds that of a monopolar arrangement or when greater energy availability is required.

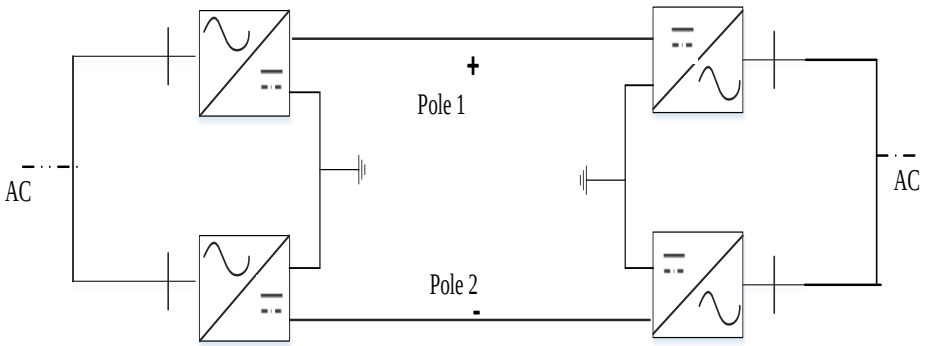


Fig. 2-8 *General configuration for a bipolar HVDC Configuration*

They are also used when it is necessary to split the power capacity between two poles due to lower load rejection power. During routine maintenance or in case of outages of one pole, part of power can still be transmitted using the unfaulty pole. This type of configuration offers power up to 10GW. The normal state of operation is shown in Figure 2.8. However, during a DC line fault in one of the links, the faulty pole will be isolated and the current in the healthy pole will be taken over by the earth return path as shown in Figure 2.9. Furthermore, during a pole outage such as in the case of converter fault, current can be commutated from the earth return path to the conductor provided by the faulty pole as shown in Figure 2.10[15]. Generally, the bipolar configuration with a dedicated metallic return are used for relatively shorter distance transmissions or when there are limitations imposed on the use of ground return electrodes[15].

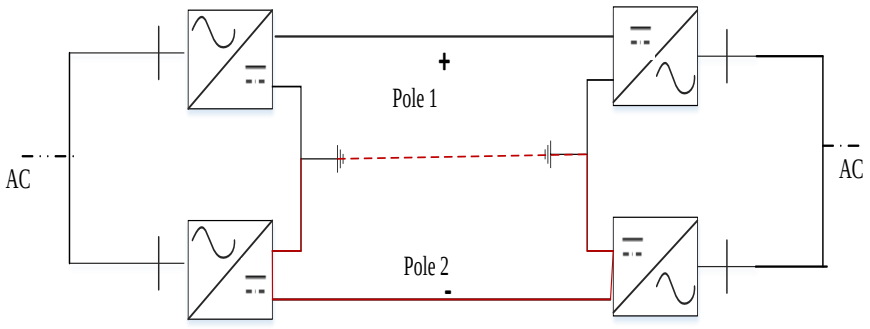


Fig. 2-9 *Operating mode of a bipolar HVDC system during a DC side fault* [15]

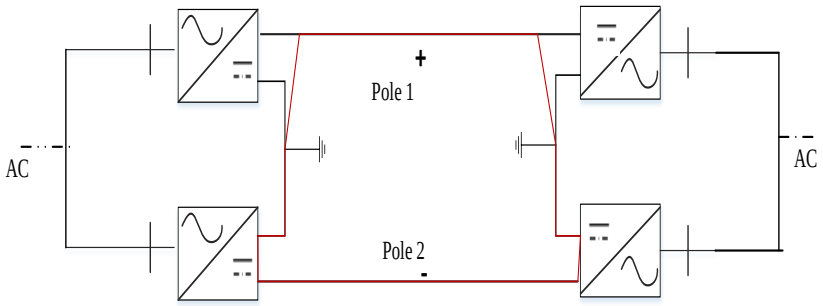


Fig. 2-10 *Operating mode during a pole outage such as converter internal fault* [15]

HVDC system could also be interconnected to form the so called multi-terminal HVDC system or DC grid. DC grids can either be radially interconnected or ring connected (or Meshed). These are explained in detail in section 2.4

2.3 HVDC for grid integration of wind farms

Generally, for transporting electrical energy generated offshore over shorter and medium distance, the transmission to the shore can be achieved using HVAC interconnections. A typical arrangement is shown in Figure 2.11, where the generated voltage at say *25kV* is stepped up by an offshore substation to say *72kV* or more. This is then transmitted via an AC subsea cable until it is stepped down to the required system voltage by an onshore substation transformer. However, as indicated in section 2.2.1, as the transmission distances increase, it becomes uneconomical to transport electrical power using HVAC interconnections. This is due to the high transmission losses due to the energy required to charge and discharge the line or cable capacitances. Therefore, HVDC is the only feasible option for the integration of offshore wind farm into the transmission system. Generally, future offshore wind farm will be located further into the sea than they are today due to the requirement for space and the need minimise the effect of wind speed variability. A schematic diagram of an offshore wind farm connecting to an AC network via an HVDC link is shown in Figure 2.12

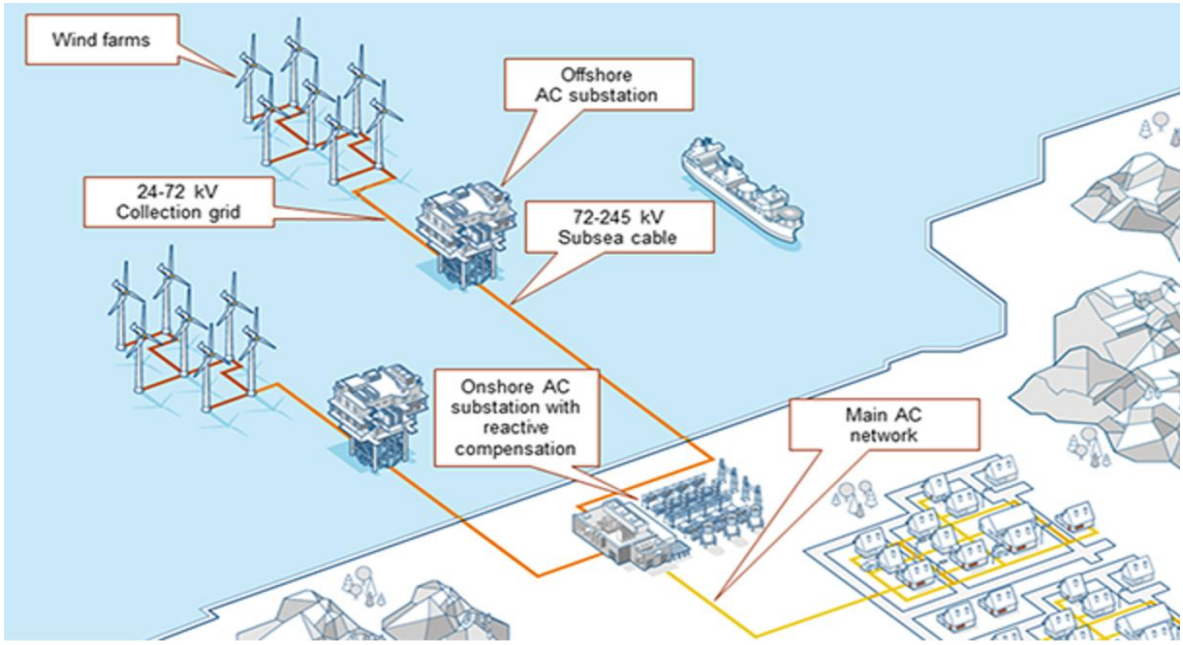


Fig. 2-11 *Offshore windfarm integration using HVAC interconnections*[20].

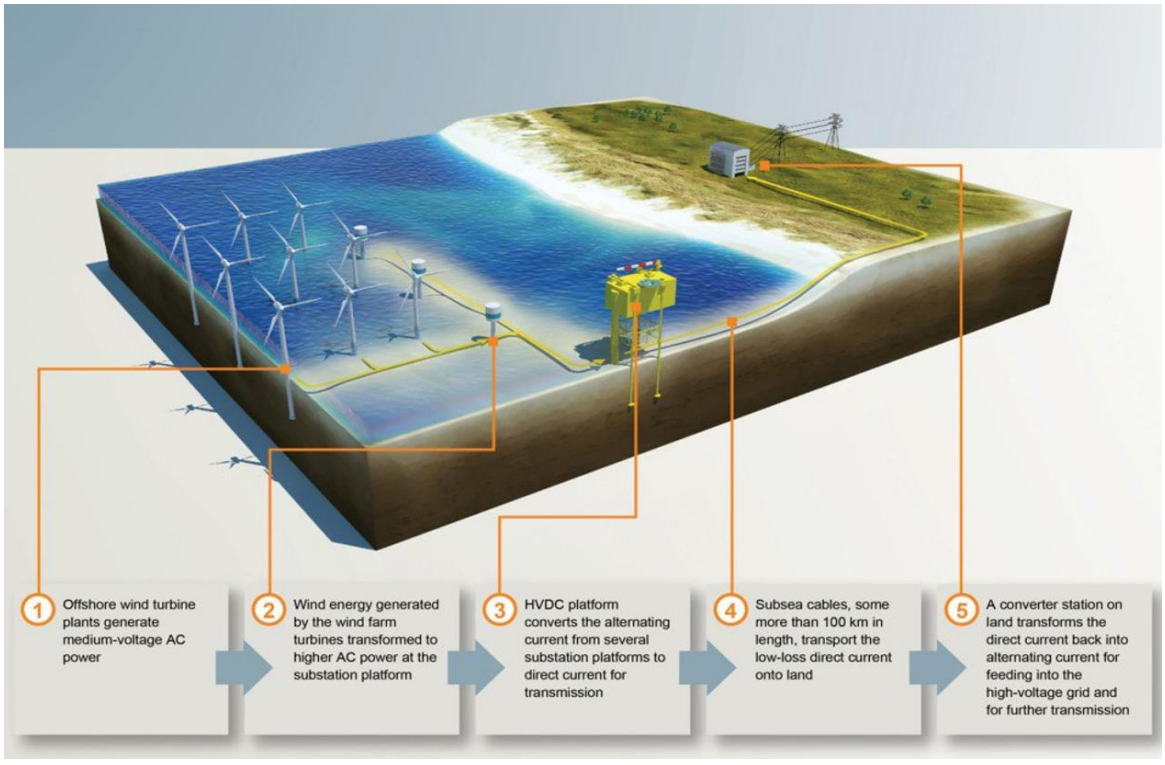


Fig. 2-12 *Offshore windfarm integration using HVAC interconnections*[21]

As shown, the electricity generated from the offshore wind farm is transmitted as an AC to an offshore converter station which converts it into HVDC and fed to the mainland via

a subsea cable. The land based converter station converts the DC back to AC for onward transmission to the HVAC grid. Owing to the advantages such as reduced losses and higher transmission capacity of HVDC over HVAC, there has been significant developments in HVDC interconnected offshore wind farms across the world.

2.3.1 Offshore Wind farm in Europe

Generally, the development of offshore wind farm with HVDC interconnections has already started in the North Sea and there are plans for future expansion. In Europe for example, approximately 1558 MW of new offshore wind power capacity was grid-connected in 2016. A net addition of 338 new offshore wind turbines across six wind farms were grid-connected from 1 January to 31 December 2016 [22]. The total installed capacity of offshore wind power in Europe to date is 12,631 MW from 3,589 grid-connected wind turbines in 10 countries. Figure 2.13 shows the Dolwin3 project expected to be completed in 2017. This project is currently being carried out by General Electric and will be the third grid connection in the DolWin wind farm cluster in the south western region of the North Sea[23].

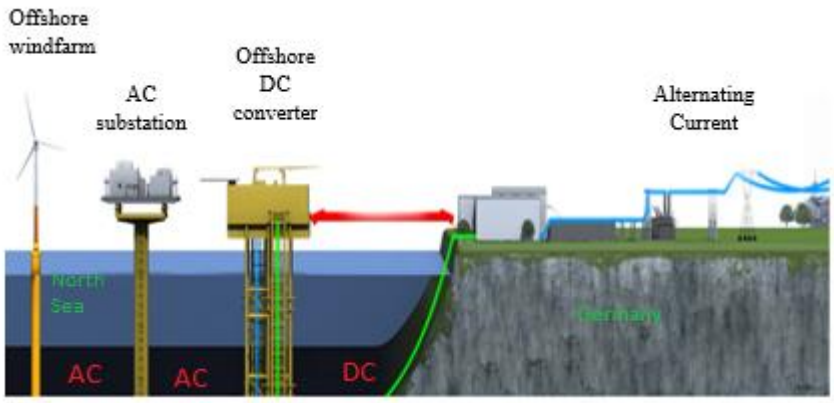


Fig. 2-13 *Schematic diagram of Dolwin3 Project*[23]

It has a rating of 900MW, 320KV with a total DC cable length of 162km. The generated power at the sea is delivered to the mainland using a subsea cable of 83 km. From the coast, the wind power will then be transported a further 79 km using an underground cable to the converter station in Dörpen/West in Lower Saxony (Germany) [23]. Upon completion, this project is expected to supply around one million households in Germany.

2.3.2 Offshore Wind farm in UK

The UK generates more electricity from offshore wind than any other country in the world. The sector is meeting around 5% of annual UK electricity requirements and this is expected to grow to 10% in 2020. At present, the UK now has 29 offshore wind farms, with a total of 1500 turbines generating over 5.1GW of operational capacity. This capacity is enough to power 4million homes. At present, a further 4.5GW capacity is under construction[22]. A map of UK showing the activities of offshore wind farm to date is shown in Figure 2.14. At present, the UK had a total operational capacity of 6.9 GW. Assuming a 30% average output, this corresponds to

$$6.9 \times 0.3 \times 24 \times 365$$

$$= 18\text{TW-h (Approximately)}$$

Now, with UK annual demand of 400TW-h, this value corresponds to 4.5% of the total UK energy demand. (Neglecting network losses of about 8% of total demand)

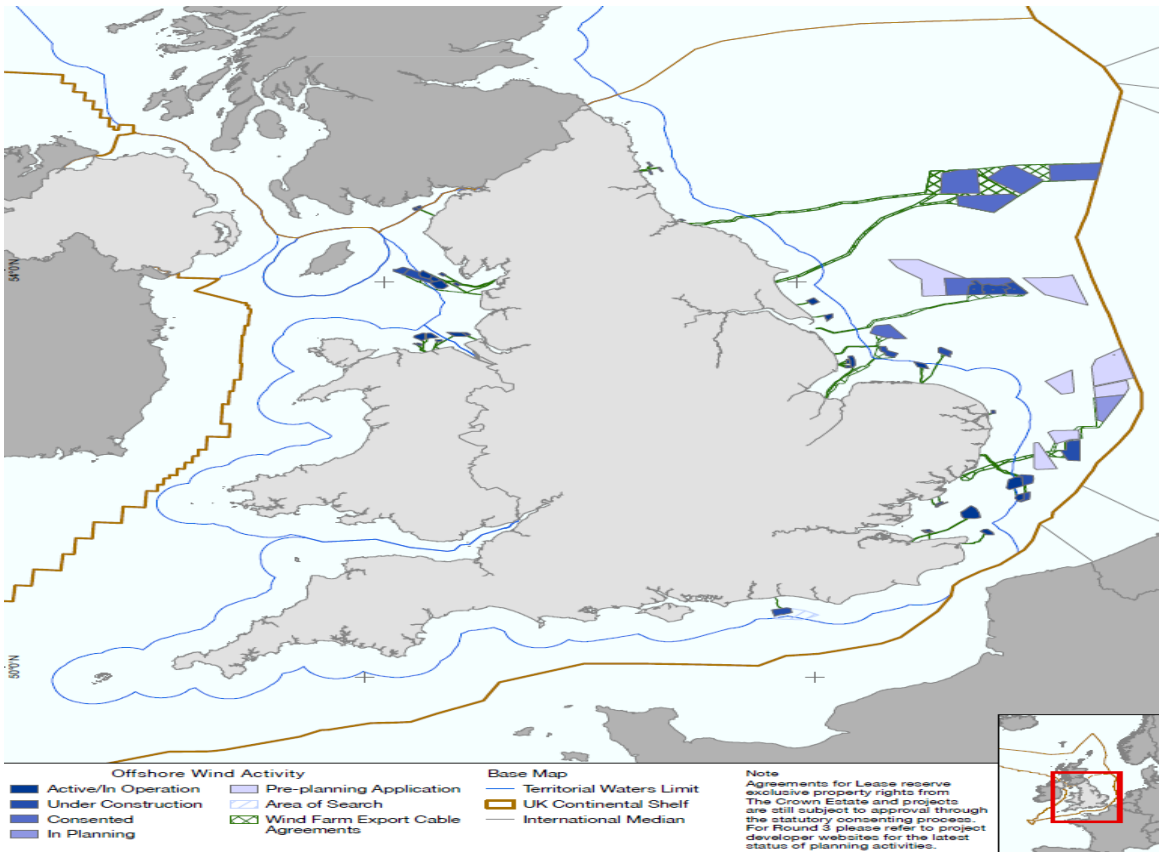


Fig. 2-14 *Offshore wind farm activities in UK* [22].

2.4 Multi-terminal HVDC and DC grids

For enhanced reliability and functionality as well as minimising conversation losses and saving costs, HVDC network can also be interconnected to form a multi-terminal network. Theoretically, this can either be achieved by either connecting the converters in series or in parallel[24], however only the parallel scheme has been practically proven. As shown in Figure 2.15, four converters are connected in parallel; comprising two rectifiers and two inverters thus given more flexibility and reliability, and improved power transfer capacity.

In parallel operation (Figure 2.15), all parallel converters are connected to the same bus. Therefore, the DC link voltage is a common parameter for all converters, but with differences in the voltage drop which is largely due to the DC line load current. Ideally,

all converters connected in parallel are provided with voltage and current control capabilities. However, as there is only one DC link voltage, only one converter and often the inverter with the largest capacity controls the DC voltage [24] whilst the other converters control their respective DC currents.

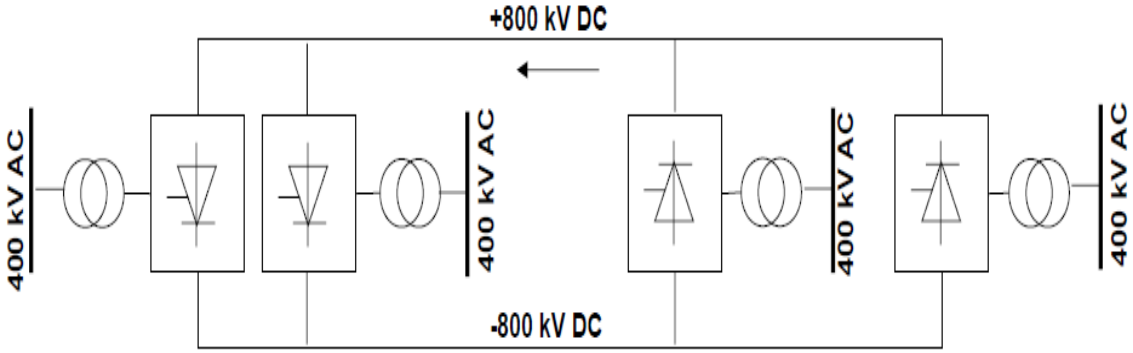
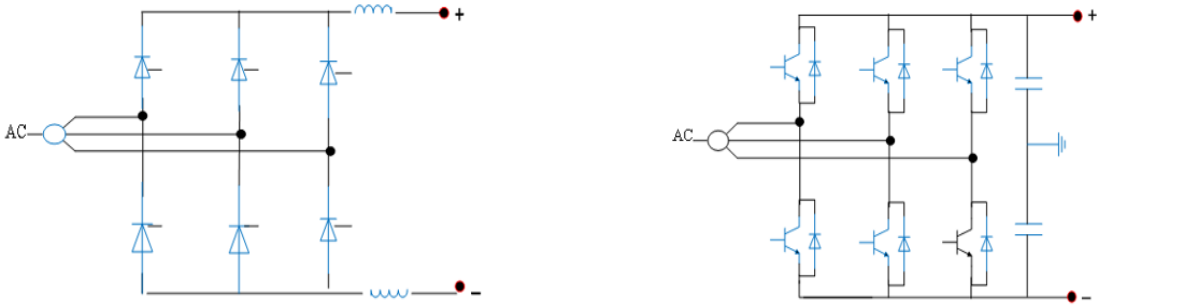


Fig. 2-15 *Multi-terminal HVDC system* [24]

Generally, controlling either the current or voltage has some technical implications and limitations and can be achieved by either of the two HVDC converter technologies viz: the *line commutated converter* (LCC) and the *voltage source converter* (VSC) technologies but with each having its own relative advantages and disadvantages.



(a) *Line commuted converter, LCC* ***(b)*** *Voltage source converter, VSC*

Fig. 2-16 *Types of HVDC converters*[2]

LCC are based on thyristors whilst VSCs are based on Insulated Gate Bipolar Transistor (IGBT) which are self-commutating. Generally, LCC are almost exclusively used for

point-to-point transmission based HVDC systems. In practice, they are usually fitted with a large DC side inductance connected in series with the line (Figure 2.16), and as such are robust to DC side faults since the DC side inductance can limit the rate of rise of fault current *(di/dt)* during DC side short circuits[25]. However, a major disadvantage of the LCC for use in MT-HVDC system is that power reversal can only be achieved by reversing the voltage polarity, hence making it impossible to operate each converter station independently as either a rectifier or an inverter without changing the polarity of the DC pole voltages. This capability is a key requirement for interconnecting several converter stations (or regional countries or cities with HVDC links), thus resulting in the so-called HVDC grids; which can either be radially or ring connected (Figure 2.17). For this reason, the use of LCC is limited to parallel HVDC networks (Figure 2.5) but not applicable for use in DC grids (Figure 2.17) since reversing the power will reverse the voltage polarity of the DC bus. Generally, unlike the multi-terminal HVDC networks shown in Figure 2.15, each converter station in a DC grid must have the capability of operating as either an inverter, or a rectifier

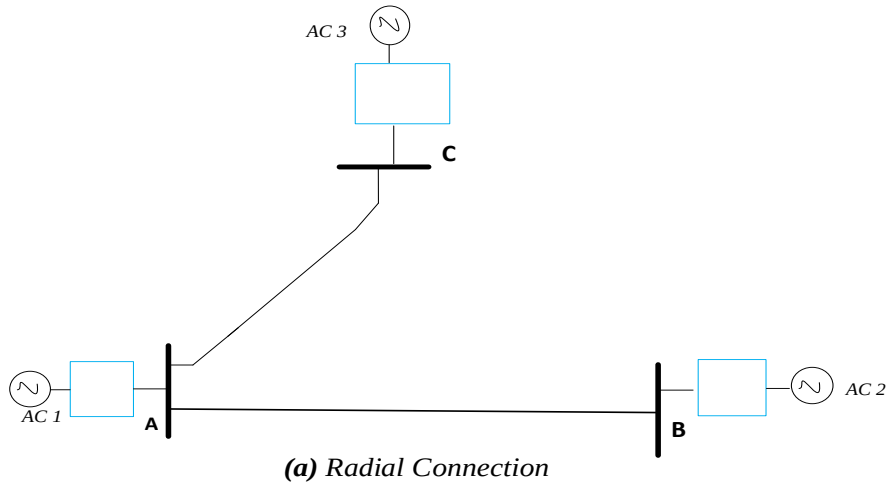
VSC converters have numerous advantages over the conventional thyristor based Line Commutated Converters (LCC) such as black start capability and the ability to independently control active and reactive power. Furthermore, the power flow in VSC - HVDC systems can be independently controlled without changing the voltage polarity thus allowing for a common bus to be used to interconnect several VSCs as well as enabling the use of Cross Linked Polyethylene (XLPE) cables[26]. Generally, as VSC does not require polarity inversion, there is no problem of decrease in the insulation performance, such as space charge influence.

2.4.1 Key drivers for DC grids

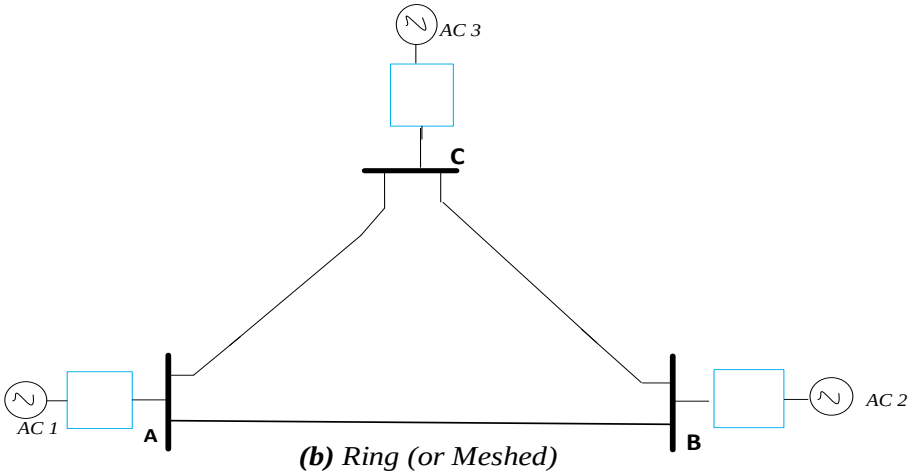
In general, the primary motivation for the development of HVDC grid is the need to interconnect multiple HVDC links and to enable power transfer between all DC terminals. Some of the benefits include better utilisation of assets, better reliability and security of power transfer, better efficiency, and enhanced power trading and increased operational flexibility. In light of these numerous advantages as well as its envisaged capabilities, VSC technology is the only viable option for the development of future HVDC grids.

Key advantages of DC grids are:[3][6] [27][28].

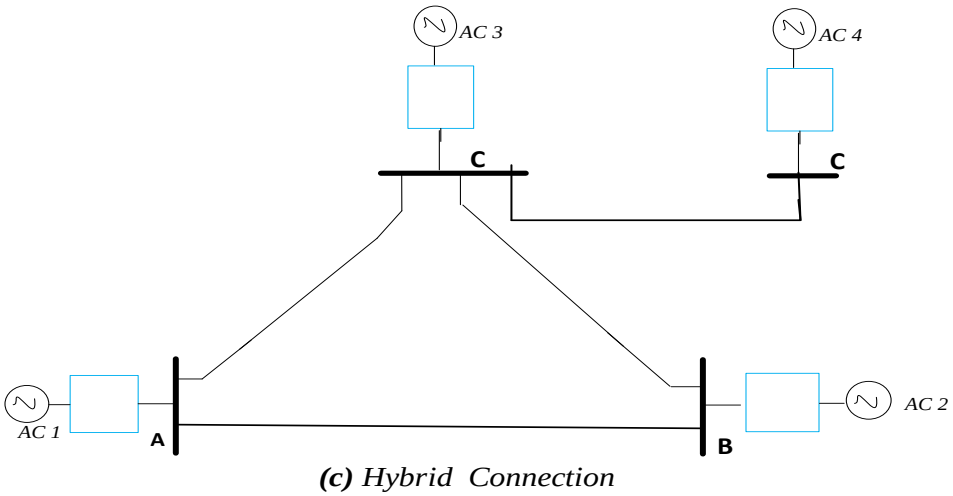
- Better management and integration of renewable energy generation
- Increased grid security
- Enabling cross border energy trading
- Provides more efficient network by reducing reliance on thermal generation
- Enabling the integration of large scale renewable energy sources (RES) Integration
- Enabling the Internal Electricity Market
- Ensuring supply security by complementing micro grids
- Provision of multiple DC lines for the power delivery within the system thus enhancing system redundancy and reliability
- Creating export opportunities for European technology
- Increased availability of the grid, and the reduced construction and operation costs since existing network can be expanded to realise HVDC grid



***(a)** Radial Connection*



***(b)** Ring (or Meshed) Connection*



***(c)** Hybrid Connection*

- Converter Station

***Fig. 2-17** Configurations of HVDC grid*

2.4.2 The European Super Grid

The transmission grids will be more international, crossing different economic zones and national borders. It will also have to be operated and regulated by a mixture of international agencies, national agencies as well as system operators. The grid, which is generally referred to as "*European Super Grid*" would help to create a secure, cost-effective and sustainable power system. A conceptual configuration for the European Super grid interconnecting different regions and countries is shown in Figure 2.18 [29].

Fig. 2-18 *A conceptualized European Super grid* [29].

2.5 HVDC converter technologies

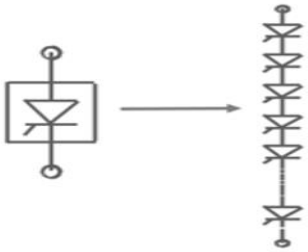
As previously stated, HVDC converters can be classified as either LCC (or CSC) or VSC based.

2.5.1 Line Commutated Converters (LCC)

LCC is a mature cost effective HVDC technology based on thyristor power semiconductors, which enables the bulk transfer of power of up to 8 GW with low losses[14]. Furthermore, due to the large DC inductor located at the line ends, they are inherent DC fault protection. They are available as point to point overhead line and submarine/land cable and is ideally suited for back to back schemes[14]. Traditional HVDC transmission employs LCC with thyristor valves. Such converters require a

synchronous voltage source to operate, and therefore does not possess the capability for a "black start". The ability for a converter to "black start" is an important feature for a DC grid. In that case the converter can be connected to a weak AC system or to an island.

The basic building block used for LCC-HVDC conversion is the three phases, full-wave bridge generally referred to as a six-pulse or Graetz bridge. The term six-pulse is due to six switching operations (or commutation) per period which results in a characteristic harmonic ripple of 6 times the fundamental frequency in the DC output voltage. Details of the operation principles can be found in standard textbooks. As shown in Figure 2.16, each six-pulse bridge consists of 6 controlled switching thyristor valves [30]-[33]



(a) Schematic diagram

(b) Pictorial view

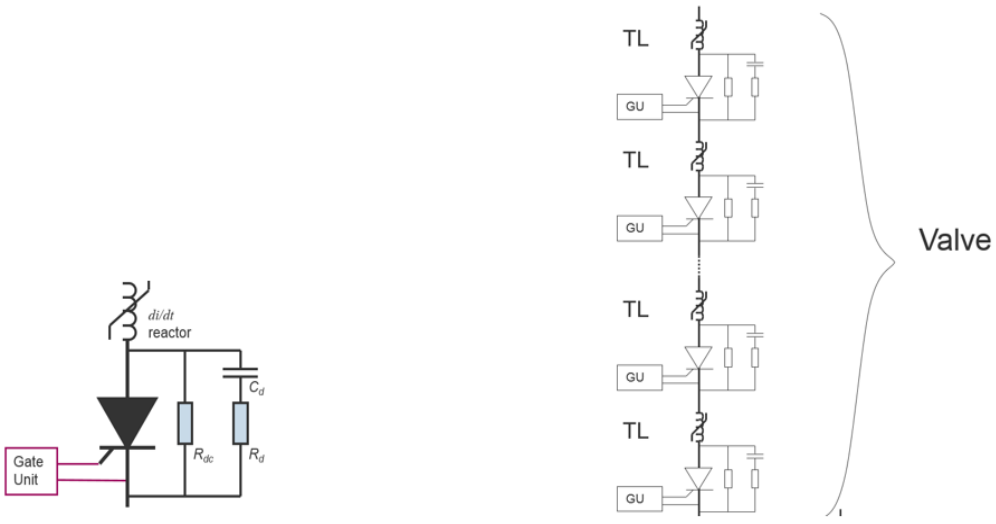
Fig. 2-19 *The thyristor valve*[30][33]

A thyristor valve is a collection of thyristors connected in series (or occasionally series-parallel) to achieve the desired voltage level. The term 'valve' was derived from early HVDC schemes which used mercury arc '*valves*' (vacuum devices) to achieve the same

result. A single thyristor (or inverse-parallel pair of thyristors), together with its associated components is referred to as a *thyristor level* (Figure 2.20) [30]. A thyristor level consists of the following

- The thyristor
- The *damping circuit* consisting of the *damping capacitor* C_d and a *damping resistor* R_d,
- The *grading circuit* comprising the *grading resistance*,
- The *di/dt* limiting reactor and the gate firing circuit.

The gate firing pulse is supplied via an optical fibre. The damping or *snubber* capacitor, C_d helps to handle the voltage overshoot during turn off. The damping or *snubber* resistor, R_d helps to damp oscillations caused by the combination of snubber capacitor and the circuit inductance. The *di/dt* reactor can also be lumped together as shown in Figure 2.21.

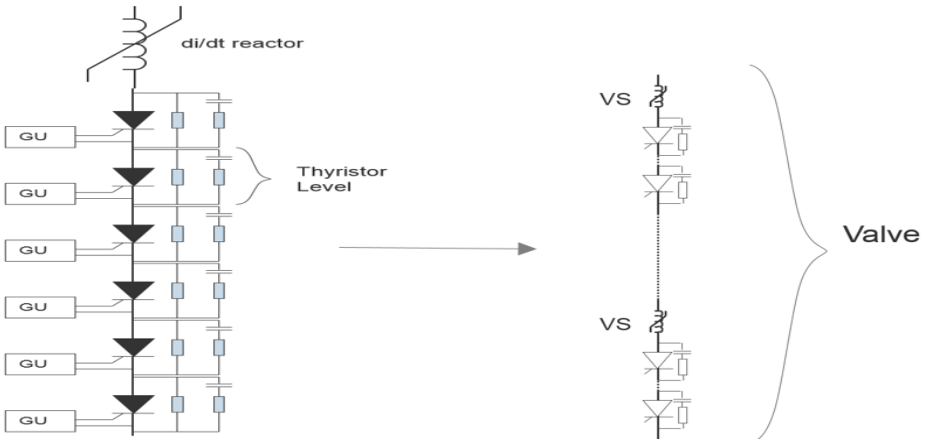


***(a)** Thyristor Level (TL)* ***(b)** Thyristor Valve*

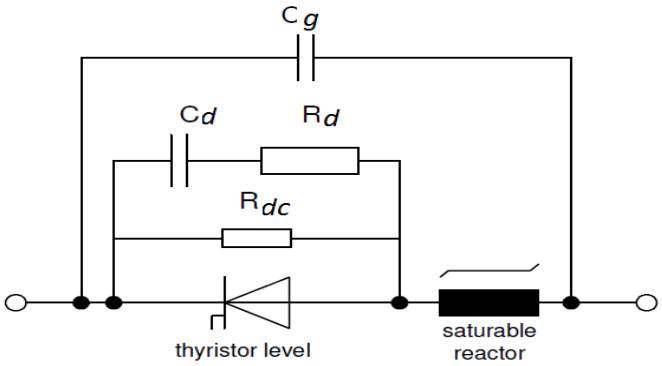
Fig. 2-20 *A thyristor level*[30]

The grading resistor R_{dc} ensures equal voltage distribution among the series connected thyristors. The di/dt limiting inductor limit the *di/dt* stress of the thyristors at turn on as well as limiting the dv/dt during transients in the off state[31]. Also, for steep voltage

transients, an uneven voltage distribution between thyristor levels would result. To control this unbalance, grading capacitors, C_g are usually connected in shunt to the series connection of thyristor levels and valve reactors as shown in Figure 2.21b[31]. The DC terminals of two six-pulse bridges with AC voltage sources displaced by 30^0 can be connected in series to increase the DC voltage and eliminate some of the characteristic AC current and DC voltage harmonics. This is referred to as 12 pulse arrangement. In 12-pulse operation, the characteristic AC current and DC voltage harmonics have frequencies of 12n ± 1 and 12n, respectively. The 30◦ phase shift is achieved by feeding one bridge through a transformer with a star-connected secondary and the other bridge through a transformer with a delta-connected secondary [32].



(a) With lumped di/dt



(b) Thyristor level showing grading capacitor

Fig. 2-21 *A thyristor level with lumped di/dt reactor*[30][31]

Most modern LCC based HVDC transmission schemes utilise 12-pulse converters to reduce the harmonic filtering requirements required for six-pulse operation; e.g., 5^{th} and 7^{th} on the AC side and 6^{th} on the DC side. Generally, harmonic currents flow through the valves and the transformer windings, but cancels out on the primary side of the transformer since they are they are 180° out of phase (Figure 2.23). As shown in Figure 2.24, the thyristor valve is clamped together with a clamping straps and with a clamping force of about $135kN$. The entire valve structure is suspended from the ceiling of the valve hall via porcelain insulators.

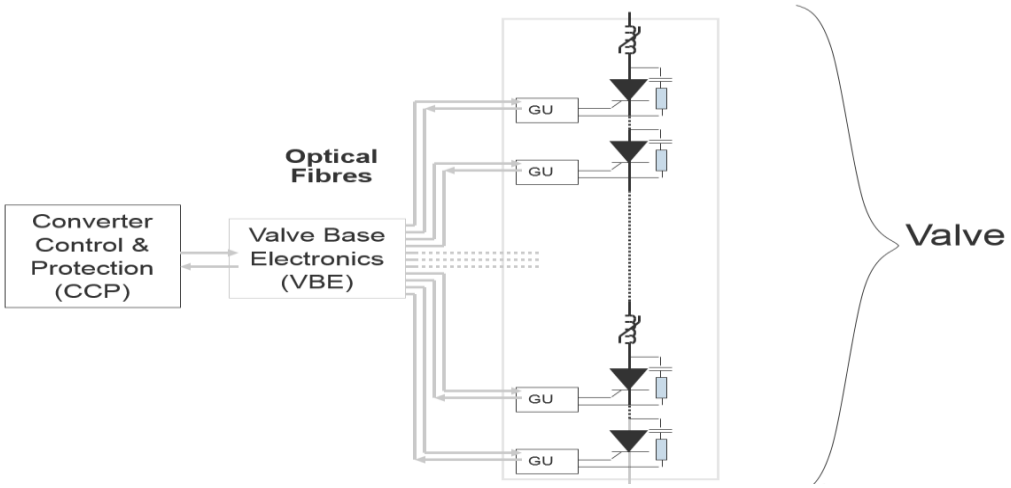
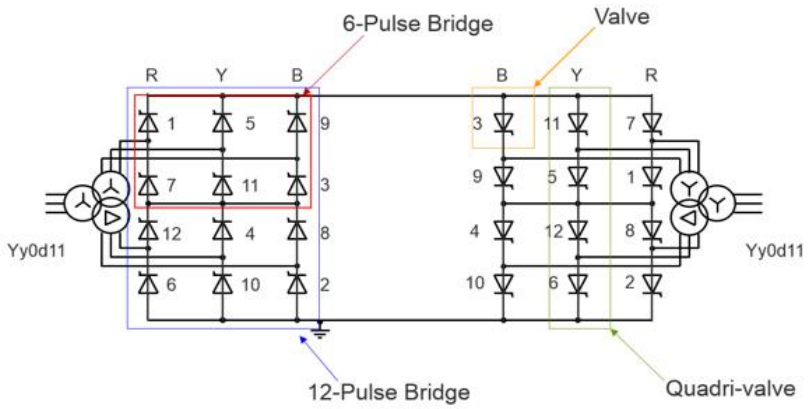


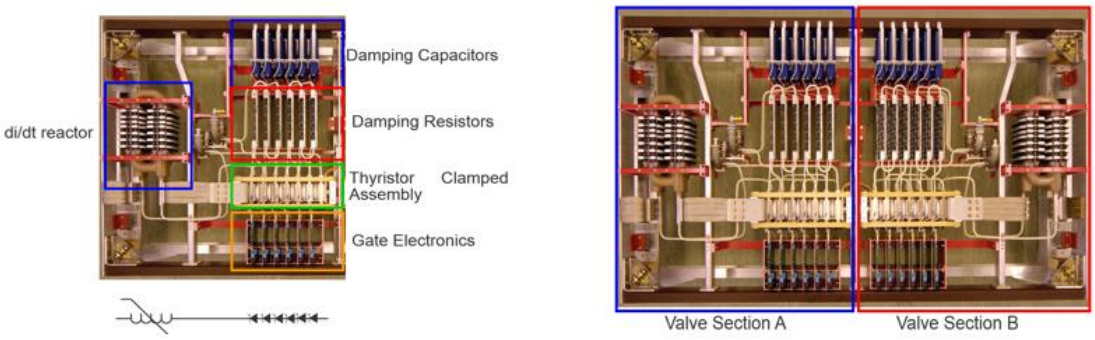
Fig. 2-22 *A thyristor valve showing gate firing circuit*[30]

They are designed to be air insulated, water cooled and suspended indoors in a controlled environment. They are also designed to meet seismic requirements. As earlier stated, LCC requires a relatively strong synchronous voltage source to commutate. The three-phase symmetrical short circuit capacity available from the network at the converter connection point should be at least twice the converter rating for converter operation [32]. Furthermore, LCCs can only operate with the AC current lagging the voltage. Therefore, the conversion process demands reactive power, thus requiring reactive power compensating devices such as shunt banks, or series capacitors. Generally, any surplus or

deficit in reactive power from these local sources must be accommodated by the AC system. Also, any difference in reactive power demand must be kept within given limits to keep the AC voltage within the acceptable tolerance. The weaker the AC system or the further away the converter is from the generation station or source of supply, the tighter the reactive power exchange must be to stay within the desired voltage tolerance.

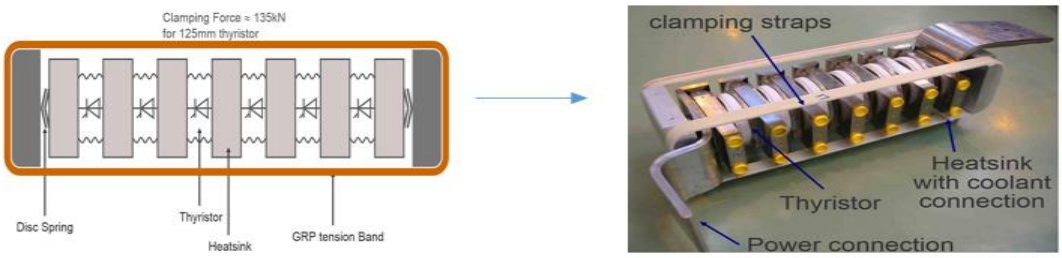


(a) Schematic diagram

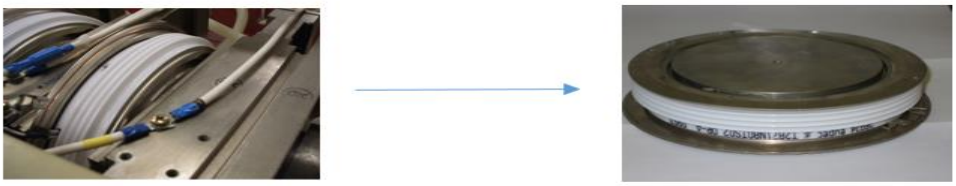


(b) Pictorial View

Fig. 2-23 *12 – Pulse HVDC Converter arrangement* [30]



(a) Thyristor valve in a Clamp



(a) Single thyristor

Fig. 2-24 Thyristor valve assembly[30]

In HVDC thyristor valves, more than 95% of the heat losses are produced in the thyristors, snubber resistors, and valve reactors, hence requiring forced cooling where water is generally used as shown in Figure 2.25. Generally, the mechanical design of an HVDC converter is based on an arrangement of multiple valve towers for one twelve pulse group. For example, in a 500kV converter each valve twin-tower consists of four valves, with each valve comprising three thyristor modules[31]

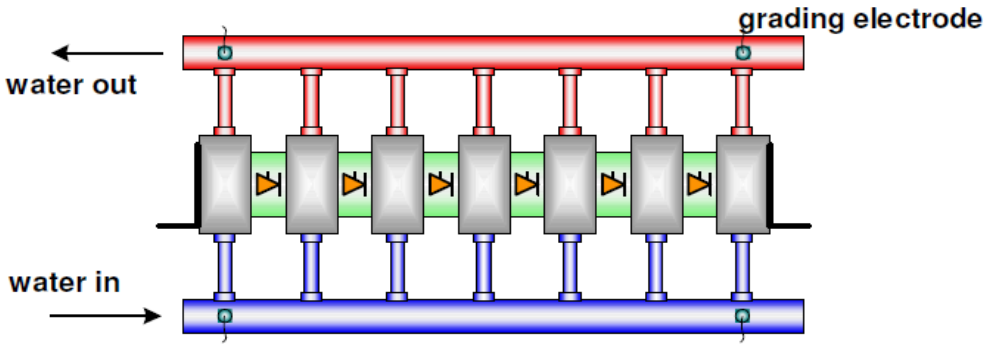


Fig. 2-25 Piping configuration for the cooling circuit of a thyristor stack[31].

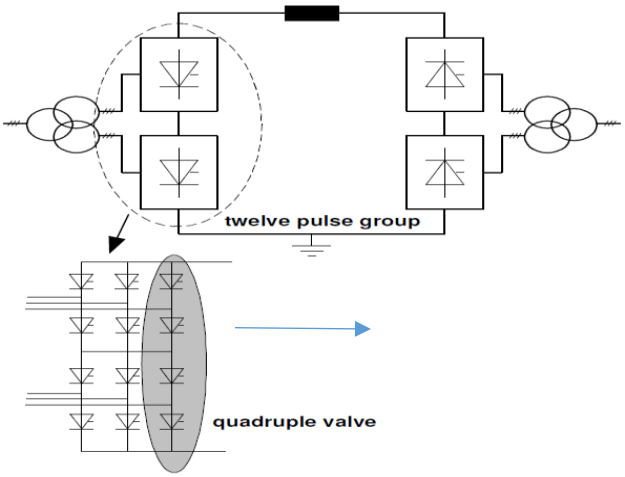


Fig. 2-26 LCC HVDC Converter assembly [32].

The twelve modules are arranged in 6 groups within the suspended twin structure of the tower. The high voltage end is at the bottom and also includes separate corona shields [31] (Figure 2.26). The schematic diagram of a complete LCC HVDC converter station is shown in Figure 2.27.

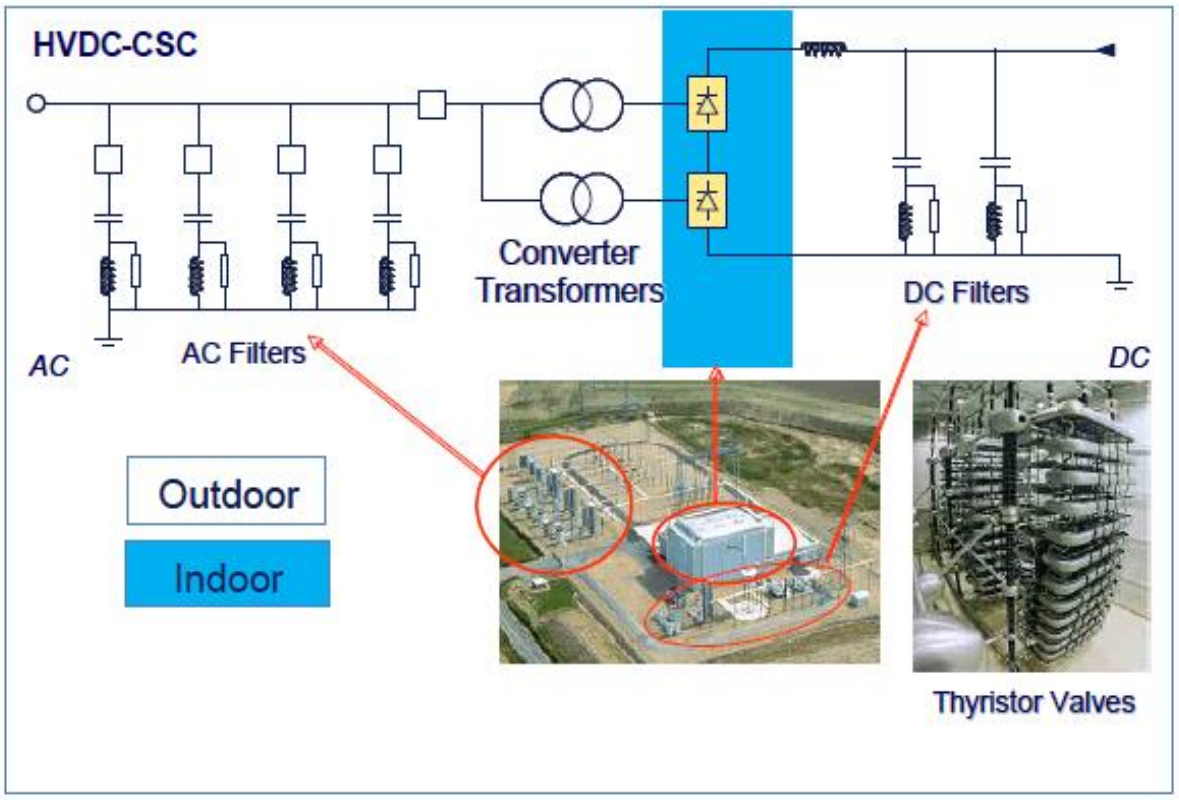


Fig. 2-27 LCC HVDC Converter station [32].

2.5.2 Voltage Source Converters (VSC)

Voltage Source Converter is a newer technology based on power transistors with a lesser footprint compared to LCC technology. They are ideal technology for submarine/land cable interconnection, integrating renewables, offshore and urban infeed applications. They are available as point to point, back to back, submarine/land cable and offshore schemes. VSCs have numerous advantages over the traditional LCC schemes such as creating an AC waveform that allows the scheme to independently control real and reactive power as well as transmitting real power into a very weak AC network, which is not possible with LCC technology[32]

VSCs are based on IGBTs which are self-commutating, and are more flexible and controllable compared to the LCCs. The use of IGBT's eliminates the risk of commutation failure. It also can absorb and generate both active and reactive power

independently of one another, thus eliminating the requirement for the expensive reactive power compensators as in LCC based HVDC. Other advantages of LCC are that there is no requirement for regulation of the short-circuit level as commutation can operate without an AC system voltage source, the generation of harmonics is greatly reduced thus minimising the volume of filters required to absorb them[32].

Also unlike the LCC based HVDC technology, an important and key feature of the VSC is the capability to '*black-start'*. That is, the ability to restore power without an external power supply. This gives VSCs the capability to supply weak AC system or an island. This is an important feature in the integration of a wind farm. Furthermore, unlike conventional HVDC transmission, VSCs have no reactive power demand and can control their reactive power to regulate the AC system voltage as in the case of a generator. A typical layout for a VSC based HVDC converter station is shown in Figure 2.28.

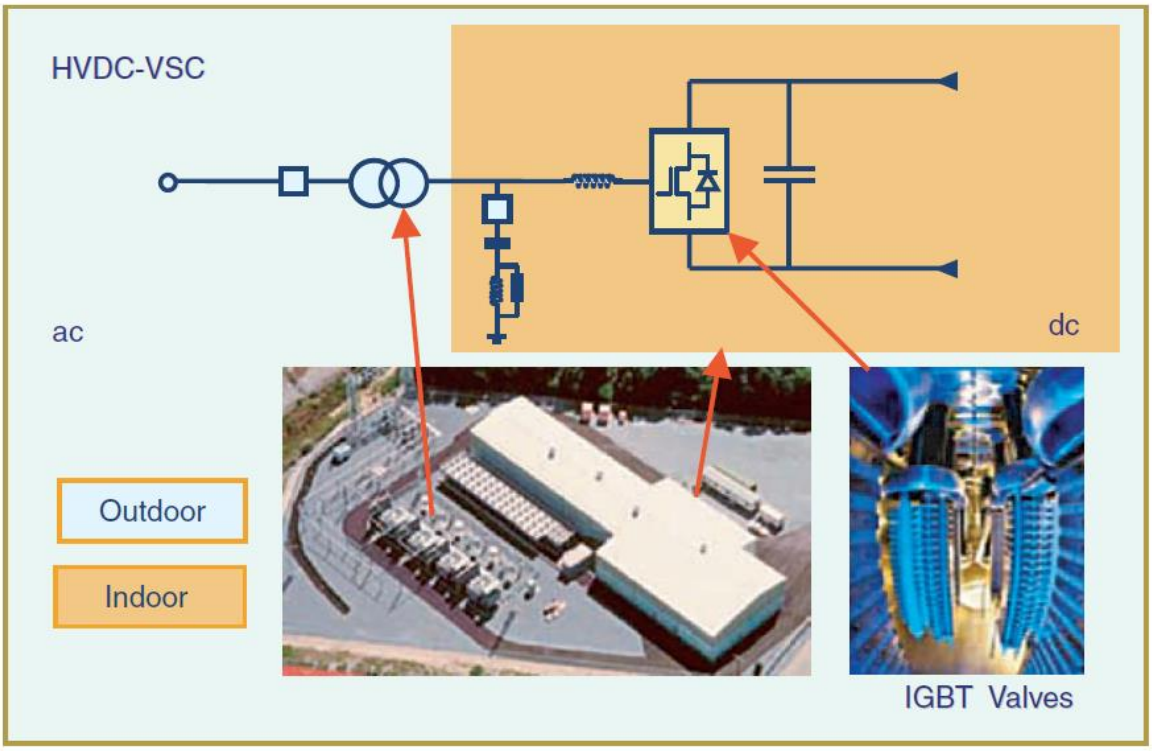


Fig. 2-28 VSC HVDC Converter station [32]

Principle of voltage source converters

VSC is a power electronic circuit that produces an AC output from a DC voltage source (Figure 2.29). It can either be operated as a Voltage Source Inverter (VSI) or a rectifier with a fixed DC source. When a VSC is used in inverter application, the DC source voltage is obtained by using a VSC as a rectifier. VSCs can be classified as either two-level VSCs or multi-level VSCs**.** In two-level VSCs, the peak to peak output voltage is made up of two voltage levels. In multi-level VSCs, the peak to peak output voltage is made up of several voltage levels. The two-level VSCs can further be classified as *square wave* or *pulse width modulated* (PWM) VSCs [34].

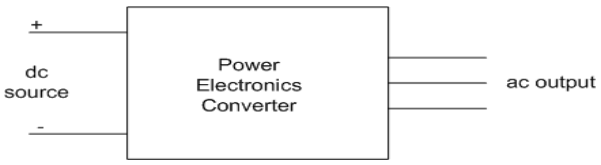


Fig. 2-29 Principle of VSC HVDC

A two-level three phase VSC is shown in Figure 2.30. For high voltage applications, a single power device (IGBT) cannot be used as a switch (or valve) in the VSCs due to their low device voltage ratings (compared to the rated DC voltage). Therefore, IGBTs have to be connected in series to support the voltage.

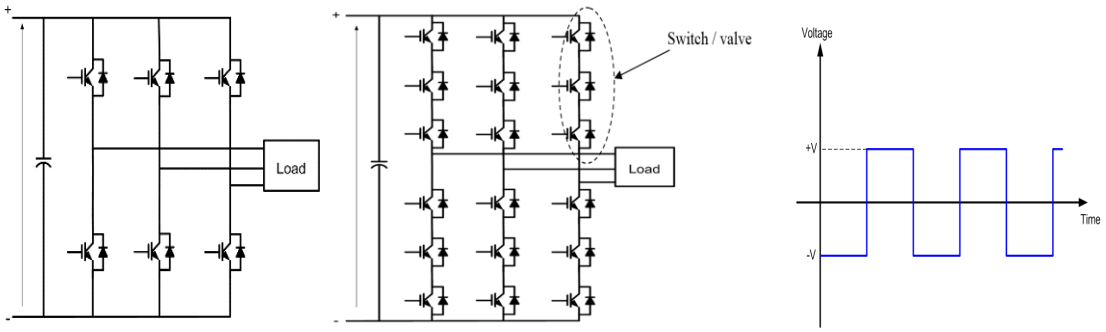


Fig. 2-30 Two level Voltage source converter[34].

The main drawbacks of the series connected IGBT are necessity of static and dynamic voltage balancing of series devices, high *dv/dt* and high harmonic content in the inverter output voltage[34].

In two-level converters, a switch/valve is formed by connecting IGBTs in series so as to attain the desired voltage ratings. In the ideal situation, the DC-link voltage should be equally distributed across the devices; however this is not the case in practical situation. This unequal voltage sharing is mainly due to the spread of device dynamic and static parameters (such as the gate-emitter capacitance, gate-collector capacitance, effective off-state resistance etc), gate drive delays and other external circuit parameters. This results in high dv/dt and higher voltage (above the rated value) across the devices[34]. This voltage unbalance may destroy or thermally overstress (due to higher power dissipation) or accelerate the ageing of series connected devices, which is an undesirable condition for the device. The methods used to solve voltage unbalance issues during the transient state are passive snubber circuits, active gate control circuits and active voltage clamping circuits[34].

Since the output of a two-level VSCs are square wave, PWM techniques are commonly used to generate a nearly sinusoidal waveform. Typically, the gate signals in the PWM VSCs are generated by comparing a reference voltage waveform with a carrier voltage waveform. This arrangement is referred to as *Square wave PWM* (Figure 2.31). Other PWM techniques includes Sinusoidal PWM, Harmonic elimination PWM, Current controlled PWM and Space vector PWM. Details can be found in standard textbooks.

The waveform of Figure 2.31 is a three level VSC. However, several IGBTs can be connected in series to synthesise a nearly sinusoidal waveform. The main advantages of the multi-level converters is lower *dv/dt* compared to the two level VSCs. Examples of the multi-level VSCs are the diode clamped and the capacitor clamped type, Cascaded H-

bridge and Chain-link half-bridge circuits. The schematic diagram of the diode clamped and capacitor clamped type are shown in Figure 2.32. Generally, several IGBTs can be connected to synthesise a nearly sinusoidal AC waveform. Details are outside the scope of this thesis but are available in literature. However, the major disadvantages is the requirement of complex control technique to synthesise the desired AC voltage which also results in high switching losses and harmonic problems[30], [34].

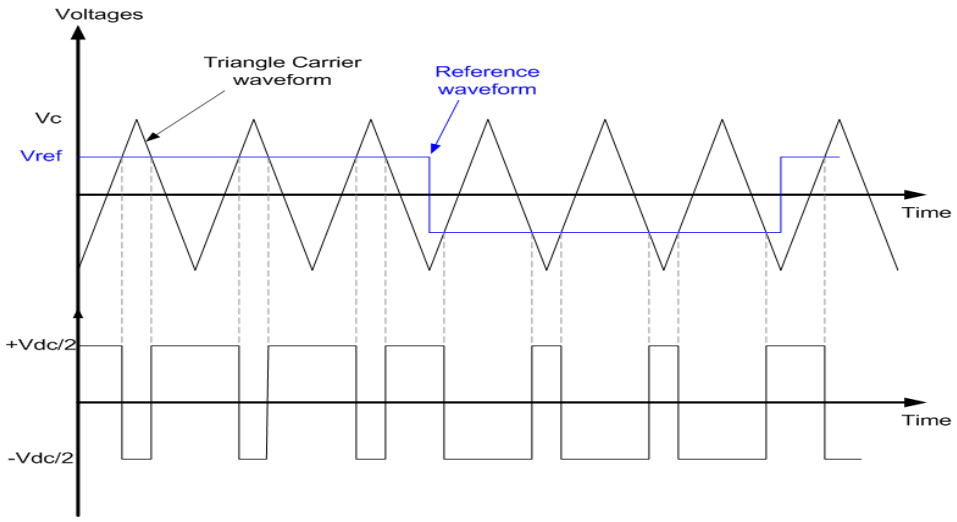
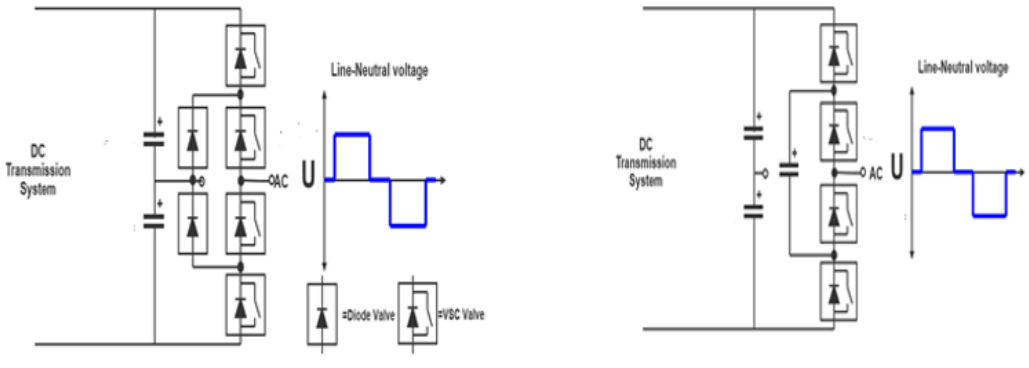


Fig. 2-31 Two level Voltage source converter[34].



(a) Diode Clamped *(b) Capacitor Clamped*

Fig. 2-32 Three level Voltage source converter [34]

2.5.3 The Modular Multi-Level Converter (MMC)

Recent trends in VSC technology led to the development of the Modular Multilevel Converter (*MMC*). MMC consists of a large number of identical but individually controllable sub-modules (*SMs*), which form its basic building block. They can be scalable to attain any desired voltage rating, avoiding the need for connecting semiconductor switches in series. Some of the key features of the MMC includes [35]–[43].

- Modular Design
- Low switching frequency resulting in reduced losses compared to 2 or 3 - level VSC converters.
- Scalability
- Flexibility in control of voltage level,
- Ability to control the submodule as a voltage source and with discrete number of voltage steps,
- Reduced harmonics.

The complete circuit arrangement of a three phase MMC scheme is shown in Figure 2.33. As shown, it comprises two *multi - valves* in each phase – namely the upper and lower multi-valves. The multi-valves are collectively referred to as *phase module* (or *Leg*). Each of the multi-valves have an equal number of *SMs;* and the *SM* capacitor is usually charged to a voltage, V_{CM}. The arm reactor is designed to limit the circulating current resulting from capacitor voltage imbalances and also limits the rate of rise of DC faults during DC side short circuits. The voltage across the capacitor at any time can be obtained by the use of Equation 2.1. Thus

$$V_{CM} = \frac{V_{DC}}{N_{SM}} \qquad \textbf{(2-1)}$$

V_{DC} is the voltage across the converter terminal and N_{SM} is the number of SMs in a multi-valve (or arm). V_{CM} is the instantaneous voltage of the capacitor. The pictorial view of the basic components of a SM is shown in Figure 2.34.

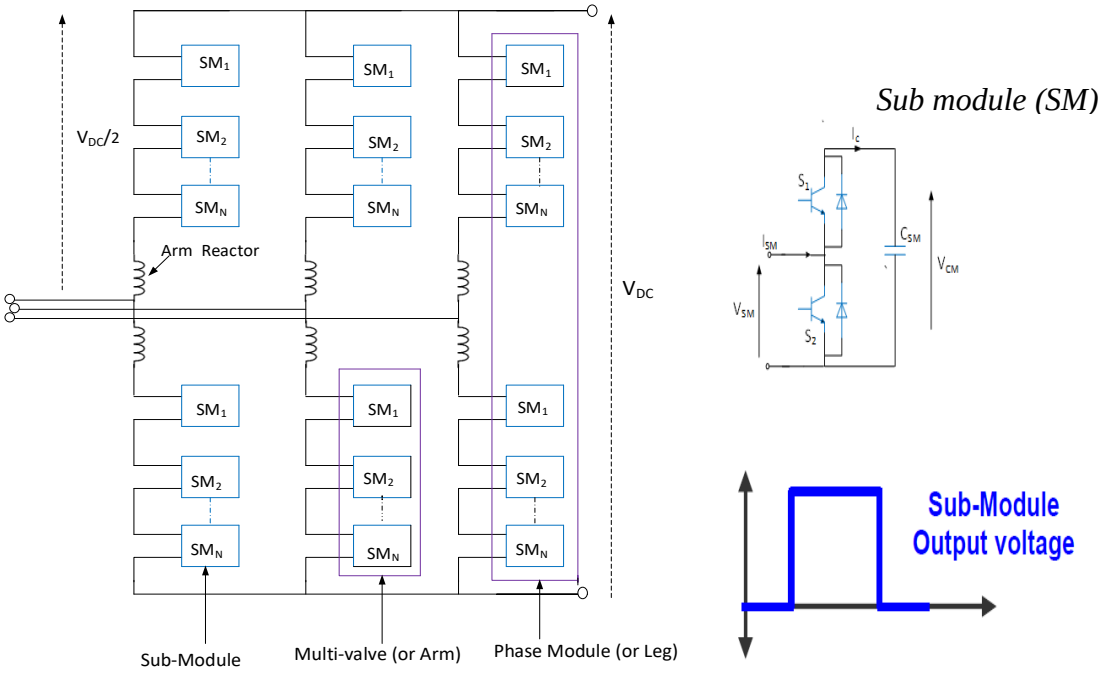
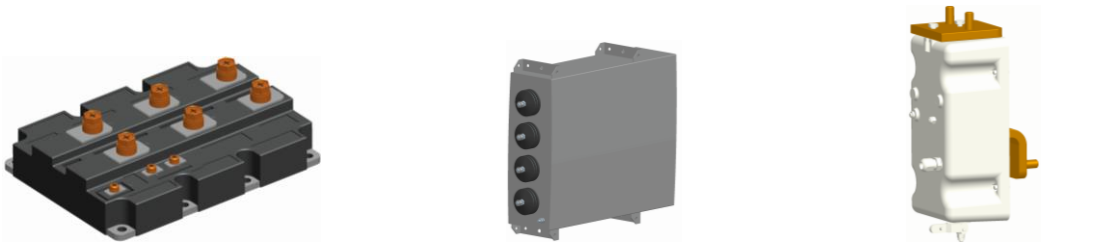


Fig. 2-33 *Topological structure of Modular Multi-Level Converter (MMC)*



(a) *IGBT* ***(b)*** *Capacitor* ***(c)****By-Pass Switch*

Fig. 2-34 *Pictorial view of the basic components of a sub-module (SM)*[30]

The net output voltage in an MMC is the sum of the individual output voltages from each *SM* in a multi-valve. Under steady state conditions, the total DC voltage in each converter leg equals the nominal DC link voltage; and only half of the *SMs* in each arm are connected to their respective capacitor (or inserted) during normal operating conditions. Another key and important feature of the MMC is the reduced *dv/dt* on the AC side, since the voltage steps are smaller compared to the conventional VSCs thus enabling the use of a transformer with a lower insulation requirement[40]

The circuit arrangement of a *SM* is shown in Figure 2.35. As shown, a *SM* consists of two IGBT switches S_1 and S_2 , and a capacitor C_{SM} . The function of the two switches, S_1 and S_2 is to either "*insert"* or "*by-pass"* the capacitor in the current path thus allowing the production of two voltage levels. When the capacitor is inserted in the path of current the voltage is V_{SM} and "*zero*" when it is "*by-passed*". The switching table is presented in Table 2.1 and three possible switching states can be realised. However, in practice other components may be added. Each sub-module is only capable of generating two voltage levels; zero voltage or positive module voltage, therefore under fault conditions the presence of the anti-parallel diodes in each IGBT implies that the converter cannot prevent, or "block", conduction between the AC terminals of the converter into a fault in the DC system.

The fault current path can only be blocked using DC circuit breakers at the converter terminals or by the disconnection of the AC supply and then isolating the fault using off-load isolators. This is explained in detail in section 3

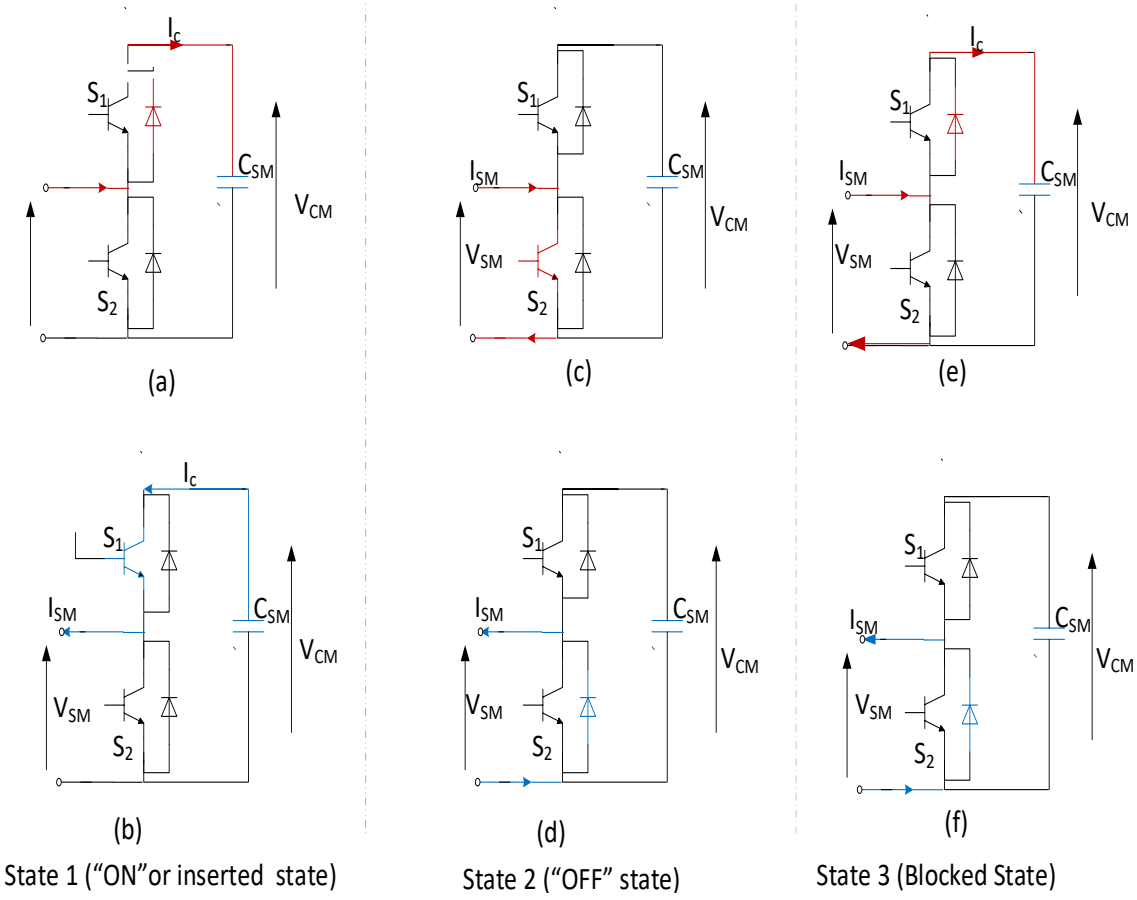


Fig. 2-35 *Switching states of a sub-module (SM)*

Table 2-1 *Switching table for a SM*

Mode	***S_1***	***S_2***	***State***
1	*ON*	*OFF*	*"ON" or Inserted ($V_{SM} = V_{CM}$)*
2	*OFF*	*ON*	*"OFF" ($V_{SM} = 0$)*
3	*OFF*	*OFF*	*"Blocked"*

The ON* or *inserted state. During this state, S_1 is "*ON*" and S_2 is "*OFF*"; the current will be conducted through the *SM* capacitor. The capacitor will get charged if I_{SM} is positive and discharges when it is negative. Generally, the current can either flow through the diode of S_1 and thereby charge the capacitor (Figure 2.35(*a*)) or through the IGBT of

S_1 to discharge the capacitor (Figure 2.35b). The output voltage, V_{SM} of *SM* therefore equals the capacitor voltage, V_{CM}

***The OFF or by-passed State*:** S_1 is "*OFF*" and S_2 is "*ON*" and the *SM* capacitor will be by – passed and behaves like a short circuit. (Figure 2.35 (c & d)). As a result, V_{SM} will be zero and the capacitor voltage, V_{CM} will remain constant

The Blocked State: S_1 and S_2 are "*OFF"* and the freewheel diode provides a path for the current. During this state, the direction of flow of current determines whether the capacitor will be charged. (Figure 2.35 e&f) Ideally, it is not allowed to be discharged. Generally, at the instant of operating the converter and during fault condition all submodules are in this state.

Based on this switching sequence, each of the individual *SMs* in an *MMC* can be individually and selectively controlled hence making the converter leg to operate like a controllable voltage source[41]. Generally, in a *SM*, only one of the switches is switched on at any given instant. The number of voltage levels that can be realised by an *MMC* is equal to the number of *SMs* in a single *arm* plus one[42]. The *SM* can also be of a full bridge type (Figure 2.36). An advantage is its fault limiting capability, thus making it able to ride through DC side faults but not without generating losses (which is likely to double that in the half bridge *SM*) as well incurring cost. Unlike the *half bridge* arrangement, the full bridge arrangement can produce both positive and negative voltages. It is this ability that gives the fault tolerance and limiting capabilities[6]. Unlike the half bridge submodule, the full bridge sub-module can produce three different voltages at its terminals; zero voltage, positive sub-module voltage and negative sub-module voltage. The availability of the sub-module to generate a negative voltage gives the full bridge converter the ability to "block" the AC terminal voltage thus driving a fault current into

a short circuit in the DC system and therefore stop the fault current. The full bridge converter can therefore be said to fulfil the role of both converter and DC breaker.

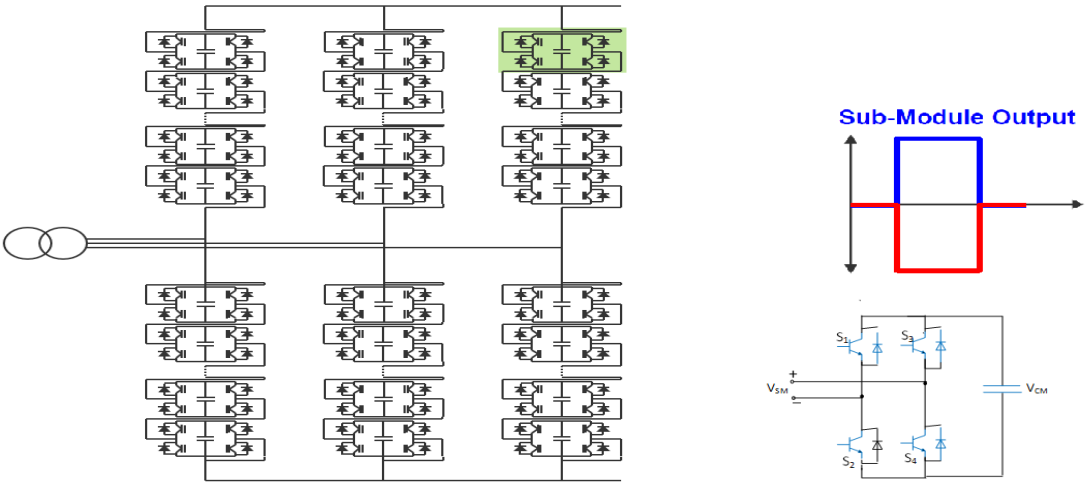


Fig. 2-36 *Full-bridge sub-module (SM)*[6], [30]

For simplicity, further details on the switching arrangements as well as the resulting waveforms are not shown but can be found in literature [2], [37]. A typical practical MMC HVDC system based on half bridge Submodules is shown in Figure 2.37. This is a demonstration project and was developed by General Electric. The pictorial view of the completed project is shown in Figure 2.38.

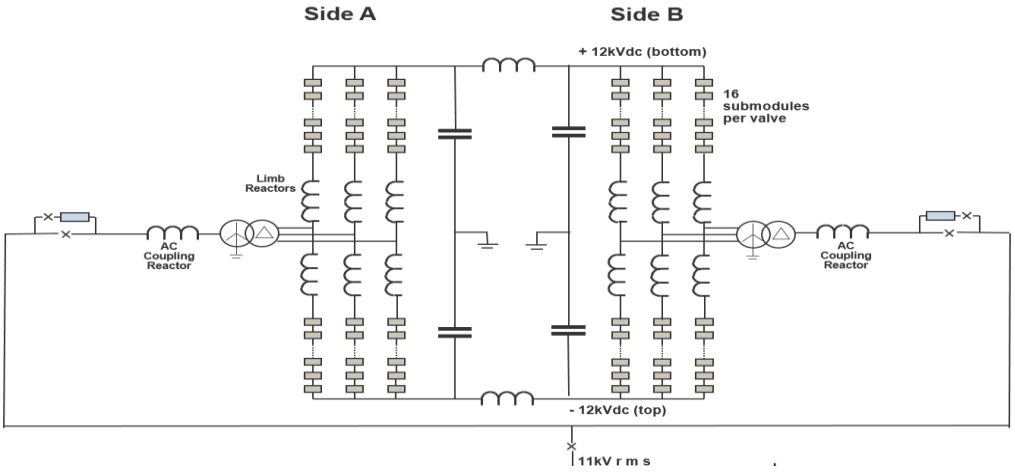


Fig. 2-37 *Practical MMC-HVDC based on half bridge Sub-module* [30].

(a) A Sub-module

(b) Valve module (8 Sub-module

Fig. 2-38 *Full-bridge sub-module (SM)* [30].

2.6 Short circuits in HVDC systems

Generally, like the conventional HVAC system, HVDC systems are prone to faults. The types of fault that could occur on a DC grid can be grouped into any of the following.

- *DC side Faults*: this includes the DC link short circuit such pole to ground faults, pole to pole faults or pole to pole to ground fault.
- *AC Side faults*: faults or disturbances on the DC side or switching transients
- Converter Internal Faults or submodule internal faults, diode or capacitor faults
- Lightning disturbances.

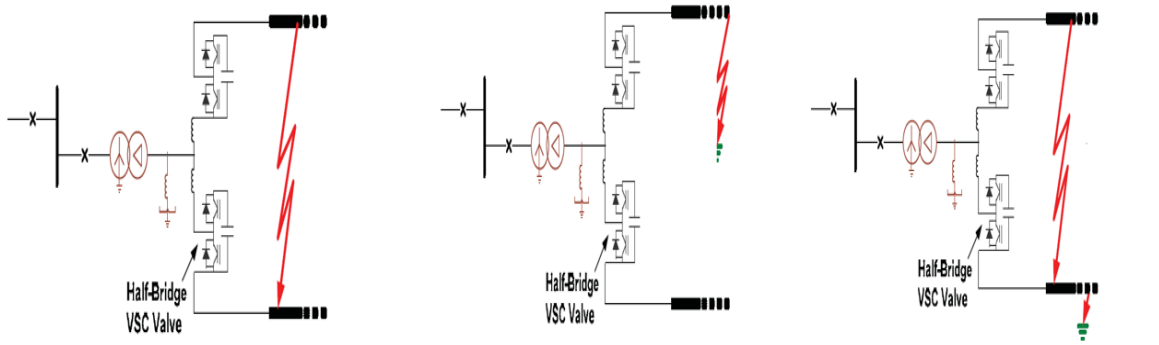
Table 2.2 summaries some common faults in MMC based HVDC systems as well as their primary causes. However, this research focuses of DC side faults.

2.6.1 Pole-to-Pole versus Pole-to-Ground faults

As shown in Figure 2.39, a pole-pole (*P-P*) fault is that which occurs when there is a direct contact or insulation breakdown between the positive pole and the negative pole of a transmission system, whereas a pole-ground (*P-G*) fault is said to occur when there is an insulation breakdown and there is direct contact between either the positive pole and ground; or between the negative pole and ground.

Table 2-2 *Common Faults in MMC-HVDC System* [43]

Level	***Faults Types***		***Level***		***Fault Types***
Submodule Level (SM)	IGBT	Open Circuit	System Level	AC Side Fault	AC grid voltage unbalance
		Intermittent gate misfiring			Negative Electrode Short Circuit
	Diode	Open Diode			Positive Electrode Short circuit
		Short Circuit			Monopole to Ground
	Capacitor	Fault in Capacitor Structure			Lightning and switching disturbances
					Open Circuit
Converter Level		Capacitor Voltage unbalance		DC side Fault	Positive Electrode Short circuit
		Circulating current among three Phase Unit			Negative Electrode Short Circuit
		Unbalance between upper and lower arm voltage			Monopole to Ground
		Control of energy stored in the leg			Open Circuit
		Single Phase to ground		Whole System Fault	Modulation Control Scheme
		Double Phase to ground			Various disturbances
		Three-Phase to Ground			Unequal energy from AC to DC side



(a) Pole-to-Pole fault *(a) Pole-to-ground fault* *(a) Double Pole-to-ground fault*

Fig. 2-39 *Pole-to-pole and pole-to-ground faults* [4]

Generally, a transmission system can either be a cable or an overhead line. The choice between the two is determined by environmental constraints, cost and reliability of the transmission system, whereas the environmental impact on cable is much smaller compared to overhead lines. The DC side P-P is the most serious fault but not common. The DC cable ground fault is the most common but less destructive. Cable faults are usually caused by external mechanical stress, insulation failure, excessive voltage/current or aging. As a result, the faults are usually permanent and will require a complete shutdown of the line and costly repair. The faults in overhead lines are usually caused by lightning strikes, object falling across the positive and negative line, etc, and may either be temporary or permanent. As shown, DC short circuit can also be a double P-G. However, the effect of a double P-G is the same as a P-P fault[19]. The characteristic differences in the footprints between a *P-G* and *P-P* fault is explained in detail in Chapter 4.

2.7 Technical and economic challenges in developing DC grids

As previously stated, the future HVDC network will be interconnected to form a DC grid since it has been proven to be the most viable option for utilising the potential of offshore wind power. However, some technological gaps need to be addressed before MT-HVDC

system can be realised. These include non-availability of commercially, DC line fault detection algorithms, DC – DC converters and power flow control issues. Details are explained hereunder.

2.7.1 Lack of commercially available HVDC breakers

As indicated in Chapter 1, the major issue with the gap in development of the DC grid is the rapid propagation of fault currents into the grid. Existing techniques for two-terminal HVDC system utilising AC side breakers (Figure 2.40) are not applicable to DC grids as this will de-energise the entire grid and other sub-grids connected to the network. Therefore, DC breakers located at the line / cable ends are required to isolate the faulty section. (Figure 2.41).

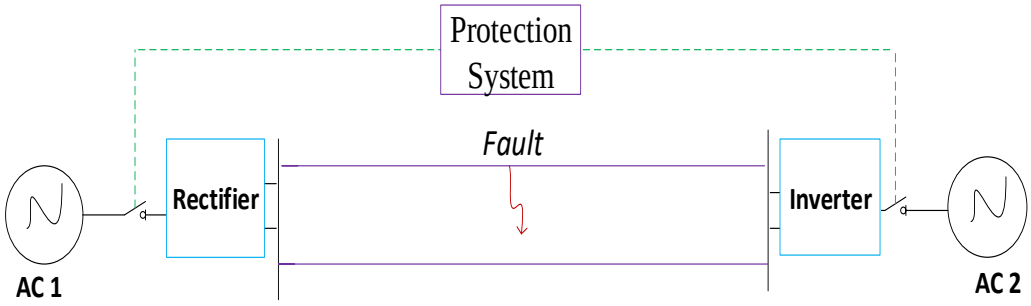


Fig. 2-40 *Existing protection technique for two-terminal HVDC systems*

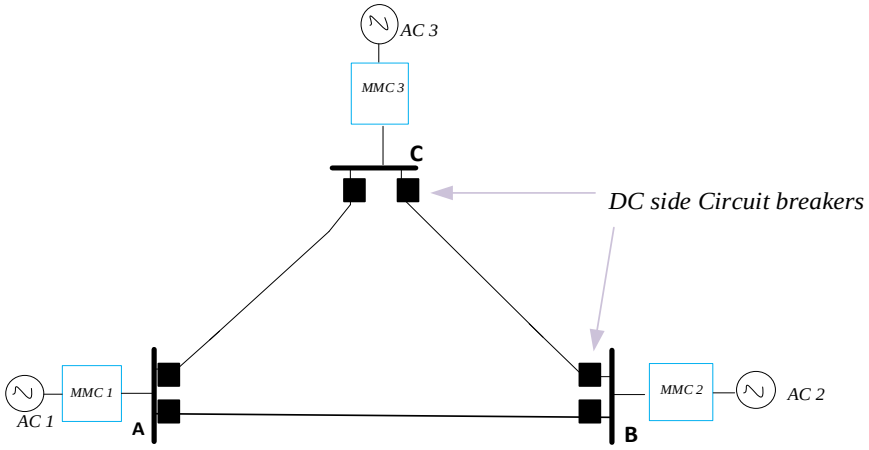


Fig. 2-41 *Three terminal DC grid showing HVDC breakers*

To date, no commercially available HVDC breaker exists. Attempts made to develop mechanical HVDC breaker [8], yielded limited results due to technical issues involved in generating a zero crossing of the current as well as methods of dissipating the huge amount of energy involved. In the same way, proposed solid state HVDC circuit breakers suffer some setbacks due to its high-power losses resulting from the on-state resistance and forward voltage drop[44], [45]. This adds to the cost of operating the converters. However, it is anticipated that a hybrid HVDC breaker which combines electromechanical parts with power electronic switches will be commercially available in the near future since prototype HVDC breakers have been proposed in literature[9], [10]. A typical example is that developed by General Electric as shown in Figure 2.42, details of the operational principles can be found in[46].

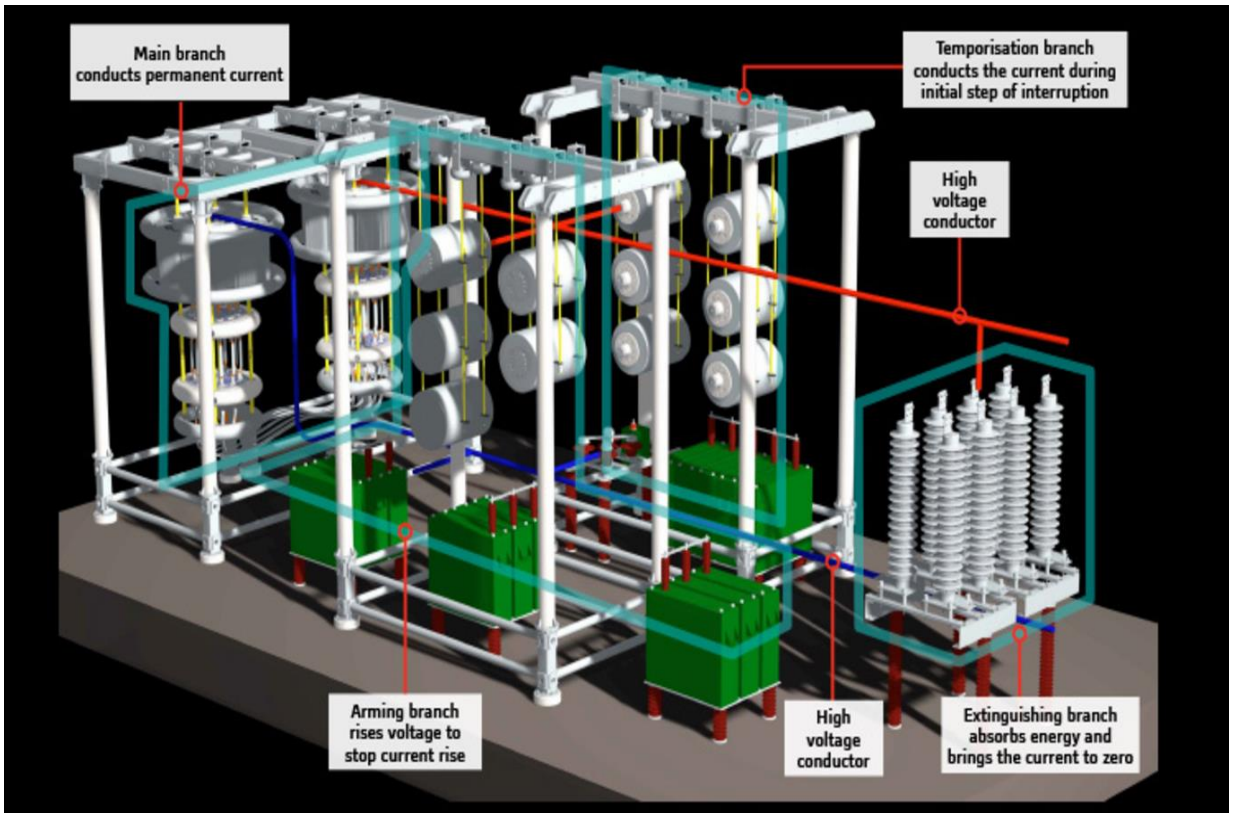


Fig. 2-42 *A Prototype hybrid HVDC breaker*[46]

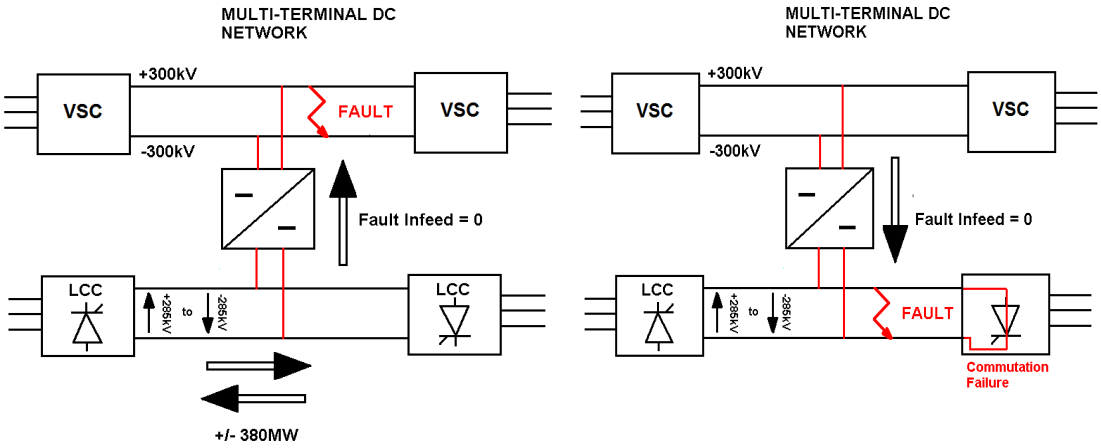
2.7.2 DC fault detection algorithms:

As indicated in section 1.1, the protection algorithms developed for conventional *HVAC* system are not suitable for the protection of DC grids due to the characteristic differences in their fault current footprints. This is because DC fault current rises rapidly (resulting from the low inductance in DC systems compared to AC systems). Considering the vulnerability and the associated cost of the power electronic devices, the fault must be detected and cleared very quickly. Therefore, the protection algorithm for DC grid must detect the fault while the fault current is still rising, well before it reaches steady state.

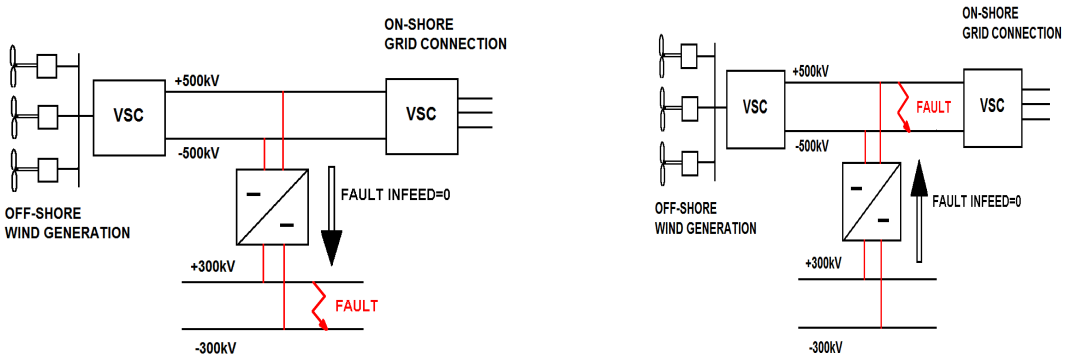
Generally, the protection trip decision window should be shorter than those used in HVAC systems. Generally, the fault detection time, including the time delays in the hardware is targeted at *1ms* [7]**.** Therefore, if the protection system must meet these requirements, existing protection algorithms for HVAC systems will have to be re-developed for DC grids. Several attempts have been made in this regard but more work still needs to be done, further details are presented in section 3.1

2.7.3 DC/DC converters

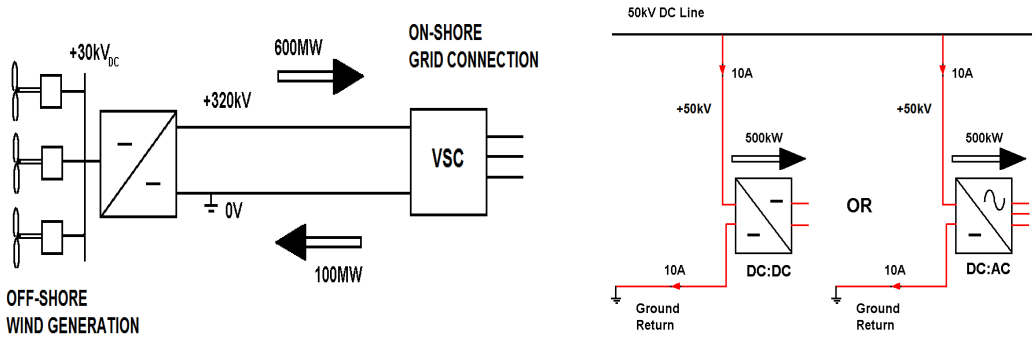
Generally, the development of HVDC grids will depend on the gradual expansion of existing point-to-point HVDC links. Therefore DC/DC converters are needed to transform the voltages from one level to another. Also, DC/DC converters may also find useful applications during power flow control to prevent overload in specific network sections if MTDC grids are expanded to meshed configurations. In general, DC-DC converters are needed for interconnecting two transmission systems of different voltage ratings and have the capability of *fault blocking*, power transfer, distribution taps as well as low voltage taps (Figure 2.43)[47].



(a) LCC to VSC network inter-tie



(b) Distribution taps



(c) Offshore wind farm collector *(d) Low voltage DC taps*

Fig. 2-43 *Applications of DC-DC converters for future DC grids*[47]

2.7.4 Power flow control devices

Generally, during normal steady state operating conditions in any transmission network, some paths may be lightly loaded and some overloaded. To avoid this problem, power flow control devices are required. Furthermore, the power flow control measures can also be used to prevent the overloading of a transmission line/cable during post-fault conditions, by transferring the excess current through an alternative DC transmission line. Power flow control devices have been widely used in AC systems, but techniques and devices employed to control the power flow in AC grids are not directly applicable to DC grids due to the characteristic differences between AC systems and DC systems

In AC networks, the dominant impedance is the transmission line inductance; therefore, by inserting capacitor banks or inductors, the line reactance can be varied and, thus regulating or controlling the power flow around the grid. However, in DC networks, the flow of current is largely dependent on the DC resistance of the conductors and the transmission path inductance plays no part in the steady-state power flow. Attempts have been proposed for power flow control in a DC meshed grid, each having their own advantages and disadvantages such as DC transformers, variable series resistors (VSR), and series voltage sources (SVS).

2.8 Summary

The analysis carried out revealed that HVDC is the most economical method for integrating an offshore wind farm. Furthermore, to harness the full potential of these offshore wind farm farms, existing HVDC networks will be expanded and interconnected to form a DC grid. Key advantages of MT-HVDC systems include flexibility, reliability, optimal equipment utilisation and cost reduction. It will also pave the way for energy trading among regional countries. However, the successful development would require

that some technological gaps be addressed among which include the development of fast fault detection algorithms as well as fast operating HVDC breakers. This is largely due to the characteristic differences in the fault current footprints between HVAC and HVDC interconnections. Consequently in a HVDC grid, a fault in one part of the network would propagate very rapidly and could result in a total shut down of the entire network. Therefore the need for a fast fault detection and isolation strategy or strategies is pre-eminent.

Studies carried out on HVDC converter technologies show that although the LCC is robust and inherent to DC side faults, it is not suitable for DC grid application since reversing the flow of power in LCC based HVDC will reverse the voltage polarity. However, VSC has flexibility in control and can change the direction of power flow without a change in the bus voltage polarity. Types of VSCs include two-level, multi-level and MMC; with each having their advantages and disadvantages. The analysis carried out also shows that the MMC –VSC is the most suitable converter topology due to its inherent capability such as flexibility in voltage control and scalability. *MMC* converter can either be HB or FB submodules. The HB MMCs are referred to as *non-blocking* converters since they are not able to block DC side faults whilst the FB *MMC* are referred to as *blocking converters* since they have the capability to block DC side current. However, in terms of switching losses and cost, the HB - SM configurations have relative advantages over the FB - SM. However, whether or not a converter would be a HB -SM or FB - SM is a matter of compromise.

Generally, in anticipation that HVDC breaker will be commercially available soon, a major issue still remains, the development of suitable DC line protection algorithms for application to DC grids. However, in order to address this, existing protection philosophies developed for HVAC systems, those used in DC traction systems, as well as those applicable to two terminal HVDC systems including proposed techniques for DC

grids were studied. The types of fault scenarios in HVDC grids as well as the general protection requirements for the development of HVDC protection algorithms were also studied. The findings are presented and discussed in details in Chapter three

Chapter 3

3 Review of Protection of DC and AC Systems

3.1 Introduction

In this chapter, the protection issues that need to be considered in the development of HVDC grids are presented. The existing protection methods and principles for low voltage DC systems such as DC traction systems, HVAC systems and conventional two-terminal HVDC systems are evaluated. Finally, the proposed protection methods and strategies applicable to DC grids are critically reviewed.

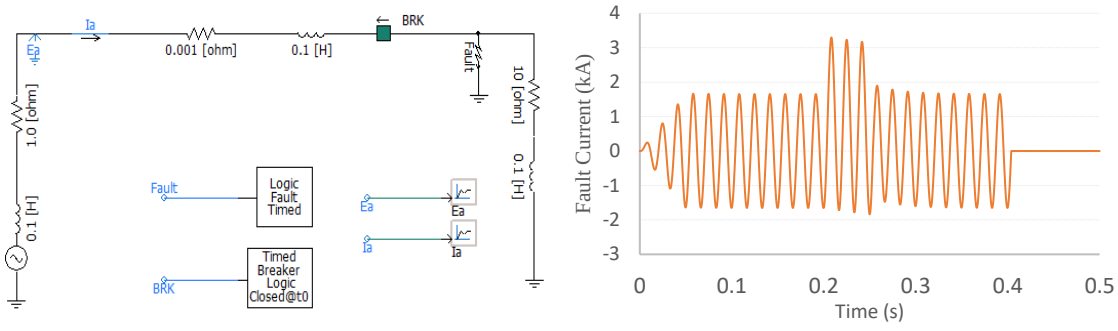
3.2 The nature of fault in DC Systems

As indicated in Chapter 1, the absence of zero crossings in DC systems as well as the low inductance compared to AC systems is a major issue with the development of the DC grid. In AC networks, the current is periodically driven through zero and current zero is the ideal instant to interrupt the fault current. In AC systems, the fault clearance time is normally 60 – 80ms, with 40ms for circuit breaker. However to interrupt fault in DC system, the circuit breaker must perform many times faster than in AC systems, typically 8 times faster than in AC systems. This implies that fault current interruption in DC networks must be done very precisely and much more rapidly.

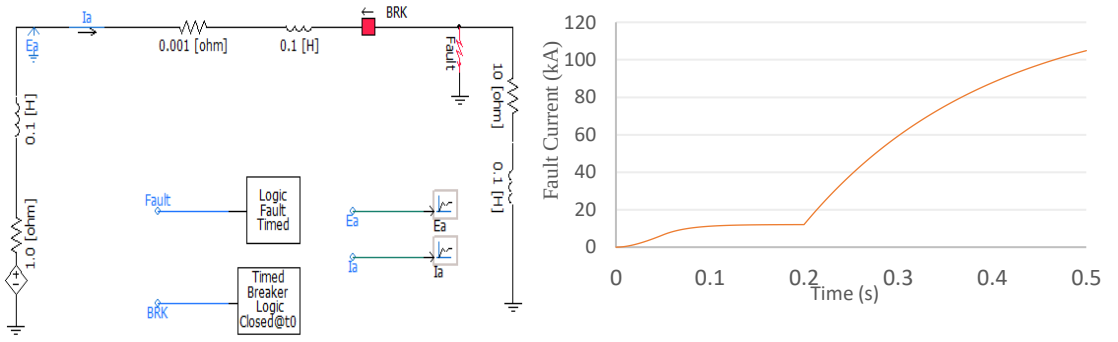
3.2.1 Fault current interruption in DC Systems

Generally, with AC systems there is the natural passage of current through zero at each half cycle. This corresponds to the extinguishing of the arc during the circuit opening. However, with DC there is not such natural zero (Figure 3.1 and Table 3.1) and therefore, to guarantee arc extinction, the current must decrease to null, thereby forcing the current passage through zero [48].

As shown in Figure 3.1a, following the occurrence of the fault at 0.2sec, the magnitude of the current increases and then decreases with time until the fault is cleared by the use of an AC breaker after a further 0.2sec. However, in the case of DC system as shown in Figure 3.1b, the fault current rises exponentially and continue to rise without decay.



(a) AC fault



(a) DC fault

***Fig. 3-1** AC Versus DC Short Circuit Current*

Generally, DC fault current interruption technique has been employed in developing low and medium voltage DC circuit breakers such as those used in DC traction system (Figure 3.2). However, a means of dissipating the huge amount of energy involved remains a major concern in adapting this principle for HVDC breakers. This is largely due to the large fault current in HVDC systems resulting from their large power ratings. However, as previously mentioned, with the recent advancements made in the development of HVDC breakers, this research focuses on DC line fault detection algorithms for application to DC grids.

Table 3-1 AC Versus DC Short Circuit Current [49]

AC Fault	*DC Fault*
Natural zero	No natural zero
Magnitude decay over time	Magnitude quickly raises over time
Typically, higher reactance	Typically, lower reactance

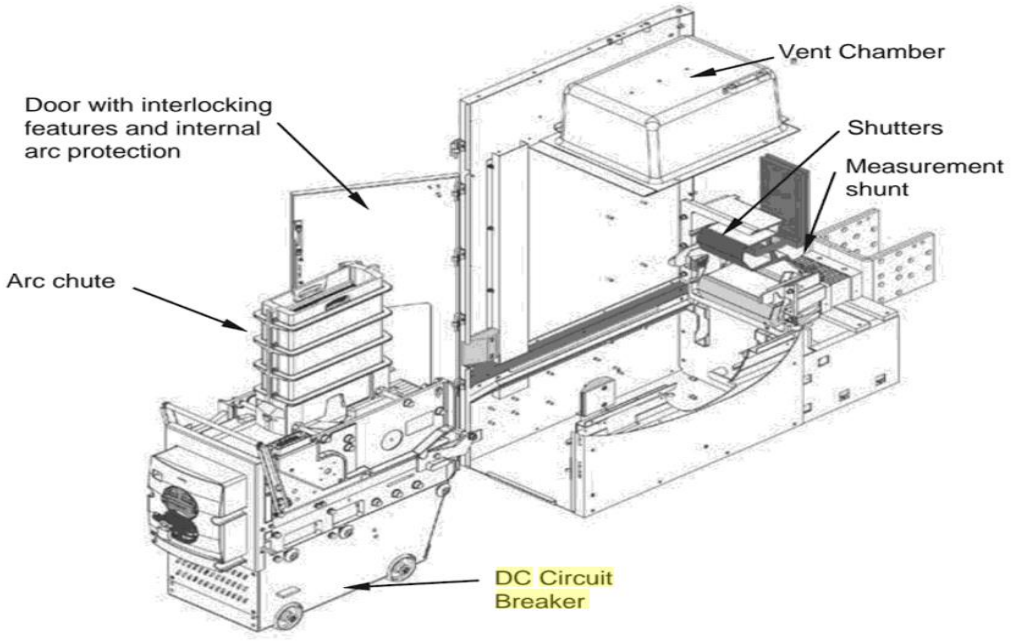
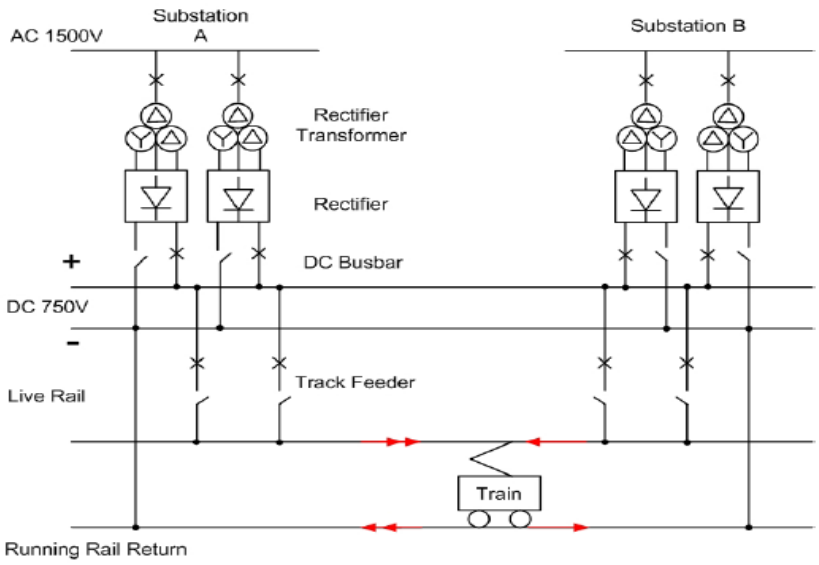
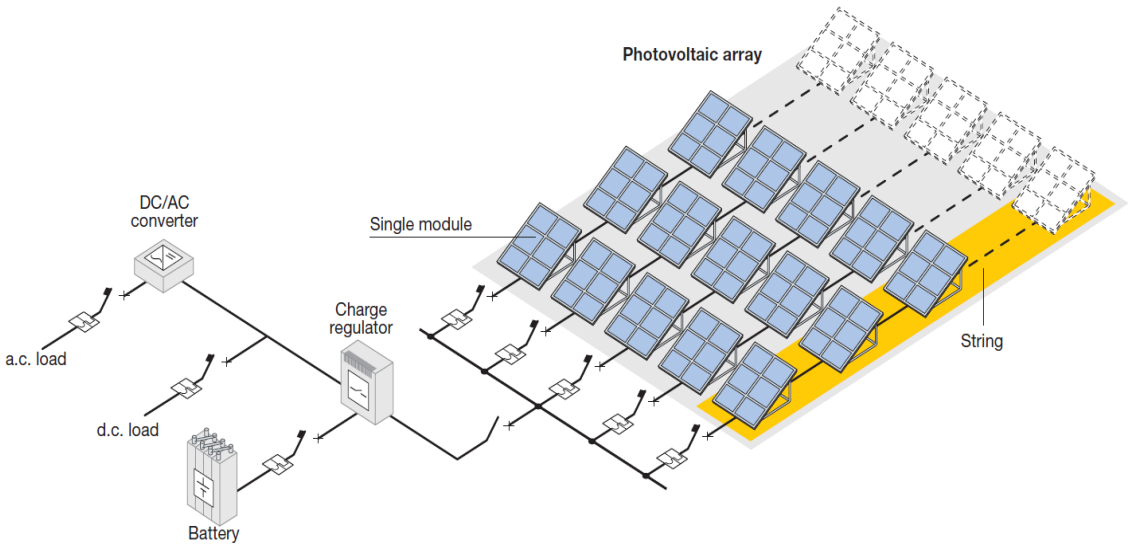


Fig. 3-2 *Withdrawable DC circuit breaker for DC traction application*[50].



(a) *DC traction systems*[51]



(b) *Stand-alone photo-voltaic plant* [48]

Fig. 3-3 *Applications of DC circuit breaker*

The applications of circuit-breakers in DC circuits for electric traction in general can be summarized as follows [48]

- Protection and operation of both overhead and rail contact lines (Figure 3.3)

- Protection of air compressors on board underground and train cars
- Protection of distribution plants for services and signalling systems
- Protection of D.C supply sources, such as renewable sources (Figure 3.3)
- Protection and operation of D.C motors.

As stated earlier, due to the large current resulting from the voltage they handle (typically 750V for DC traction and 200kV for HVDC systems) and subsequently huge amount of energy dissipation in HVDC systems, the requirements and concept of HVDC breaker is different from that of low voltage DC breaker.

3.3 Protection algorithms for low voltage DC systems

In general, DC circuit breakers will rely on trip signals from relays in order to operate. These relays rely on measured electrical quantities (voltages and currents) on the system that indicates whether a fault has occurred. Some existing protection algorithms used for DC traction applications include:

3.3.1 Direct – acting (or instantaneous) overcurrent protection

This provides protection against overloads as well as high speed operation during high current faults. However, the major draw-back of this technique is that it cannot discriminate between normal load conditions and low level or remote faults. For example, the train starting current can be significantly larger than the fault current resulting from a long distance remote fault. (Figure 3.4). This can result in faulty relay discrimination, hence leading to spurious trips. However, this situation is rare in practice, but measures must be taken should they occur,

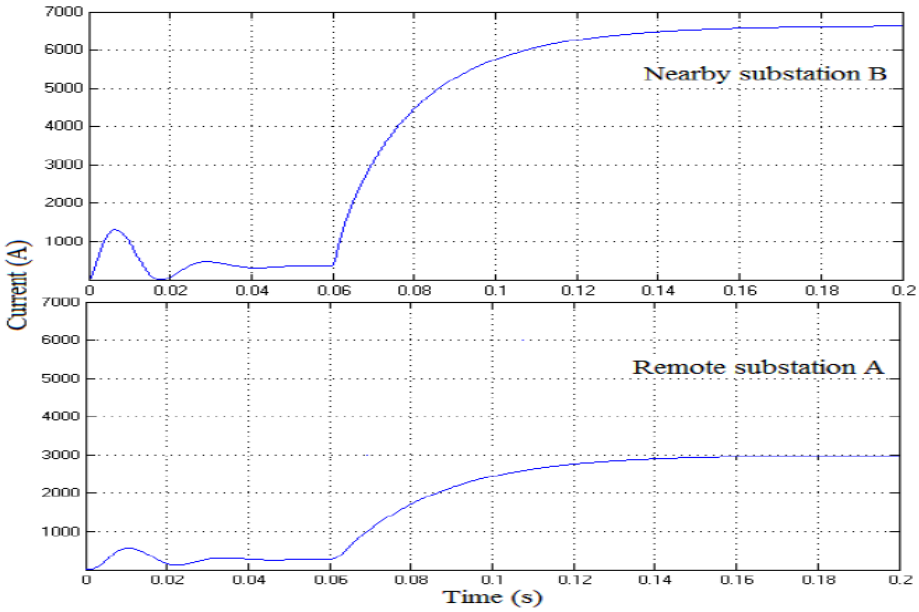
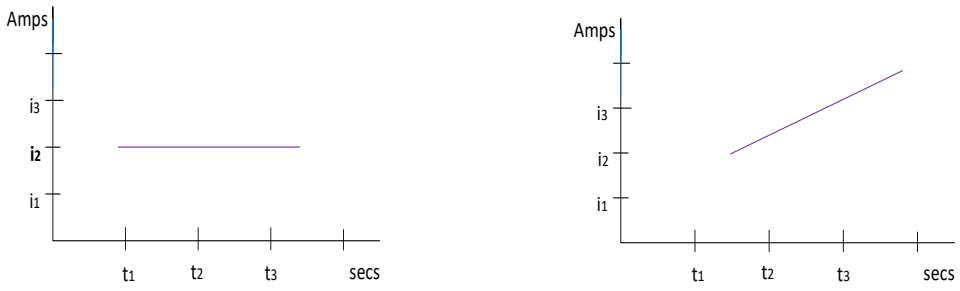


Fig. 3-4 *Close-up versus remote fault*[51]

3.3.2 Rate of rise (*di/dt*) protection

This technique is widely used in DC traction system as it measures the initial increase in the current thus detecting the presence of fault before reaching damaging levels. A DC line fault is detected by comparing the incremental DC current (Δi) at the relay terminal with a predetermined threshold for a pre-set time duration, (Δv)



(a)Pre-fault condition *(b) Post-Fault Condition*

Fig. 3-5 di/dt *Protection Technique by Sampling*

$$\frac{di}{dt} \approx \frac{\Delta i}{\Delta t}$$

As shown in Figure 3.5, prior to a DC line fault, the current, i is in steady state so that the di/dt is ideally zero. During DC short circuit, the calculated di/dt is greater than a *setting* (or threshold) which is usually determined after considering all operating conditions including overloads. The *di/dt* based protection technique is extensively evaluated in Chapter 5.

3.3.3 Impedance protection

Generally, the impedance of a track section as seen from the relay location is the ratio of the track voltage to the current flowing in the relay. The presence of a fault along the track will result in a decrease in the line impedance. If the calculated impedance is less than the setting impedance, a trip signal is initiated. This technique is extensively used by the Network Rail in the UK[50]

3.3.4 Under voltage protection

This technique monitors a reduced track voltage during fault or during normal load conditions at the substations and along the track. A time delay element is also incorporated to provide discrimination between fault and normal load conditions, thus rendering it inadequate for close – up faults. Furthermore, it cannot provide directional discrimination.

3.3.5 Multi-function protection

Generally, modern low voltage DC relays normally incorporates two or more principles for fault identification and detection , for example the DC relay shown in Figure 3.5 [52]

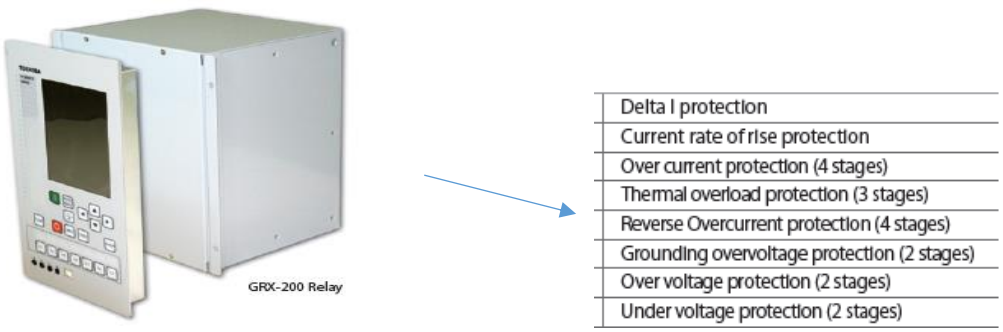


Fig. 3-6 *Practical di/dt relay* [52]

Generally, whether the protection algorithms developed for DC traction systems would be suitable for the protection of DC grids depend on grid configurations and the minimum time required to clear the fault. This includes the nature of the transmission medium (whether a transmission line or a cable), the length of the transmission medium as well as the converter topologies. Furthermore, for DC grids, the effect of cable capacitances as well as the long length of the transmission systems impact on the resulting fault current profile. The frequency dependency of the distributed line parameters as well as travelling wave effects is another major issue. Also, the time required to clear the fault in DC grids (ideally *1ms* including the time delays in the hardware) would also impose limitations in adopting the protection techniques. However, the *di/dt* protection technique was further investigated to ascertain its suitability for DC grid protection. The findings are presented in Chapter 5. In the same way, the protection algorithms developed for HVAC system is also investigated and details of the findings are presented hereunder.

3.4 Protection algorithms for HVAC systems

The protection techniques for HVAC system available in literature fall under one or a combination of two or more of the following.

- Impedance based or Distance Protection Technique
- Differential protection
- Overcurrent Protection
- Boundary Protection
- Travelling wave based protection techniques

3.4.1 Impedance-based or distance protection technique

Impedance or distance based protection techniques have been widely used in AC systems. The basic principle is that the impedance seen by a relay reduces suddenly during faults. The impedance measured during a fault is referred to as *apparent impedance* Z_p. The idea is to estimate the impedance between the fault point and the relay by measuring the loop voltage and the current formed following the occurrence of a fault. Since impedance is proportional to the line length, the distance to the fault, l_f can be estimated. As shown in Figure 3.7, the voltage measured at the relaying point is divided by the measured current to get the apparent impedance, Z_p which is the calculated impedance at any instant in time following fault inception. This value is compared with a value referred to as *reach point* impedance, Z_r to determine whether a fault has occurred along the line (Terminal AB as shown)[53], [54].

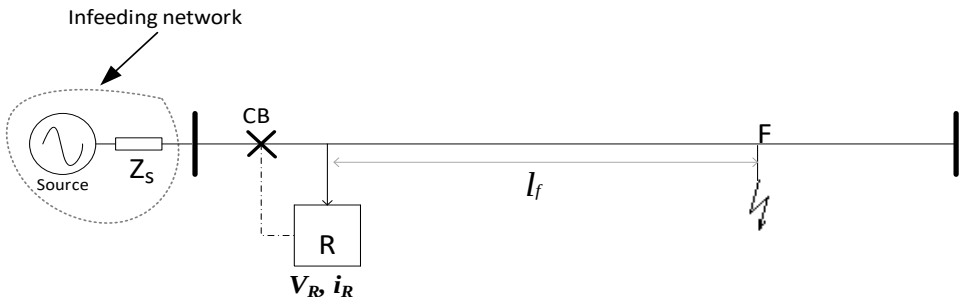


Fig. 3-7 *Basic principle of distance protection* [53]

If Z_p is less than Z_r a fault is detected and the circuit breaker will receive a trip signal to operate. Thus,

When $Z_p < Z_r$

Z_p = Fault impedance.

Z_r = Reach or setting point impedance

Z_r is selected after considering all system conditions such as switching and overload condition to avoid nuisance trips. A very good advantage of this technique is that it only operates for faults occurring between the relaying point and the selected reach point, thus making it to be inherently directional. In this way, it can distinguish between internal and external faults. Also, it does not rely on information from remote end terminal and as such no communication channel is required - hence making it very fast in operation. The only information required are the voltage and current signals measured at the local terminal.

Considering Figure 3.8, the arbitrary faults F_{i1}, F_{i2} and F_{i3} are internal faults and hence falls within the protection zone of the relay, *R*. However, with respect to relay R, F_{e1}, F_{e2} are external faults. As per distance protection, the corresponding fault distances are l_{f1}, l_{f2} and l_{f3} respectively.

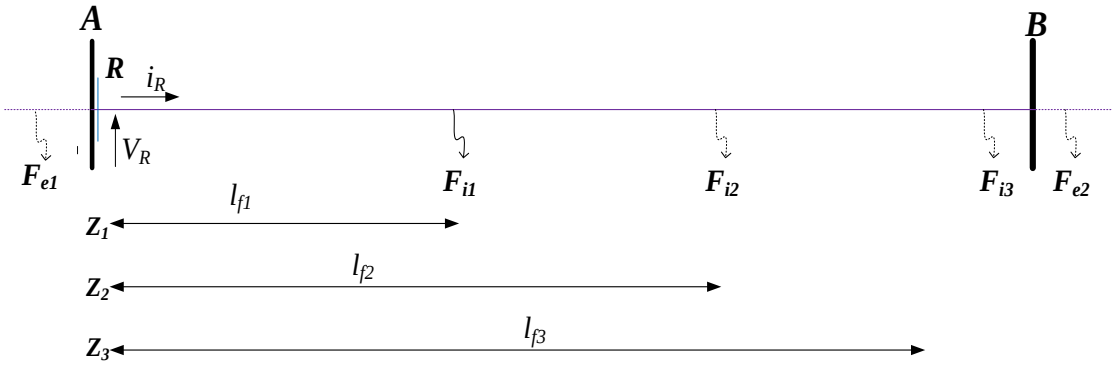


Fig. 3-8 *Basic principle of distance protection*

As the impedance is a complex number, directional protection technique utilising the reactive component is usually used to provide discrimination for reverse faults (F_{e1} as shown) while the concept of zoning is used to provide discrimination for forward external faults (F_{e2} as shown).

Due to inaccuracies in the measurements resulting from CT errors, measurement errors, inaccuracies of the line impedance, a protection reach setting of 100% of the line length is not practically possible with distance protection. To avoid nuisance tripping of the

distance relay, the protection line is divided into different *zones of protection* and with each zone having its own settings (Figure 3.9).

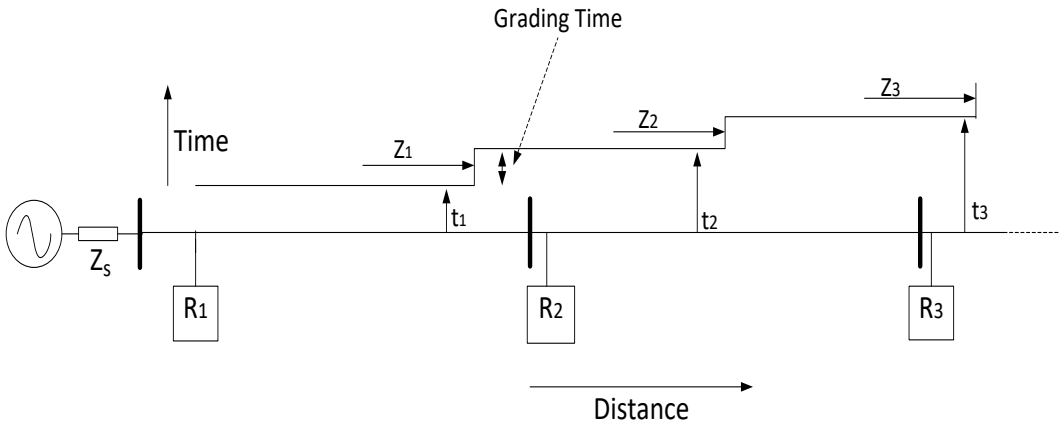


Fig. 3-9 *Basic principle of distance protection* [53].

For example, zone 1 has a *reach* setting of up to 80% - 85% of the protected line resulting in a security margin typically 15 – 20% from the remote end of the line[53][54] is selected as zone 1 or *under-reaching* stage. In this way, there is no risk of zone 1 protection overreaching the protected line. The remainder of the line (15% – 20%) and up to a minimum of 120% of the line is covered by zone 2 (over-reaching stage). However, in many applications zone reaches are set to cover the entire protected line section +50% of the shortest adjacent line [54] In order to ensure selectivity and mal-operation, zone 2 is time – delayed or graded (typically 0.4 - 0.5s for electromechanical relays and 0.25 - 0.3s for analogue static or numerical relays) relative to the protection of the adjacent line [53] In most applications, a third zone may be provided to protect the entire length of the neighbouring lines. Zone 3 covers the first and second line and up to 20 - 25% of neighbouring (third) line. Zone 3 setting can also provide back-up protection for the second line. This is achieved by reversing its setting to cover up to 20% of the second line.

Generally, different types of impedance relays exist such as plane impedance relays, mho relays, with the latter having the advantages of providing directional discrimination. In all, the aim is to either provide directional discrimination or to provide discrimination against high resistance or arcing faults.

The advantages of the distance protection include the following [53][54]**.**

- It is comparatively simple to apply.
- It is fast in operation for faults located along the protected circuit.
- It can provide both primary and remote back up protection in a single scheme
- When applied with signalling channel, it can easily be adapted to create a unit protection scheme.
- Insensitive to source impedance variations

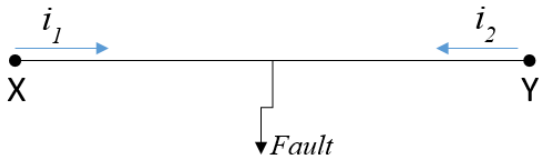
Recent studies have also proposed a distance protection technique for application to Teed-lines[55]. However, the reliance on communication will impose some limitations in adapting this technique for DC grid application.

Generally, conventional distance protection techniques applicable to AC systems are based on power frequency components; which make it suffer some setback in application for HVDC systems, for DC grid protection considering the time constraints. Furthermore, the absence of a nominal frequency implies that much work is needed to develop such techniques for DC systems, since it will need to be transient based. For this reason, those parameters that changes in the transient state would form the basis in adapting the distance based protection philosophy for application to the DC grid. In this research, the inductance based technique was investigated in the first instance based on lumped parameter modelling, the findings are presented in Chapter 5. Studies regarding the application of distance protection for HVDC system have been carried out in the recent

past and details can be found in[56]. However, none have been reported for DC grid protection.

3.4.2 Differential Protection

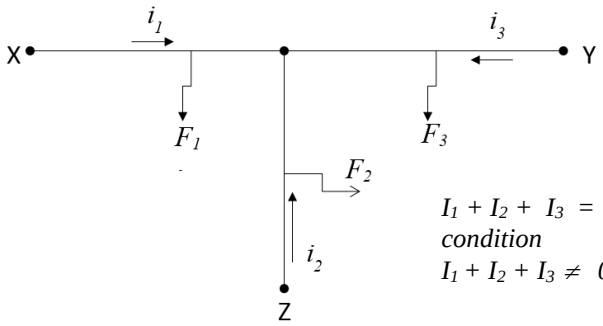
Differential protection is based on Kirchhoff's current laws, and hence during normal operating conditions, all current into a network node shall add up to zero. For example, as shown in Figure 3.10, a fault can therefore be detected by comparing the magnitude and phase of the two currents.



$I_1 + I_2 = 0$ *for normal condition*
$I_1 + I_2 \neq 0$ *for fault conditions*

Fig. 3-10 *Differential protection for two terminal networks*

Differential protection schemes can also be applied to Multi-terminal (or Teed) network as shown in Figure 3.11. The major challenge with the differential protection scheme is the requirement of communication channel between the respective terminals which renders it unsuitable for the primary protection for DC grid.



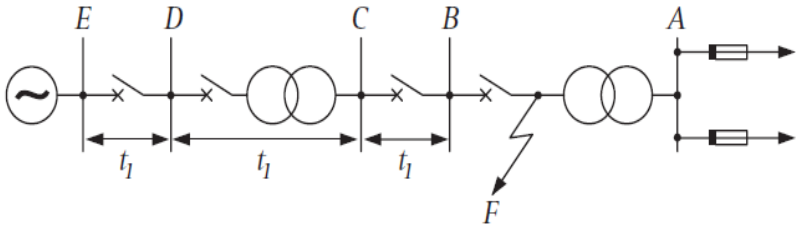
$I_1 + I_2 + I_3 = 0$ *for normal condition*
$I_1 + I_2 + I_3 \neq 0$ *for fault conditions*

Fig. 3-11 *Differential protection for three-terminal network*

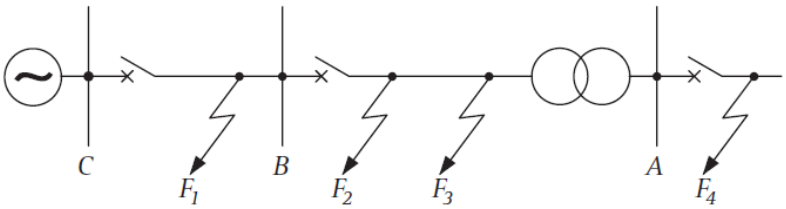
However, the technique is very reliable when the two terminals are close apart. For this reason, this scheme is widely used for the protection of transformers, generators and bus bars. Details can be found in standard textbooks.

3.4.3 Overcurrent Protection

An overcurrent protection scheme detects a fault by monitoring the current flowing in a system and comparing it with a predefined setting. They are usually used for the protection of radial networks but with suitable appropriate coordination, they can be applied to parallel networks. Among the various possible methods used to achieve the correct relay co-ordination are those using either time or overcurrent, or a combination of both. The basic idea is to ensure that each relay isolates only the faulty section of the power system network, without service interruption on the healthy sections of the transmission system.



***(a)** Time discrimination*



***(b)** Current discrimination*

***Fig. 3-12** Overcurrent protection*[54]

As shown in Figure 3.12a, relay *B* is set at the shortest time delay possible. Therefore if a fault occurs at say F, the relay at *B* will operate in *t* seconds to clear the fault before the relays at *C*, *D* and *E* have time to operate. Generally, the time interval *t1* between each relay time setting must be long enough to ensure that the upstream relays do not operate

before the circuit breaker at the fault has operated. The major disadvantage of the time discrimination is that the most severe faults are cleared in the longest operating time.

Discrimination by current relies on the principle that the fault current varies with the position of the fault due to the difference in impedance between the source and the fault. Consequently, the relays controlling the various circuit breakers are set to operate at pre-set values of current such that only the relay nearest to the fault operates. The limitation of the current discrimination is that it relies on appreciable impedance between the points under consideration. To overcome the limitations inherent in the time and current discrimination, the inverse time overcurrent relay was developed, where the time of operation is inversely proportional to the fault level. This type of relay has both time and current settings, which are usually varied to meet the desired applications. Some defined characteristics are the Standard inverse, the very inverse, the extremely inverse and the definite time. Generally, it is not intended to investigate this further as an overcurrent element cannot provide adequate protection for DC lines. However, it can be used to provide an instantaneous trip for secondary protection.

3.4.4 Boundary Protection

A transmission line protection based on transient components without communication links can be referred to as *boundary protection*[57]. In this type of protection scheme, the different time-frequency characteristics of the fault generated transient components between internal and external faults are determined by analysing the frequency response of reflection and refraction coefficients at the boundary[57]. The operating principle is based on the fact that a fault on a transmission line will generate wideband current signals which propagate outward from the point of faults towards the busbar[58][59]. At discontinuities, a portion is reflected and another portion refracted. However, a substantial

amount of the transient current signals, in particular, those in the high frequency range will be shunted by the capacitance posed by the discontinuities.

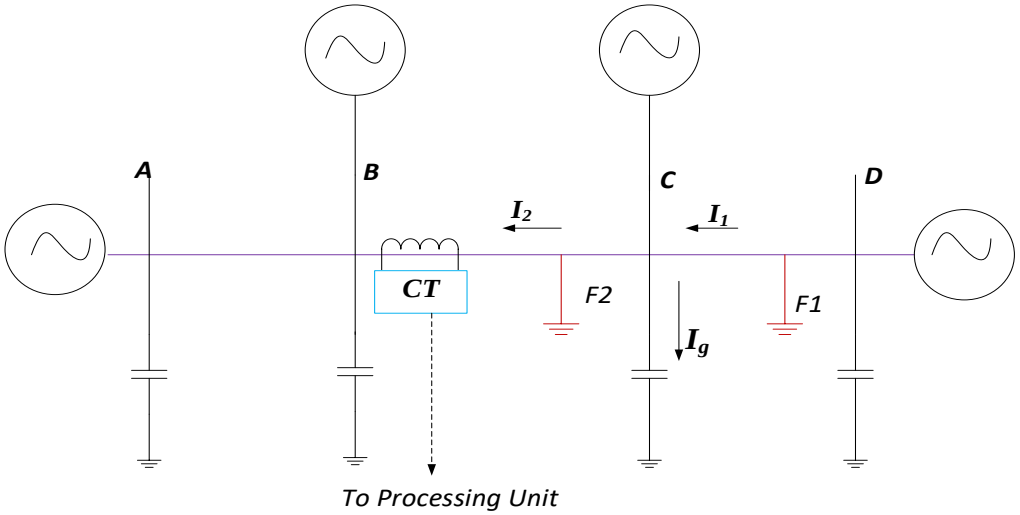


Fig. 3-13 *Boundary protection scheme for AC systems* [59]

Consider fault F_1 of Figure 3.13, with respect to line section *BC*, a wide band current signal will be initiated towards terminal *C* and into line section *BC*. However, some of the signal will be shunted to earth by the bus bar capacitance (I_g as shown). As a result, the fault generated transient signal detected at the relaying terminal located at busbar B will be attenuated compared to the initial I_1. However, there is no such attenuation for an internal fault on the line, such as fault F_2. This principle could be a good discriminant between internal and external faults. A major disadvantage of this technique for use in the DC grid is that it will require complex mathematical computation techniques thus resulting in computational burden and time. A two terminal HVDC line protection technique utilising this concept has been reported in [60], [61]. Generally, boundary protection is still at the research level; however the technique could be explored further for deployment to HVDC network.

3.4.5 Travelling Wave Protection Philosophy

Travelling wave based protection (TWBP) technique provides the fastest means of fault detection in power systems since it utilises the higher frequency content of the fault generated components to detect the occurrence of a fault. The basic principle is to detect the occurrence of the high frequency components at the relay terminals; and use these signatures to detect the presence of a fault on the line under consideration. Generally, the occurrence of a fault on a transmission line will result in voltage collapse at the point of faults and initiate a forward and backward travelling wave. These travelling waves are considered as equivalent to superimposing a voltage at the point of fault, whose magnitude is equal but opposite to the pre-fault steady state voltage[62]. The superimposed components contain sufficient information that can be used for high speed fault identification and protection. These include fault type, fault location and fault direction[63], [64]. The major issue with travelling wave based protection philosophy as used in an AC system is the occurrence of faults at or close to zero crossing of the supply voltage, thus making it very difficult to detect the fault. However, this is not the case in DC systems. Other short comings of the travelling wave based techniques include:

- variation in surge impedance at high frequencies,
- requirement of high sampling rate, (up to 1MHz in some cases)
- problems of multiple reflections,
- interference signals and noise

***Basic theory of travelling waves*:** As shown in Figure 3.14, a fault occurring at a distance l_f from the fault point to the relaying terminal (terminal *'A'* as shown*)* will appear as an abrupt injection at the point of fault. This injection will travel in the form of a wave and therefore propagates in both directions. This wave will be continuously attenuated; and

bounce back and forth between the point of occurrence of the fault and the bus terminals (*'A'* and *'B'* as shown) until the post fault steady state is reached.

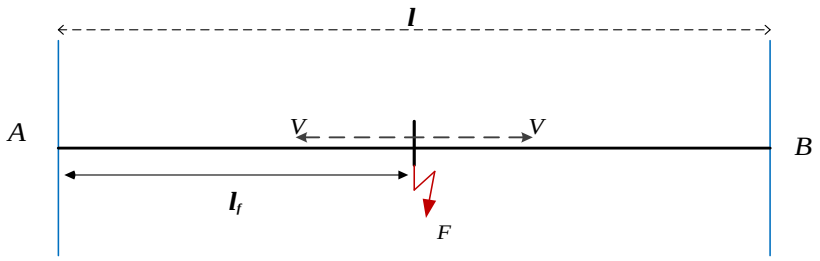


Fig. 3-14 *Propagation of electromagnetic wave during fault*

The transient fault signals recorded at the terminal of the lines will therefore contain multiple and successive reflections. This abrupt change is commensurate with the transient fault signals. If the velocity of propagation is known, the distance to fault can be estimated. The point of fault is denoted by *F* as shown. The actual location of fault can be estimated using either *single-ended* method or *double - ended* method, details of these are presented in Chapter 6.

3.5 Methods of DC line Protection in HVDC systems

The existing DC line protection algorithms developed for HVDC systems including those proposed in literature fall under one or a combination of two or more of the following

- The current derivative technique
- The voltage derivative
- The polarity identification technique
- The differential protection technique
- DC Voltage Level ($\Delta \boldsymbol{V}$) Protection
- DC Current Level ($\Delta \boldsymbol{I}$) Protection
- Travelling wave based protection
- Boundary protection

3.5.1 The current derivative (*di/dt*) based Protection technique

The current derivative or di/dt based DC line protection technique uses the initial rate of rise of the fault current to determine whether a fault has occurred on a particular line under consideration line. As explained in section 3.3, it has been widely used and established for DC traction systems. Also, depending on the direction of fault with respect to the local relay, the calculated di/dt could be positive (for a *forward directional fault*) or negative (for a *reverse directional fault*). For example, considering a section of a transmission network shown in Figure 3.15, the di/dt with respect to the relay is positive for fault F_1 (forward fault) and negative for fault F_2 (reverse fault). Generally, whether a fault is forward or reverse is a matter of convention, depending on the relay reference direction of current.

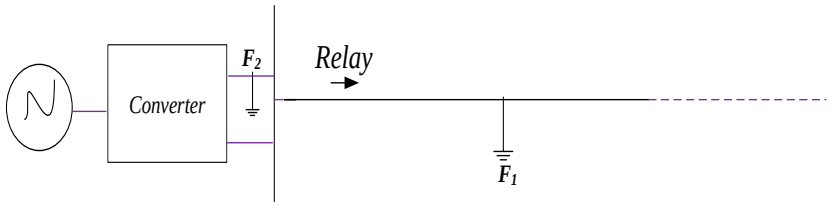


Fig. 3-15 *Positive versus negative* di/dt

Some proposals regarding the application of di/dt protection techniques for two-terminal HVDC [65], as well as for DC grid protection are presented in [66]–[68]. However, the suitability as applied to DC grid is investigated later in Chapter 5.

3.5.2 DC Voltage Derivative (dv/dt) Protection

This is like the *di/dt* and also estimated by the method of sampling. In the voltage derivative method, the DC voltage is continuously sampled and the rate of change dv/dt is determined. A fault is detected when the calculated *dv/dt* exceeds a pre-determined threshold. This technique is widely used for the protection of two terminal HVDC

system[65]. An advantage of this technique is that it is fast in operation. However, its disadvantage is that the sensitivity depends on the fault loop impedance as well as fault distance. The larger the fault loop impedance/distance, the more the magnitude of the measured voltage is damped hence this results in difficulties in detecting faults under these scenarios. However, some proposals for DC grid protection technique utilising voltage derivative has been proposed in [69], [70].

3.5.3 Polarity Identification Technique

The polarity of the transient fault generated signals recorded at the relay terminal following fault inception can also be used to provide directional discrimination between internal and external faults[71]. For an internal fault, the polarity of the transient voltage and current at both terminals of the protected line are of opposite sign.

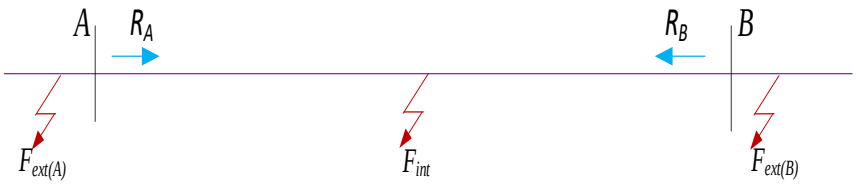


Fig. 3-16 *Polarity identification technique* [71]

However, for external faults, the polarity is the same at one terminal and opposite at the other terminal. This is presented in Table 3.2. However, a major constraint with this technique is the reliance on communication between the local and remote end relays, which results in delay in the response time. However, they are suitable for back-up protection.

Table 3-2 *Polarity Identification Technique* [71]

Fault Type	*Terminal A*		*Terminal B*	
	Δi	Δv	Δi	Δv
Internal , F_{int}	*Positive*	*Negative*	*Positive*	*Negative*
External to A, $F_{ext(A)}$	*Negative*	*Negative*	*Positive*	*Negative*
External to B, $F_{ext(B)}$	*Positive*	*Negative*	*Negative*	*Negative*

The basic principle is explained hereunder. As shown in Figure 3.17, and assuming a fault, *F* occurring on the line as shown. The application of a *fictitious voltage source* at the fault point causes voltage and current travelling waves moving from the fault point F towards the terminals (A and B as shown).

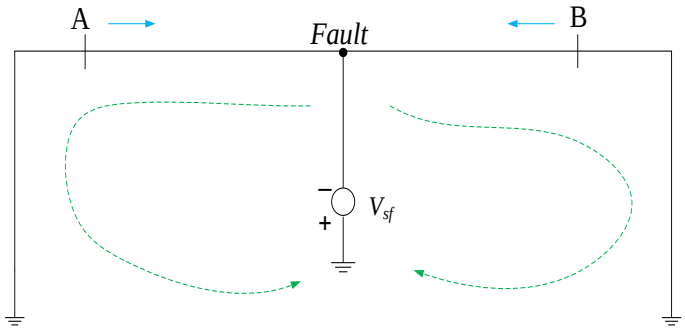


Fig. 3-17 *Basic principle of the polarity identification technique*

Now, assuming that the pre-fault steady state voltage is positive, the fictitious voltage causes a negative voltage wave to travel towards terminals A and B. However, the current waves are positive since the fictitious voltage source, v_{sf} causes current to flow from A to F and B to F respectively. Therefore for the first few milliseconds following fault inception, Δv is negative and Δi is positive at both terminals, where Δv and Δi are superimposed components of the fault generated signals (voltage and current respectively). For external faults, the fictitious source, v_{sf} causes Δi and Δv to have the same polarity at one terminal and opposite polarity at the other terminal. Generally, either the polarity of the superimposed current or voltages (in some cases power) can be compared for fault identification. The practical applications of this principle for HVDC systems has been demonstrated in the work reported in [70][72], [73]. For an internal fault on the DC link, the polarities of the incremental change in the current and voltage at both relay terminals are opposite; whereas for an external fault, the polarities the polarities of the incremental change in the current and voltage at both relay terminals are the same at one end and opposite at the other end. Although this type of protection principle can

provide adequate protection for the entire line, it relies on communication between the relay located at the end terminals, which will result in time delays.

3.5.4 Differential Protection

This involves measuring the current and/or voltage at both ends of the relaying terminals and comparing the difference with a pre-determined threshold to determine whether or not a fault has occurred on the DC line. The differences between the two-measured current sis referred to as *differential quantity*. The information recorded at both terminals is relayed through communication channel (Figure 3.18), hence the integrity (speed and reliability) of the communication channel is a major factor in the accuracy and reliability of this technique. Furthermore, the sensitivity decreases with increase in line length due to charging and discharging current resulting from voltage variations [74]. As shown in Figure 3.18, a fault occurring along terminal *AB* is detected when the difference between the measured current at the two converter station exceeds a predetermined value. The direction of current shown is arbitrary. Generally, these differences can either be positive or negative depending on the location of the fault.

Current differential protection technique used in LCC HVDC system has been reported in [75]. A differential protection scheme utilising the incremental change in transient energy at both terminals following the occurrence of fault has also been reported in [76]. A DC grid protection technique incorporating current differential, where the sign convention is used to provide the discriminant is also proposed in[19], [77], [78]. A pilot protection scheme utilising traveling wave current polarity for application to MT-HVDC system has also been reported[72].

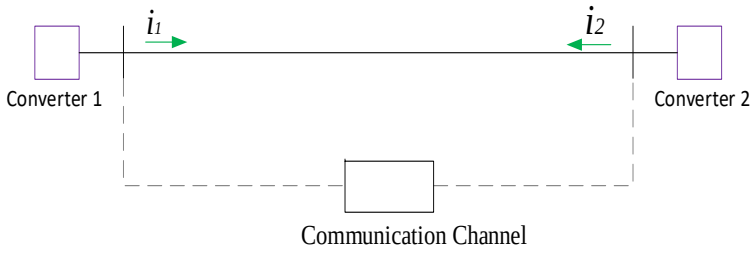


Fig. 3-18 Current differential Protection Technique

As shown, under steady state conditions, the differential current, $i_1 - i_2$ *is ideally zero.* However, during fault condition, this condition is no longer met. A DC link fault is detected when the differential current exceeds a predetermined setting.

3.5.5 DC Voltage Level (ΔV) Protection

The DC voltage level protection technique operates by responding to voltage depressions over a long-time interval following the occurrence of close-up or high impedance faults. This method is widely used in two-terminal HVDC systems[75], and is generally used as a back up to voltage derivative or travelling wave protection [74]. An advantage of this method is that it does not rely on communication channels

3.5.6 DC Current level (ΔV) Protection

This is like the ΔV protection, but a fault is detected when there is an incremental change in the current and as such generally referred to as *overcurrent protection*. They are widely used in low voltage DC systems such as DC traction systems in conjunction with *di/dt.* Its application to DC grid has been proposed and is reported in[67]. A similar approach utilising fault current limiter (FCL) has also been reported in [79].

3.5.7 Travelling wave based protection principle for HVDC systems

The principle is the same as those used for HVAC systems. Proposals regarding travelling wave based protection principles for HVDC systems is reported in[80]–[86]. A proposal regarding the application of travelling wave protection for DC grids has been reported in [87], [88]. However, a major issue when adopted for the protection of DC grid is that it relies on reflections (or multiple reflections) between the fault and the relay terminals

thereby incurring delay. These include the philosophies used in the traditional HVAC systems as well as those proposed for HVDC systems including HVDC grids. However, the studies carried out show that the reliance on successive reflection of the travelling wave components at the relay terminal for fault identification imposed some limitations on its use for DC grid protection. The reliance on complex DSP techniques would also imposed some computational burden as well as incurring delays. This is because the wave propagation delay time may be longer than the time required to detect and clear the fault. This is a major issue to be considered when deploying travelling wave based protection principle for application to DC grids. Therefore, new travelling wave based protection (TWBP) techniques are required to be designed and developed for application to DC grids.

3.5.8 Boundary Protection

This is similar to that proposed for HVAC system where the frequency character of the fault generated transient are extracted for fault identification. A two terminal HVDC line protection technique utilising this concept has been reported in [60], [61]. However, none of such technique has been reported for DC grid protection

3.6 Options and Strategies for DC grid protection

In view of the analysis above, and considering studies already proposed in literature, the assorted options and strategies in consideration for DC grid protection are presented in this section

3.6.1 "Unit" Versus "non-unit" based protection principles

Generally, the protection techniques discussed above fall under two categories - *unit and non-unit based.* Protection schemes relying on information from the local end terminal are referred to as *non-unit* protection scheme while those relying on information from

both the local end and remote end terminals are referred to as unit protection scheme. The information here referred to the current and voltage superimposed signal recorded at the relaying terminal following fault inception. Distance protection, overcurrent protection, under voltage, *di/dt* and *dv/dt* are examples of *non-unit* type of protection. An advantage of the *non-unit* protection scheme is that they do not require communication channel and as such no communication delay. Examples of unit protection are current differential protection and polarity identification technique. For a protection to be reliable and fast in operation and considering the time requirement for DC grid protection, the primary or main protection must be a non-unit type protection technique. However, the secondary or back-up protection could be unit – type protection.

3.6.2 Transient and steady-state based protection principles

Protection techniques and principles could also be classified as either steady state based or transient based. Those protection techniques which are based on the character of the transient components of the fault generated signal (voltage or/and current) are regarded as transient based protection; whereas those based on the character of steady state components of the fault generated signals are referred to as steady state based protection. The traditional distance protection techniques applicable to AC systems is an example of steady state based protection technique whereas travelling wave and polarity identification technique, current and voltage derivative protection techniques are regarded as transient based.

Conventional HVAC systems uses the steady state based protection algorithm such as the distance protection, thereby given the protection system enough time to detect the fault. However, in DC system the fault must be detected and cleared during the transient state. These parameters that vary with distance during the transient state such as the inductance could be used, thereby paving the way for a distance protection strategy. An attempt was

made to relate the initial rate of rise of the fault current with the loop inductance, thereby estimating the fault distance, the findings are presented in section 4

3.6.3 "Blocking" versus "non-blocking" HVDC converters

As discussed in section 2.5.3, MMC based HVDC are the most preferred converter topology for application to DC grid due to its technical advantages compared to other VSCs. The protection principles for DC grid can either be archived using either of the two MMC submodules configurations, the half bridge (or non-blocking converter) or the full bridge (blocking converters) HVDC converters[19], [68], [69]. Generally, the non-blocking converters are not able to block fault currents whereas the blocking converter does.

"Non-blocking" HVDC converters: In this technique, it has been proposed to place DC circuit breakers at both ends of the DC overhead lines or cables[69]. During DC side faults, the faulty segment is isolated without interrupting the operation of the remaining converters connected to the healthy section of the grid (Figure 3.19a). The major advantage of this technique is that it does not require a total shut down of the entire grid. Furthermore, active power transfer can be restored immediately following fault clearance

"Blocking" HVDC converters: This involves blocking the converters using the full bridge MMC HVDC model and thereafter isolating the faulty section using fast mechanical switches during DC side faults in any of the sections (Figure 3.19b). An advantage of this technique is that the converters can provide voltage support throughout the contingency. However, a major disadvantage of this approach is that a considerable amount of time is taken to re-establish the active power transfer on the healthy section of the DC grid [68].

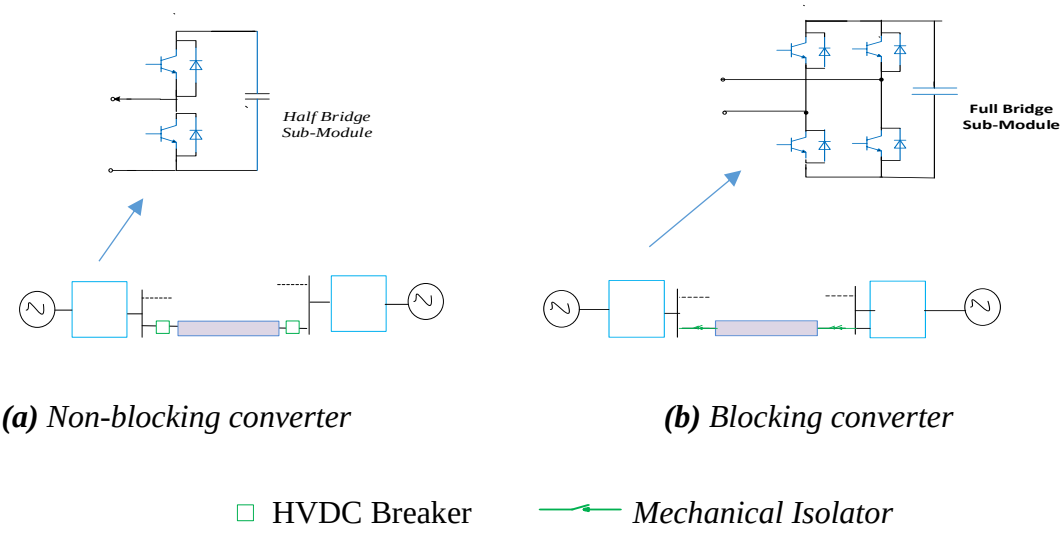


Fig. 3-19 *Blocking and non-blocking Converter Protection Strategies*

3.6.4 Use of AC side Circuit Breakers

This involves tripping the AC side circuit breakers at all converter stations and thereby disconnecting the whole grid once a DC line /cable fault is detected. (Figure 3.20). The converters are later connected to the grid when the faulty sections have been isolated using fast DC switches or isolators. The major disadvantages with this method are that the power flows in the healthy sections are disrupted. Furthermore, this technique requires an extended period in re-establishing the reactive power of the converters and the active power transfer on the healthy part of the DC network once the faulty section is isolated.

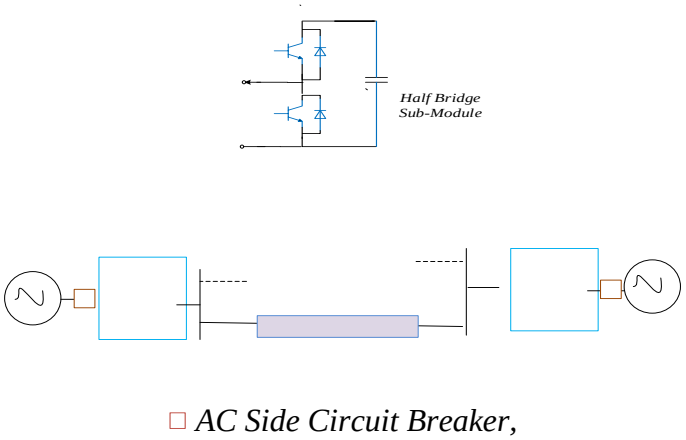


Fig. 3-20 *Protection strategy utilising AC side circuit breaker*

Clearly, the use of DC side circuit breakers is the most desirable for the protection of DC grids and as such the protection technique adopted in this research assumes a DC side breaker located at the ends of the lines/cables. Generally, and in some cases fault current will be installed alongside DC breakers as part of the protection strategies for the future DC grid. This will help to reduce the *di/dt* during DC side short circuit conditions which will give the breaker time to operate.

3.7 Summary

The chapter explores the protection issues associated with HVDC grid developments such as the nature of a DC short circuit fault. The study revealed that the nature of DC short circuits in HVDC grids demands that the fault current must be interrupted as quickly as possible, hence the need to develop a fast fault detection algorithm for DC grids. The basic requirements for DC grid protection as well as protection strategies for DC grids were also studied. The study revealed that for a protection scheme to be secure and reliable, it must be *non-unit transient based*.

Having explored the existing protection philosophies applicable to AC systems, DC traction systems and existing two terminal HVDC systems, as well those proposed in literature for DC grid, an attempt is now made to develop a new DC line protection technique for application to DC grid. However, there must be a compromise considering sensitivity, reliability, stability and speed of operation of the various techniques discussed above. For example, if a protection system has higher sensitivity, it may somehow be less secure. Also, a protection system with higher selectivity may not operate as fast as required. For example, the travelling wave and voltage derivative are currently being used for two-terminal HVDC protection are fast in operation but insensitive to high impedance faults. (the higher the fault resistance or fault distance, the poorer the sensitivity); and

as such may not guarantee absolute selectivity, considering the length of the transmission lines/cables.

Furthermore, the polarity identification as well as the current differential techniques relies on a communication channel between the local and remote end relays and as such may not be suitable for primary protection, whereas they can provide full selectivity. In an analogous way, the under-voltage and over-current technique will be too slow to act considering the time constraints in detecting and discriminate the fault. Generally, it can be said that *non-unit* protection scheme provides fast fault protection but cannot provide absolute selectivity, whereas unit protection schemes can provide protection for the entire line/cable length but are somewhat slow in operation compare to *non-unit scheme*.

In summary, the optimal protection technique for DC grid should possess the following attributes

- Must be transient based.
- Must be selective – able to isolate only the faulty section without interrupting the heathy section of the grid.
- The primary protection must be a non-unit scheme
- It must be fast in operation
- It must be insensitive to noise and normal load transients including lighting conditions
- The secondary (or back) protection could either be unit or non-unit

In order to provide full protection coverage for the entire line/cable length without compromising selectivity, the possibility of adopting the so-called hybrid protection technique may be a suitable way forward. Examples have been reported in [70], utilising *dv/dt* and polarity identification; [67] utilising the differences in the magnitude of the

di/dt measured at the local and remote end terminals as well as in [68] where a *dv/dt* supervised di/dt was used. Reference [89] also presented a hybrid protection technique utilising travelling wave and boundary protection. Proposals regarding the use of signal processing as well as optical sensors have also been reported in[26], [90], [91].

In all, the key issue is to develop a method for the fast fault detection in DC lines for application to DC grids. However, as protection algorithms are usually developed based on the characteristic difference between internal and external faults, the starting point therefore will be an understating of the characteristic differences in the fault current footprints associated with diverse types of fault scenarios, such as internal versus external fault. The study carried out in this regard is explained in Chapter four

Chapter 4

4 Fault Characterisation in DC Systems

4.1 Introduction

In this chapter, characterisation of faults in DC systems is presented. This includes six pulse rectifiers which are representative of a DC traction system and thyristor based LCC HVDC systems. Thereafter, the work was extended to a VSC-HVDC system. The MMC based HVDC system was considered since modern VSC HVDC system will be based on MMC due to their advantages over the two-level VSCs such as flexibility in control and scalability. Simulation results based on full scale MMC-HVDC models are also presented. The characteristic differences between a *P-P* and *P-G* faults, effects of fault resistance, effect of fault distance as well as the effect of the variation in the DC side inductor is also presented. In all, the aim was to determine the characteristic footprints with a view to developing a suitable DC line fault detection technique for application to HVDC grids.

4.2 Analysis of Short Circuits in DC Systems.

4.2.1 Short Circuited Six Pulse Converter

Six pulse rectifiers are the basic building blocks of a DC traction substation, as well as the LCC based HVDC systems. The term *six pulse* is due to six commutations or

switching operations per period. This results in a characteristic ripple of six times the fundamental frequency in the DC output voltage. Details of the operating principle and the different modes of operation of a six pulse converter are outside the scope of this research but can be found in standard textbooks. The equivalent circuit of a six pulse bridge converter operating under short circuit is shown in Figure 4.1. For simplicity, the converters are represented by diodes which are representative of a thyristor operating at zero firing angle. As shown, a short circuit at the terminal of the converter is equivalent to a three-phase short circuit on the AC side.

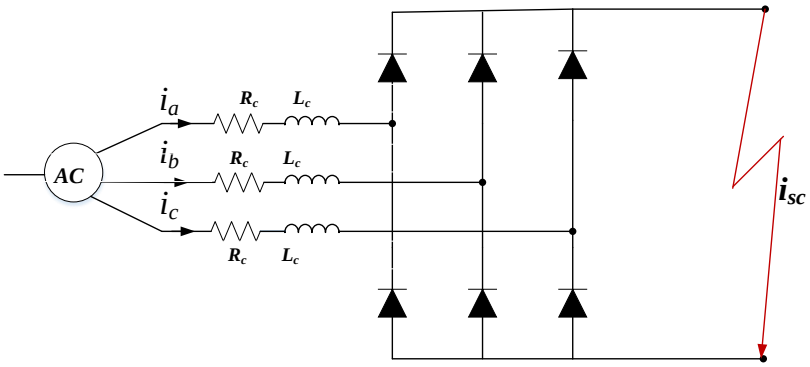


Fig. 4-1 *Six Pulse Rectifier operating under bolted fault*

R_c and L_c are the source resistance and inductance respectively.

4.2.2 Prediction of short circuit current

The procedure for calculating the short circuit current in DC auxiliary system are well stipulated in the IEC 61660 Standard[92]. Analysis of short circuit in six pulse rectifier is also well documented in [93]–[97]. However, for this study, three analytical methods for calculating the current arising from a fault in DC systems six pulse bridge rectifier are reviewed.

All techniques were verified by simulations using Simulink to ascertain their suitability in predicting the transient behaviour of the fault current during a DC side short circuit.

The techniques studied included that proposed by Denning [96]; Pozzobon [95] and Fujimura and Honda's Model[97]. Details of the parameters used for this study are given in Table 4.1 and are computed as presented hereunder.

The parameters used in this calculation are based on a 1MVA traction transformer with 5% impedance, and on its own base. For this study, the X/R ratio was taken as 20 while the DC voltage was taken as 750V as in London underground.

$$V_{DC} = \frac{3\sqrt{2}}{\pi} .\sqrt{3}\ V_{Phase} \qquad (4\text{-}1)$$

$$\therefore\ V_{Phase} = \frac{750 \times 3.142}{3 \times \sqrt{2} \times \sqrt{3}}$$

$$= 320.67V$$

$$Source\ Reactance,\ X_c = P.U\ reactance \times \frac{(kV)^2}{MVA} = 0.06\ \times \frac{0.3207}{1.12} = 5.310m\Omega$$

$$\therefore Source\ Resistance,\ R_c = \frac{5.310 \times 10^{-3}}{20} = 0.275m\Omega$$

$$Source\ Inductance,\ Lc = \ = \frac{Xc}{2 \times 3.142 \times 50} = \frac{5.310}{2 \times 3.142 \times 50} = 0.018mH$$

Table 4-1 DC traction Parameter for Figure 4.1

MVA Rating of traction transformer	1 MVA
% Reactance of traction transformer	5%
X/R Ratio of traction transformer	20
Source Reactance, X_c	5.310 mΩ
Source Resistance, R_c	0.275 mΩ
Source Inductance, L_c	0.018mH

Now as indicated by Denning [96] and if the AC system is balanced, a short circuit fault on zero impedance on the DC side is equivalent to a balanced three phase short circuit on the AC side. In that case, the DC side transient current can be obtained by taking the sum of the positive portion of the short circuit currents on the DC side and summing them. By analysis of Figure 4.1, the short circuit current in the three phases, i_a, i_b and i_c were obtained[96].

Thus

$$i_a = \frac{v_p}{Z}\left(\cos(\omega t - \varphi) - e^{\left(-\frac{t}{\tau_{sc}}\right)}\cos(-\varphi\right) \quad (4\text{-}2)$$

$$i_b = \frac{v_p}{Z}\left(\cos(\omega t - \varphi - 120^0) - e^{\left(-\frac{t}{\tau_{sc}}\right)}\cos(-\varphi - 120^0\right) \quad (4\text{-}3)$$

$$i_c = \frac{v_p}{Z}\left(\cos(\omega t - \varphi + 120^0) - e^{\left(-\frac{t}{\tau_{sc}}\right)}\cos(-\varphi + 120^0\right) \quad (4\text{-}4)$$

Where,

$$\tau_{sc} = \frac{L_c}{R_c}; \qquad \varphi = \tan^{-1}\frac{\omega L_c}{R_c}; \qquad Z = \sqrt{R_c^{\,2} + X_c^{\,2}}$$

ω is the angular frequency of the AC system voltage.

The resulting wave forms are shown in Figure 4.2.

The analysis carried out by Pozzobon[95] is like that carried out by Denning[96] . However in this case, the short circuit current was computed by considering the envelope of the maximum current in the three phases. The waveform for this is shown in Figure 4.3.

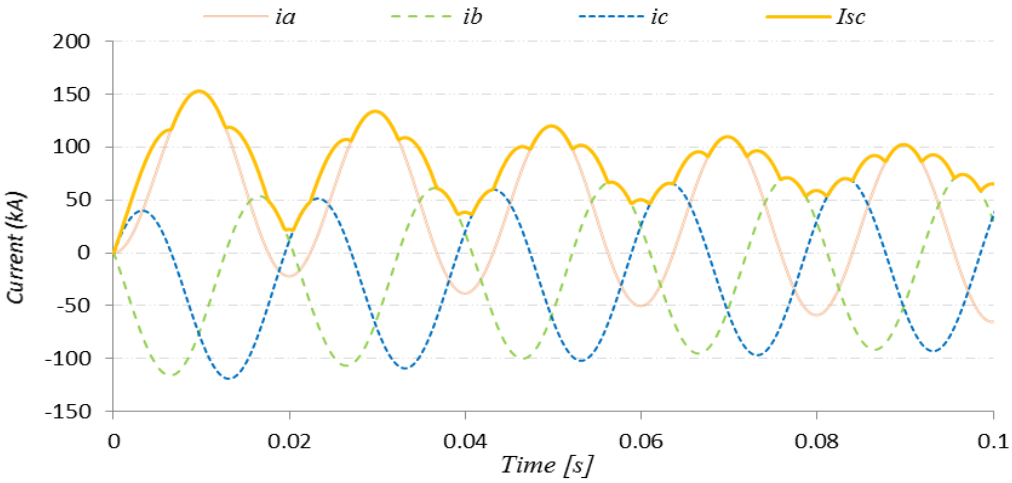


Fig. 4-2 *Calculated short Circuit Current Based on Denning approximation* [96]

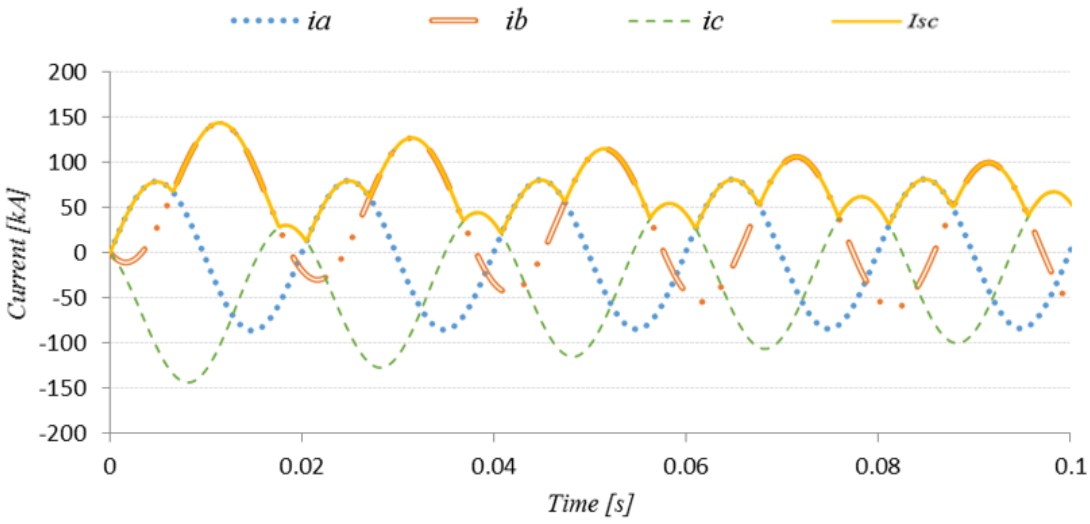


Fig. 4-3 *Calculated short Circuit Current Based on Pozzobon approximation*[95]

The work carried out by Fujimura and Honda's Model [97] represented a six pulse bridge rectifier operating under a short circuit by an equivalent DC voltage source, v_{do} in series with a resistor, R_{eq} and an inductor, L_{eq} (Figure 4.4)

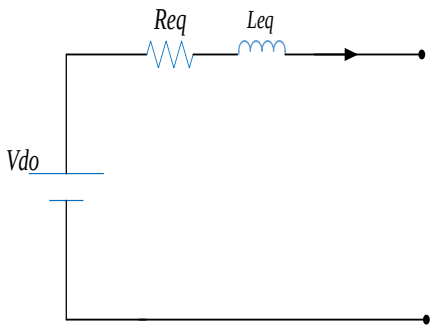


Fig. 4-4 *Equivalent Linear DC Power Source based on Fujimura and Honda's Model* [97]

Thus

$$R_{eq} = 1.5R_c + \frac{3\omega L_c}{\pi} \quad (4\text{-}5)$$

$$L_{eq} = 1.5L_c \quad (4\text{-}6)$$

v_{do} is the open circuited voltage of the six pulse bridge rectifier and is given by

$$v_{do} \approx \frac{3\sqrt{3}\, v_p}{\pi} \quad (4\text{-}7)$$

v_p is the peak DC voltage whose magnitude is equal to the peak value of the AC line voltage

The instantaneous short circuit current, i_{sc} was then be calculated by the use of Equation 4.8

$$i_{sc} = \frac{v_{dc}}{R_{eq}}\left(1 - e^{\left(-\frac{t}{\tau}\right)}\right) \quad (4\text{-}8)$$

Where τ is the circuit time constant and is expressed as

$$\tau = \frac{L_{eq}}{R_{eq}} \quad (4\text{-}9)$$

Based on the Equation 4.8, the plot shown in Figure 4.5 was obtained.

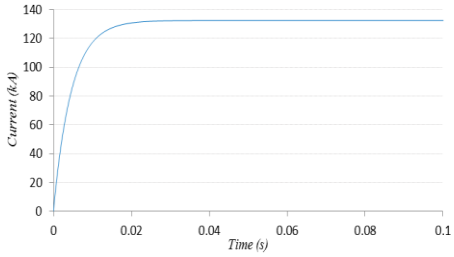


Fig. 4-5 *Short Circuit Current Based on Fujimura and Honda's Model*[97]

As expected, the fault current characteristics is an exponential rise. However, compared to the plots shown in Figures 4.2 and 4.3, the shortcoming of this method is that it fails to account for the commutation in the rectifier and hence gives somewhat unrealistic fault characteristics. The DC short circuit current was also obtained by simulating the circuit shown in Figure 4.1 based on the parameters given in Table 4.1. The Simulink model is given in Figure 4.6. All three techniques (References [95]–[97]) were compared against simulation result and the combined waveforms are presented in Figure 4.7.

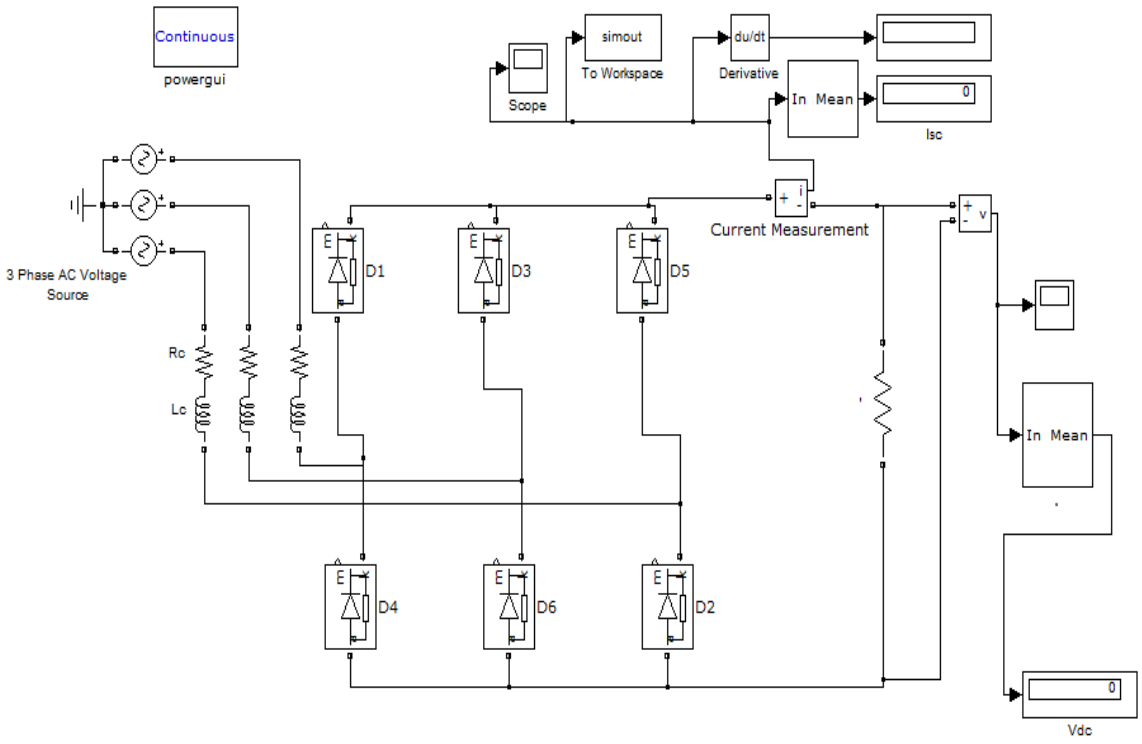


Fig. 4-6 *Simulink model for figure 4.1*

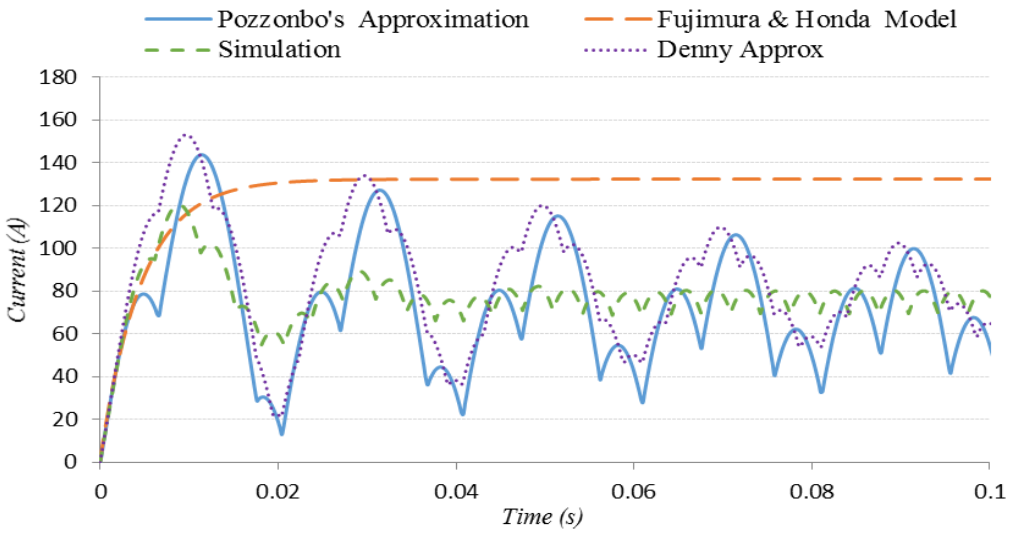


Fig. 4-7 *Comparison of the calculated short circuit current*

4.2.3 Discussion of results

The analysis carried out and considering the plots of Figure 4.6, shows consistency in their initial rate of rise and as such they can be used to predict the magnitude and rate of rise of the short circuit current for close – up faults in a six pulse rectifier, which is representative of a six pulse converter. Although there are significant differences in the post-fault steady state value, however this is not a major issue in this study as any fault detection algorithm or strategy must rely on the magnitude of the super-imposed components during the transient state. The expanded scale of Figure 4.7 is shown is shown in Figure 4.8.

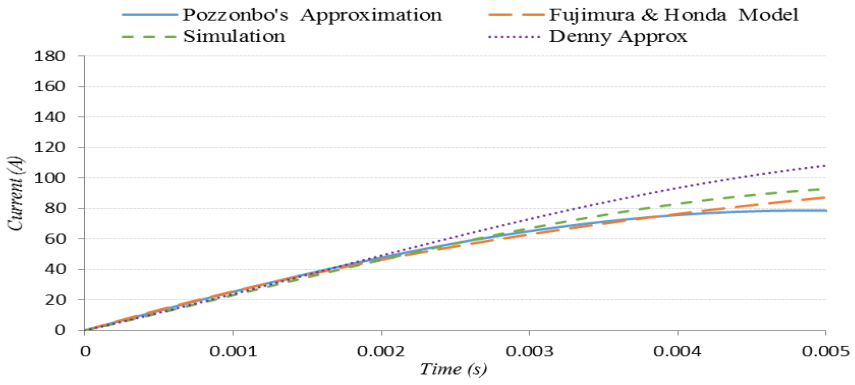


Fig. 4-8 *Comparison of the calculated short circuit current on an expanded scale*

Now, considering Figure 4.7, for up to say, *2ms* after the inception of the fault, it can be hypothesised that the initial rate of rise (*di/dt*) of the fault current is approximately linear and can be expressed by

$$i_{sc} = \frac{di}{dt} \times t \tag{4-10}$$

Based on Figure 4.7, the initial value of *di/dt* obtained from References [95]-[97] respectively; and that from simulations over *t=0 to t=0.002s* is given in Table 4.2. The results shows consistencies with those obtained from simulations.

Table 4-2 *Calculated initial di/dt based on Figure 4.7*

Model	Initial Rate of Rise, (*kA/ms*)
Denning's	24.70
Pozzonbo	23.97
Fujimura & Honda	23.16
Simulation	22.36

The percentage deviation of the key indices from the value obtained from the calculated value are presented in Table 4.3

Table 4-3 *Percentage deviation of the key indices*

Model	Percentage deviation (%)
Denning's	10.40
Pozzonbo	7.20
Fujimura & Honda	3.58

Now, recall that the current through an inductor in a resistive - inductive circuit is given by the expression below,

$$v_{dc} = L_c \frac{di}{dt} + iR_c \tag{4-11}$$

Then by differentiation and if *t=0*, the initial rate of rise can be expressed as.

$$\left|\frac{di}{dt}\right|_{t=0} = \frac{V_{dc}}{1.5 L_c} \tag{4-12}$$

Substituting the values of v_{dc} and L_c given in Table 4.1 into Equation 4.12, the initial rate of rise was calculated to be 28.571.4 *kA/ms*. This value is consistent with those presented in Table 4.2. This shows that provided the initial *di/dt* can be estimated during the first few milliseconds, the resistance of the fault loop path can be neglected.

As shown, there are appreciable differences between the calculated short circuit current and those obtained by simulation. In this study, this differences was regarded as insignificant as all models indicated can be used to predict the initial rate of rise of the fault current. However as Simulink is an established software used by both academics and industries, the results obtained by the use of Simulink was used as a basis to validate all other models. Therefore the results obtained as shown in Figure 4.7 and 4.8 are assumed to be valid in this study. Therefore all models shown are able to predict the short circuit current in DC systems.

Generally, the accuracy of a measurement depends on the time when measurements are taken, thus the closer *t* is to zero, the more accurate the result would be. This shows that Equation 4.12 can be used to estimate the initial *di/dt*. However, in the case of DC grid, the effect of the distributed line parameters must be accounted for due to oscillations in the fault current profile which ultimately will impact on the accuracy of the estimated *di/dt*. This was investigated against a full scale DC grid and findings reported in Chapter

5. However, the fault characterisation on HVDC systems based on equivalent circuit was also carried out and findings are presented hereunder.

4.3 Fault Characterisation in HVDC Systems Based on Equivalent Circuit

The analysis of short circuit in DC traction systems which are representative of LCC HVDC systems have been carried out as presented previously. Attempts have also been made to analyse the short circuit in VSC HVDC system[98], [99]. However, as modern HVDC system including MT-HVDC system will be based on MMCs, priority was given to fault current analysis in MMC-HVDC system. The short circuit analysis carried out is based on the topology of the *half – bridge MMC, the* results of the findings are presented hereunder.

4.3.1 Simplified equivalent circuit

The simplified equivalent circuit of a *MMC* converter operating under a *P-P* short circuit remote fault is shown in Figure 4.9

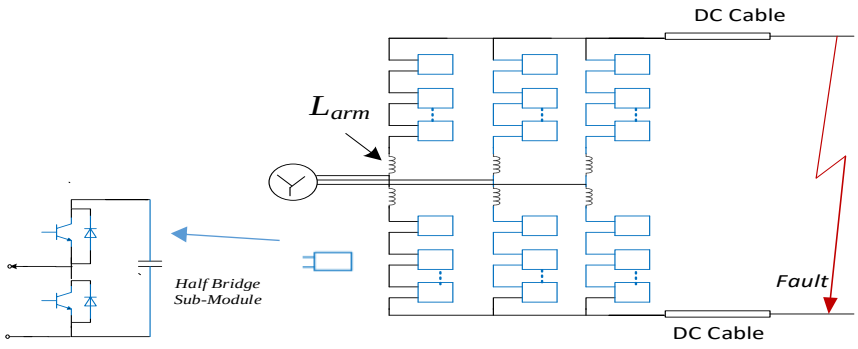
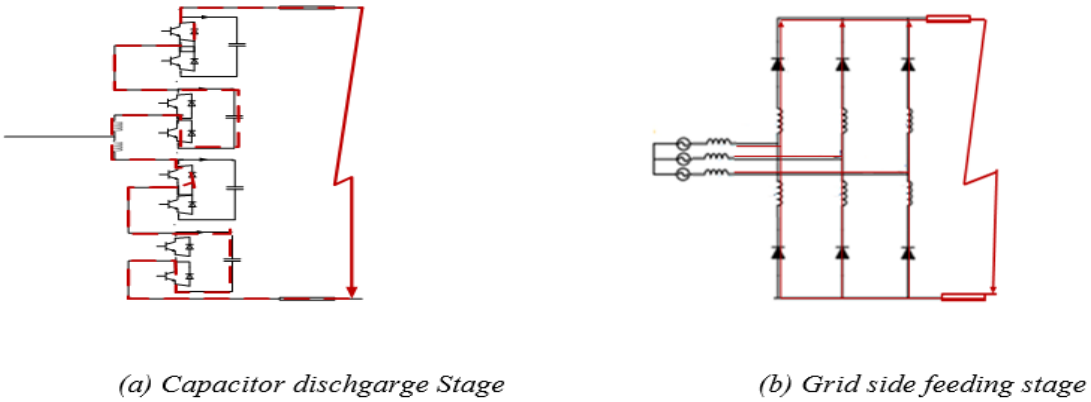


Fig. 4-9 Equivalent Circuit of a MMC during a P-P Fault

The short circuit process consists of two stages - the *capacitor discharge stage* and the *AC (grid-side) feeding stage*.



(a) Capacitor dischgarge Stage *(b) Grid side feeding stage*

Fig. 4-10 Paths of short circuit current for an MMC following a *P-P* fault

The capacitor discharge stage: This stage represents the first few milliseconds following the inception of the fault and the current discharged from the *SM* capacitance as well as those resulting from the parasitic components of the transmission systems (inductance and capacitance respectively) are the main component of the short circuit current. During this stage (Figure 4.10a), the capacitor in the *SMs* will discharge and the MMC will remain operational until it is blocked following the detection of the fault. Once the IGBTs are blocked, the AC side current will continue to flow through the free wheel diode. This stage is called the grid (or AC) side feeding stage. If the fault is not cleared, the current overshoot resulting from the discharge of current from the *SM* capacitance would be continually supported by the AC current flowing through the freewheeling diode even if the capacitor discharging current decays to zero. However, this is an undesirable condition for the entire system and its intended in this study to detect and isolate the fault well before this stage.

4.3.1 The Equivalent Inductance and capacitance

Considering the DC side of the circuit arrangement shown in Figure 4.8, the upper and lower arm inductor, L_{arm} in one phase (or leg) can be seen to be connected in series and

hence the total inductance per phase (or leg) is $2L_{arm}$. Since there are three legs in parallel, the equivalent inductance, L_{eq} of the converter is $(2/3)L_{arm}$ (Figure 4.11)

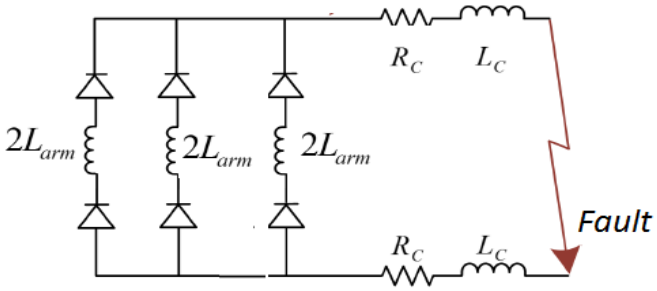


Fig. 4-11 Equivalent Arm inductance following a *P-P* fault in an MMC-HVDC

Assuming that an arm of the MMC consists of N_{SM} SMs, then the per phase number of SMs inserted is always N_{SM}. This is because only half of the submodules are inserted during normal steady state operating condition [38]. If capacitive voltage balancing is also assumed, the voltage of all six SMs ($or\ 6N_{SM}$) in the six arms are assumed to be the same. Since the energy stored in the equivalent capacitor of the converter equals the energy stored in the whole *SM* capacitor, the following equations can be written[38]:

$$\frac{1}{2}C_{eq} \times {V_{DC}}^2 = \frac{1}{2}\left(C_{SM} \times {V_{SM}}^2\right) 6N_{SM}. \qquad (4\text{-}13)$$

V_{SM}= submodule voltage

C_{SM} = submodule capacitance

C_{eq}= converter equivalent capacitance

$$V_{SM} = \frac{V_{DC}}{N_{SM}} \qquad (4\text{-}14)$$

Combining Equations 4.13 and 4.14 yields

$$C_{eq} = 6\,\frac{C_{SM}}{N_{SM}} \qquad (4\text{-}15)$$

However, as the capacitive discharge period is short, the equivalent capacitive voltage can be regarded as constant during this period. For this reason, the equivalent *SM*

capacitances were replaced by their equivalent DC voltages (Figure 4.11) during the capacitor discharge stage. This was also reported in the work presented in reference [100]**.** The DC cable was modelled using the Pi - cable model. R_c, L_c and C_c are the cable resistance, inductance and capacitance respectively. The converter and cable parameter used for this study are presented in Table 4.4. The simplified equivalent circuit of the MMC-based HVDC system is given in Figure 4.12. All simulations were carried out in Simulink (Figure 4.13) for various fault distances and the results obtained are presented in Figure 4.14.

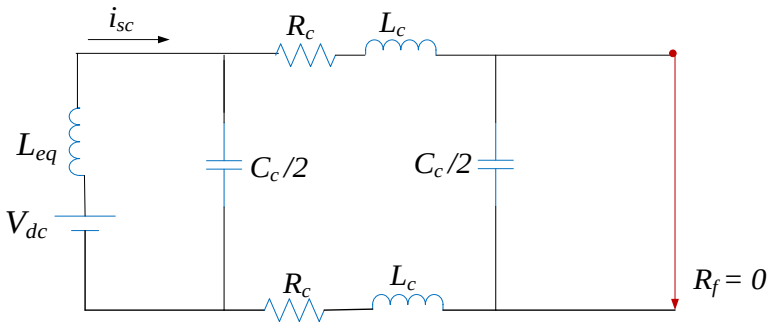


Fig. 4-12 *Equivalent circuit of MMC based HVDC following a DC short circuit*

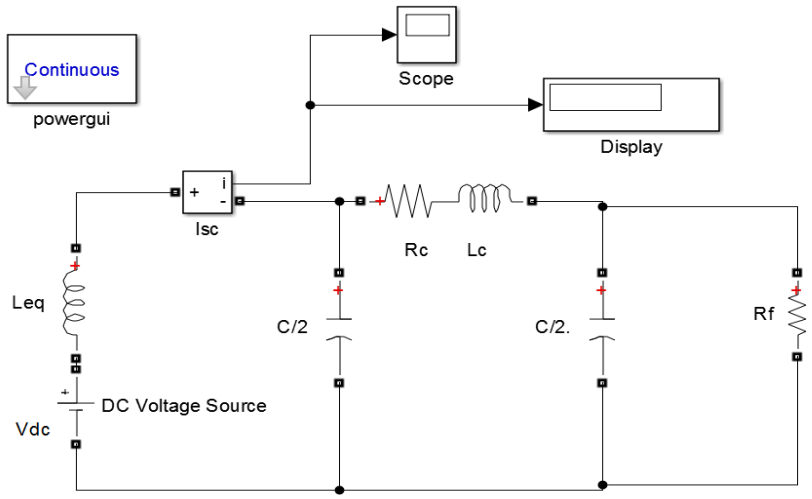


Fig. 4-13 *Simulink model for Figure 4.11*

The equivalent inductance was obtained. Thus

$$L_{eq} = \frac{2}{3} \times 33.42mH = 22.28mH$$

As shown in Figure 4.14, there is an oscillation in the fault current profile especially for short distance fault. This oscillation is attributed to the cable capacitance and was found to reduce with increasing fault distance. A $100mH$ low resistance reactor which is typical of a HVDC breaker was placed in series with the DC cable (Figure 4.15).

Table 4-4 *Parameters for the equivalent circuit of MMC shown in Figure 4.12* [38]

Parameters of MMC	***Values***
Rated capacity of converter transformer	$420\ MVA$
Nominal ratio of converter transformer	$220kV/150kV$
Leakage reactance of Converter transformers	10.5%
AC side impedance	$5 + 5\,j\,(\Omega)$
Line-to-neutral Nominal AC voltage	$220\ kV$
Nominal DC voltage	$\pm 150\ kV$
Converter nominal power	$300\ MW$
Number of Submodules per arm (N_{SM})	20
Submodule capacitor	$765\ \mu F$
Arm inductor	$33.42mH$
DC cable resistance, R_C	$2 \times 10^{-2}\ \Omega/km$
DC cable inductance, L_C	$1.91 \times 10^{-4}\ H/km$
DC cable capacitance, R_C	$2.95 \times 10^{-2}\ \Omega/km$
DC smoothing inductance	$50mH$

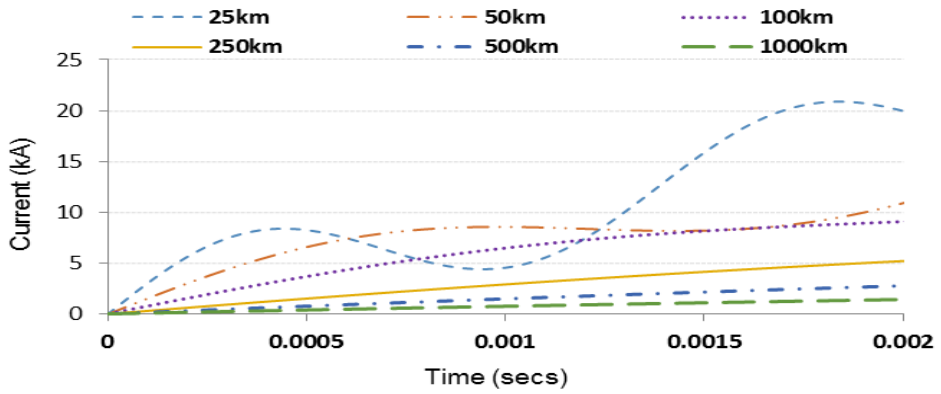


Fig. 4-14 Plots of short circuit current for varying fault distances

The purpose of this is to investigate the inductive effect of the inductor on the fault current profile. In practice, the DC inductors are located at the lines /cable ends to reduce the *di/dt* during DC short circuit. From Figure 4.15, the total series inductance, L_T considering the DC link inductor is

$$L_T = L_{eq} + L_S + L_C \qquad (4\text{-}16)$$

$L_s =$ DC smoothing inductor

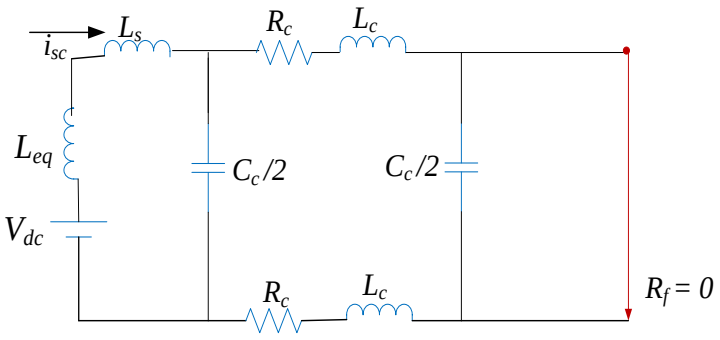


Fig. 4-15 *Equivalent circuit of MMC based HVDC following a DC short circuit with DC link inductor*

As shown in Figure 4.16, the inclusion of the DC inductor provided significant amount of damping, thus making the initial rate of rise to be linear.

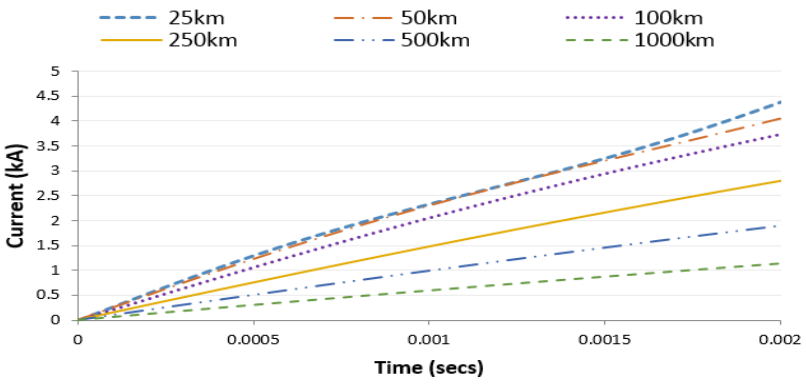


Fig. 4-16 Plots of short circuit current for varying fault distances with damping inductor

Generally, DC inductors help to attenuate the high frequency components in the fault current profile, which ultimately result in the reduced magnitude of the fault current profile. Now, still considering Figure 4.16 and neglecting the effect of the cable resistance at the instant of fault inception, the initial rate of rise (or *di/dt*) of the fault from the time of fault inception until time, *t = 0.5ms* was estimated and thereafter the system fault loop inductance calculated. Thus

$$|di_{DC}/dt|_{\ t\to 0} = \frac{V_{DC}}{L_T{}'} \tag{4-17}$$

$|di_{DC}/dt|_{\ t\to 0}$ = initial rate of rise of the fault current.

$$L_T{}' = \frac{V_{DC}}{IRRC} \tag{4-18}$$

$L_T{}'$ = Calculated system loop inductance.

Based on Equation 4.18, $L_T{}'$ was calculated for varying fault distances and the results obtained were compared with the values of L_T obtained from simulations from Figure 4.16. The results obtained as presented in Table 4.5 shows the suitability of the technique in estimating the system inductance from the initial rate of rise of the fault current. However, as the system resistance as well as capacitances may impact on the accuracy, the initial di/dt must be measured very close to a time, *t =0* so as to guarantee a high degree of accuracy

Table 4-5 Calculated versus actual loop inductance

Fault Distance (km)	$L_T\ (H)$	$L'_T = \frac{V_{DC}}{IRRC}\ (H)$	% Error
25	0.132	0.127	3.788
50	0.142	0.130	8.450
100	0.161	0.145	9.938
250	0.218	0.202	7.340
500	0.313	0.302	3.514
1000	*0.504*	*0.503*	*0.198*

The additional DC smoothing inductor added to the line was found to increase the accuracy of the technique. Generally, the larger the smoothing reactor, the smoother the fault current profile but at the expense of cost. This implies that a compromise will have to be reached, taken into consideration the accuracy and the additional cost posed by the smoothing inductor. An advantage of this technique is a *non-unit* system of distance protection and as such no information from remote end converter station is required. This eliminates the requirement of a communication channel.

Now, from the above analysis, a distance protection strategy could be formulated by comparing the calculated loop inductance following the occurrence of a fault and comparing with a threshold (or setting). For example, in the traditional distance protection strategy developed for HVAC system, if the measured impedance is less than the setting impedance, then a fault exists on the line in between the relay and the setting or reach point. In the case of DC systems, as line inductance is proportional to the length of the line, a similar protection strategy can be developed based on the line inductance. A fault is detected when the calculated loop inductance is less than the reach point inductance. With the knowledge of inductance per unit length, a decrease in the calculated inductance will effectively "*shorten*" the fault distance.

Thus,

If ….. $L_f < L_{set}$, detect fault;

else… relay remain stable

L_f is the measured inductance to the fault and is expressed as

$$L_f = L_T{}' - (Ls + L_{arm}) \qquad ((4\text{-}19)$$

L_{set} = setting inductance

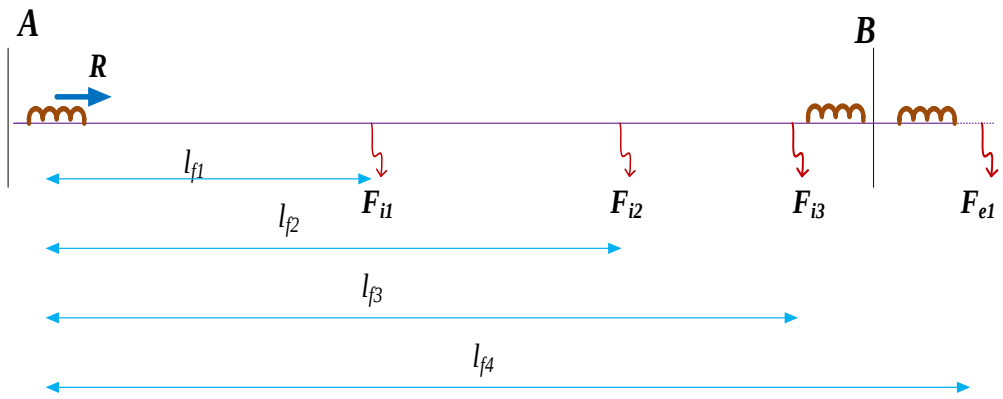


Fig. 4-17 *Section of a transmission line showing distance protection strategy based on fault loop inductance*

As shown in Figure 4.17, F_{i1}, F_{i2} and F_{i3} are internal faults whilst F_{e1} is an external fault with respect to relay *R*. The fault distances for l_{f1}, l_{f2} and l_{f3} are proportional to their respective inductances (L_{i1}, L_{i2} and L_{i3} respectively). Since inductance is proportional to the line length, a fault occurring at say, F_{e1} would result in an "increased" line length and therefore will not meet the condition for fault detection. However, any fault occurring along the line section *AB* would meet the condition for internal fault. Therefore assuming uniform line length and neglecting measurement errors in the first instance, a setting distance of l_{f4} would provide discrimination between internal and external fault. However for real life applications, such as for long distance cables, the effect of the cable capacitance would result in oscillations in the fault current profile, hence may impact on the accuracy. Further studies were carried out regarding this and findings are presented in Chapter 5.

4.4 Fault Characterisation in HVDC Systems Based on full scale MMC HVDC grid.

In order to fully characterise the faults in HVDC grids, simulations were carried out considering a full scale MMC-HVDC system shown in Figure 4.18. The test model

consists of a 4 terminal Modular Multi-level Converter (MMC) based DC grid made available in PSCAD/EMTDC software as per CIGRE 4-terminal test model [101]. However, some adjustments were made to the model to reflect the scenarios under consideration. As shown, the network consists of 4 cable sections and four MMC based on *half-bridge* submodule arrangements. As shown, *MMC1*, *MMC2* and *MMC3* are connected to an AC source whilst *MMC 4* is connected to a fixed load. All converters are of symmetrical monopole configuration. Details of the converter and AC parameters including the load parameters are given in Table 4.6. The cables are frequency dependent and distributed parameter models and as such, the wave effects including attenuation, losses and distortion have been accounted for. All cable sections have a length of 200km. Air cored inductors of *1mH* were placed at the DC cable ends to represent the inductive effects of HVDC breakers or fault current limiters. These inductors also help limit the rate of rise of current during short circuits. As will be seen later, these inductors helps to provide attenuation for the high frequency transient resulting from an external fault. The cable configuration is shown in Figure 4.19 and details of the parameters given in Table 4.7. The actual PSCAD model is shown in Appendix A4.1

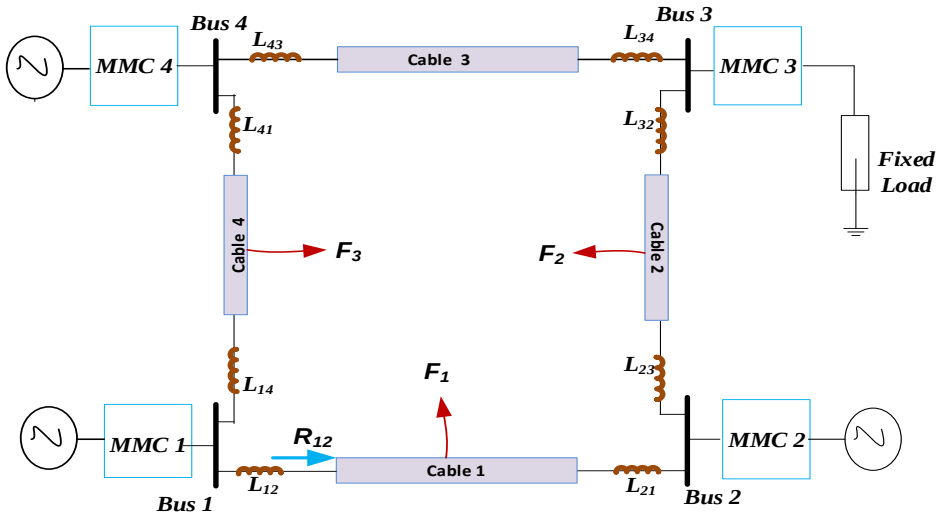


Fig. 4-18 *Four terminal HVDC grids showing internal and external fault* [101]

Table 4-6 Converter and AC side Parameters [101]

Item	Ratings
Rated Power of Converter	800MVA
Rated DC Voltage of Converter	400kV
Converter arm inductance	29mH
Cell DC Capacitor	10000μF
Nominal Frequency	50Hz
Transformer nominal voltage $_{(L\text{-}L)\ RMS}$	380kV
Nominal voltage at VSC side $_{(L\text{-}L)\ RMS}$	220kV
Leakage reactance of transformer	0.18pu
Rated real power per phase of Load	33MW
Rated reactive power per phase of Load	0.0MW
Rated load voltage$_{(L\text{-}G)\ RMS}$	83.72kV

In all scenarios shown, the fault was applied 2sec after the start of the simulation; and all measurements were taken at the positive pole terminal of the DC cable. The reference relay under consideration is relay R_{12}. For the purpose of this analysis, two types of faults shall be defined: *forward and reverse directional faults*

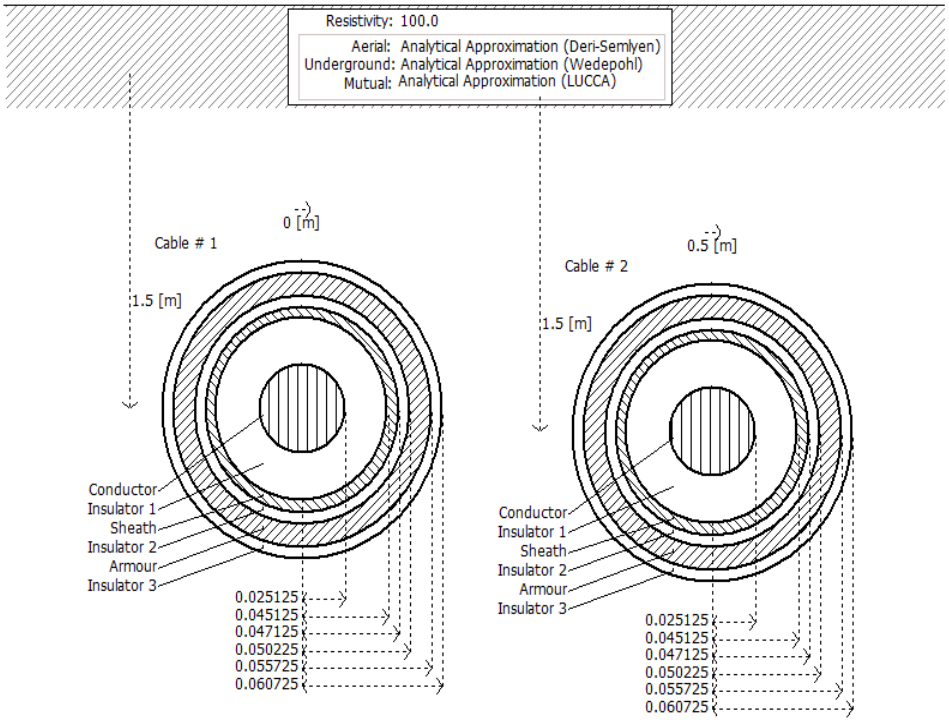


Fig. 4-19 Cable *configuration of the HVDC grid shown in Figure 4.1*[101]

Table 4-7 Conductor and Insulation Parameters [101]

Item	*Ratings*
Resistivity of core conductor	2.2×10^{-8} Ωm
Resistivity of 1st conducting layer (sheath)	27.4×10^{-8} Ωm
Resistivity of 2nd conducting layer	18.15×10^{-8} Ωm
Outer radius of core conductor	2.51×10^{-2} m
Thickness of 1st conducting layer	2×10^{-3} m
Thickness of 2nd conducting layer	5.5×10^{-3} m
Thickness of 1st insulation layer	2×10^{-2} m
Thickness of 2nd insulation layer	3.1×10^{-3} m
Thickness of 3rd insulation layer	5×10^{-3} m
Relative permittivity of all insulation layer	2.3
All relative permeability	1
Ground resistivity	100 Ωm
Length of Cable	200km

4.4.1 Forward and reverse faults

Considering Figure 4.18 and with respect to relay R_{12}, faults F_1, F_2 are regarded as forward directional fault (FDF) whilst F_3, is regarded as reverse directional fault (RDF). Also considering cable section 2 and with respect to relay R_{12}, F_1 is an internal fault and F_2 and F_3 are external faults. Therefore F_1 is a forward internal fault (FIF), F_2 is a forward external fault (FEF). The goal is to operate the relay for all internal faults and remain stable for external faults.

The cable parameters per unit length (inductance, capacitance and resistance) were also determined. Thus

The Cable inductance, *L and capacitance C,* was calculated, thus

$$L = \frac{\mu_0 \mu_r}{2\pi} \log \frac{D}{d} \ \ Henry; \ \ C = \frac{2\pi \varepsilon_0 \varepsilon_r}{\log \frac{D}{d}} \ \ Farad$$

D = the diameter of the outer conducting layer (=0.045mm)

d = diameter of inner conductor (=0.025mm)

μ_0 = permeability of free space ($= 4\pi \times 10^{-7}$ H/m)

μ_r = relative permeability = 1.

ε_0 = permittivity of free space ($= 8.845 \times 10^{-12}$ F/m)

ε_r = relative permittivity = 2.3

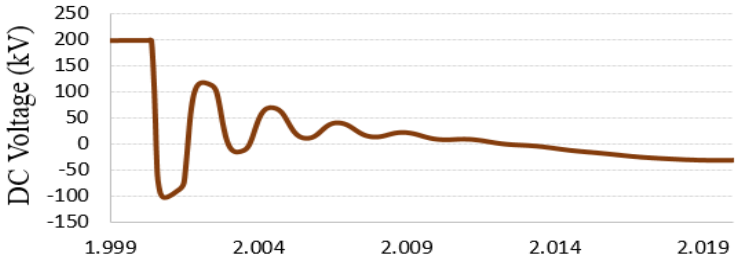
$$\therefore L = \frac{\mu_0}{2\pi}\log\frac{D}{d} = \frac{4\pi\times10^{-7}}{2\pi}\times\log\left[\frac{0.045mm}{0.025mm}\right] = 9.89\times10^{-8}H$$

$$C = \frac{2\pi\times8.845\times10^{-12}}{\log\frac{0.045}{0.025}}\times2.3 = 2.18\times10^{-10}\ F$$

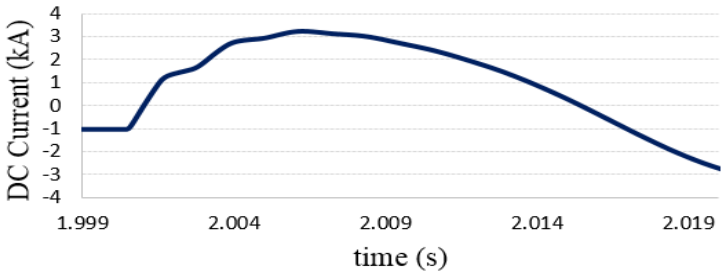
The characteristic impedance of the cable was calculated, thus

$$Z = \sqrt{\frac{L}{C}} = \sqrt{\frac{9.89\times10^{-8}}{2.18\times10^{-10}}} = 22\ \Omega$$

Figures 4.20 shows the plots of the voltage and current for a *P-G* fault occurring at F_1. As shown, under steady state, the DC voltages and currents remain stable at approximately *200kV* and *-1.03kA* respectively.



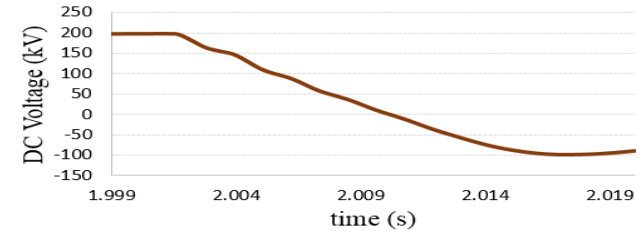
***(a)** DC Voltage*



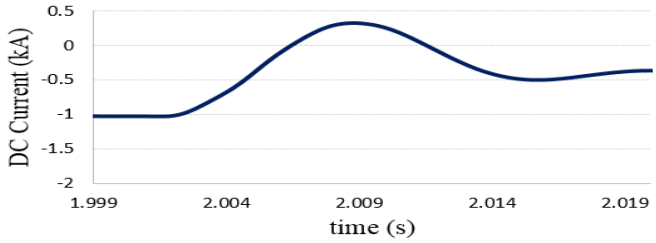
***(b)** DC current*

Fig. 4-20 Measured DC voltages and current at R_{12} considering fault F_1 (P-G fault)

However, following the application of the fault, the DC voltages collapse suddenly whilst the current increases. The negative value of the current indicates that MMC1 was inverting during the pre-fault steady state, hence exporting power into the AC system. The same scenario holds for fault F_2 (Figure 4.21) but with a significant decrease in the magnitude of the voltages and current. This is because fault F_2 is further away from relay R_{12} than F_1. Generally, the further away a fault is from the measurement terminal, the more the fault generated transient components are damped. This is also largely due to the attenuation in the current and voltage resulting from the conditions at the boundary such as the DC inductors (L_{21} and L_{23}). These characteristics provide discrimination between internal and external faults. However, whether or not this is sufficient enough for fault identification and discrimination is explored later in this section.



(a) DC Voltage

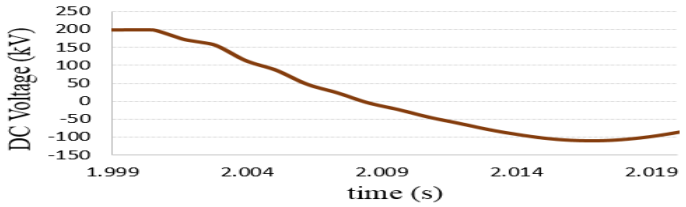


(b) DC current

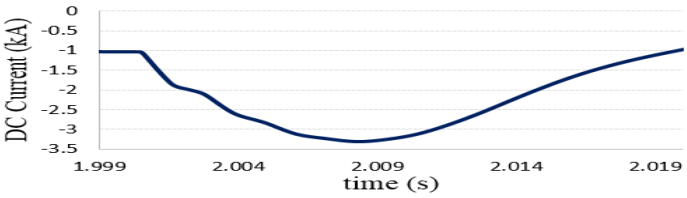
Fig. 4-21 *Measured DC voltage and current at R_{12} considering F_2 (P-G fault)*

Considering fault F_3 shown in Figures 4.22, the same scenario holds in terms of the magnitude as in Figure 4.21 due to the attenuation provided by inductors L_{12} and L_{14} respectively. However, in this case, the current flows in the reverse direction with respect

to the reference direction of current in R_{12} since *F3* is a reverse directional fault (RDF) with respect to R_{12}.

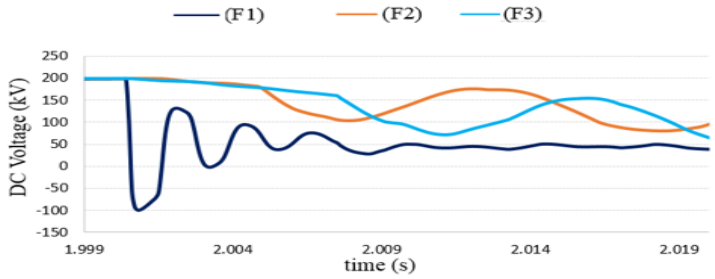


(a) DC voltage

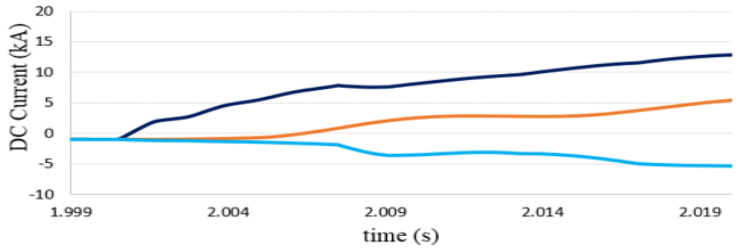


(b) DC current

Fig. 4-22 *Measured DC voltage and current at R_{12} considering F_3 (P-G fault)*



(a) DC voltage



(b) DC current

Fig. 4-23 *Measured DC voltage and current at R_{12} considering F_1, F_2 and F_3 (P-P fault)*

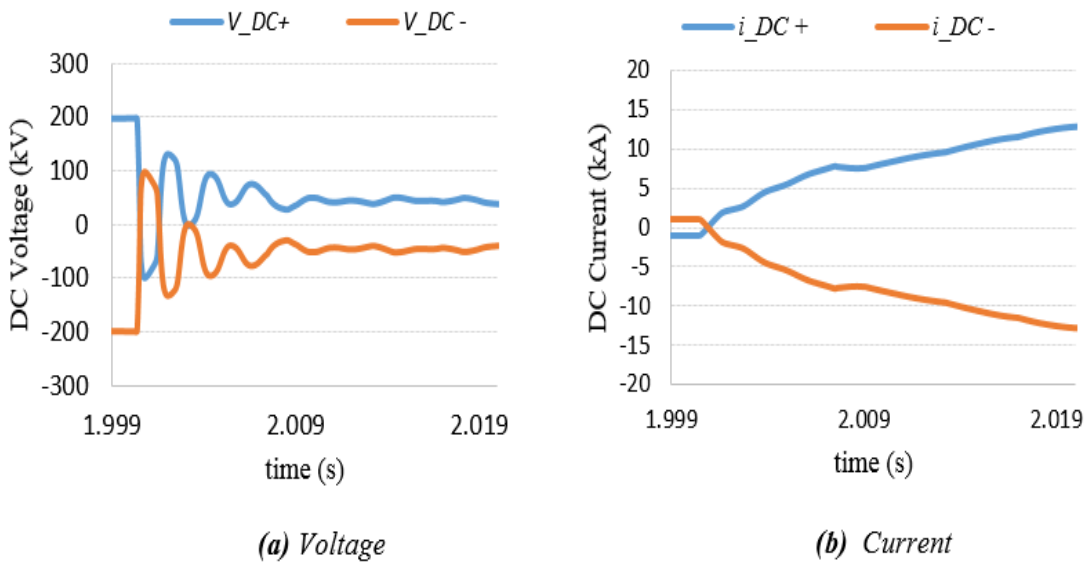
The same scenario holds for *P-P* faults shown in Figure 4.23 but with a significnt increate in the magniudes of the voltages and current compared to those of *P-G* faults. Generally, the ground resistance as well as the earthing configurations plays a significant role in the actual magnitude of the voltage and current following a *P-G* faults. Therefore for the same fault distance, the magnitude of the voltage and current resulting from *P-P* faults

are larger compared to *P-G* faults. The impact of earthing arrangements and configuration on the operation of MMC-HVDC have been researched in [102].

4.4.2 Discriminative characteristics between Pole-Pole (P-P) Versus Pole-Ground (P-G) Faults

In order to investigate the characteristic differences between the voltage and current footprints following a *P-P* or a *P-G* faults, the voltages and current signals recoded at the relay terminal for both the positive pole and negative pole terminals considering fault F_1 of Figure 4.18 were measured and recorded. However, the fault was assumed to occur at the positive pole terminal. All faults were also assumed to occur at 2s from the start of the simulation and with a fault resistance of 0.01Ω. The plots of voltages and currents recorded at the relay terminals are shown in Figures 4.24 and 4.25 respectively. Recall that the converter configuration is of symmetrical monopole arrangements.

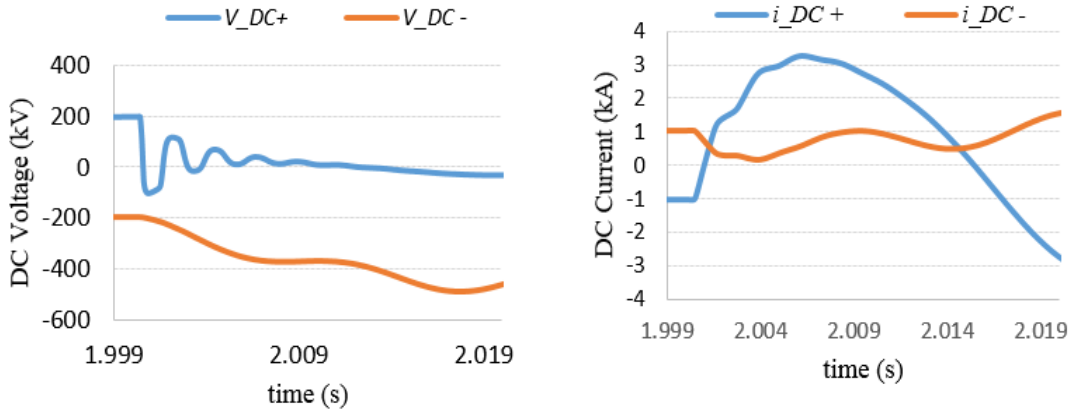
As shown in Figure 4.24, a *P-P* fault in a symmetrical monopole HVDC system results in a high magnitude of fault currents which is driven by the converter. Both the positive and negative pole voltages collapse suddenly following the application of a fault as shown. If the converter does not have the blocking capability as is the case of full bridge MMC, the fault current will rise to a value determined by the AC side reactance (transformer leakage reactance) or any other reactance within the circuit [19].



(a) Voltage *(b) Current*

Fig. 4-24 *Positive and Negative pole voltages and current for a pole-pole (P-P) fault*

A *P-G* fault results in a significant shift in the healthy pole voltage, ideally up to 2*pu*; whilst the faulty pole voltage collapses suddenly. The contribution from the AC side is small apart from the current flowing through the earthing resistor. However, the converter will experience a sudden high transient current owing to the discharge of the energy stored in the transmission system.



(a) Voltage *(b) Current*

Fig. 4-25 *Positive and Negative pole voltages and currents for a pole-ground (P-G) fault*

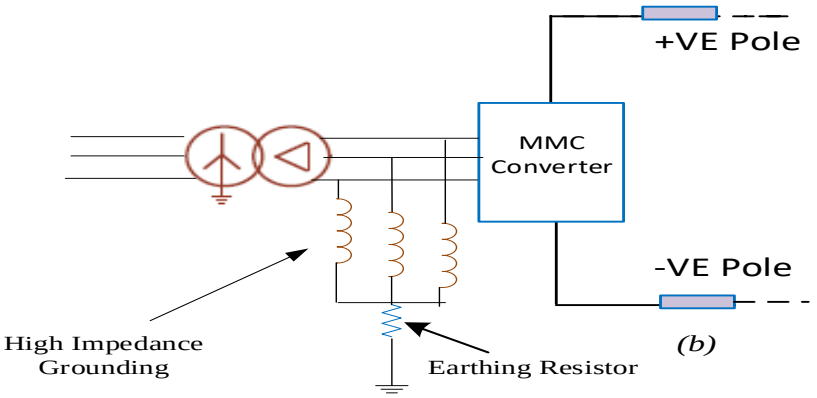


Fig. 4-26 *Symmetrical monopole configuration showing earthing configuration on AC side*

The excess voltage on the healthy cable can result in excessive stress on the DC cables if the fault is not cleared during the first few milliseconds following fault inception. However, it is envisaged in this study that the fault current would be cleared during the first *1ms*. If the fault is permanent as in the case of cable, the faulty cable must be isolated and the excessive voltage stored in the cable should be discharged by using a chopper or a Dynamic Breaking Resistor (DBR) [103]. However, if the fault is temporary in the case of overhead transmission lines (OTL), the arc will be dissipated once the lightning strikes disappear.

The key characteristic differences between the P-P fault and P-G faults are summarised in Table 4.8. Details of the short circuit current footprints and the associated over voltages in MMC based HVDC systems following a fault on underground cables and OTL are also well researched by reference[19], [104].

Table 4-8 *characteristics differences between a pole-to-pole (P-P) and pole-to-ground (P-G) fault*

Fault Type	***Pole-to-ground (P-G)***	***Pole-to-pole (P-P)***
V_{DC}+ (Faulty pole)	Collapse suddenly (Ideally to zero)	Collapse suddenly (Ideally to zero)
V_{DC}- (Healthy Pole)	Increases (Ideally to 2pu)	Collapses (Ideally to zero)

(Note: Fault occurring on the positive pole)

4.4.3 Effect of fault distance

Studies were also carried out to investigate the effect of fault distance on the current and voltage profile during a short circuit. For the sake of simplicity, only the scenarios for P-G faults are considered. All measurements were taken at the positive pole terminal and with a fault resistance of 0.01Ω. For this purpose, fault F1 on cable section 1 of Figure 4.16, and was varied as 50km, 100km, 150km, 200km, 400km. As shown in Figure 4.27, the magnitude of the fault current and voltage following the occurrence of the fault varies with fault distance. However, the magnitude for P-P faults for the same scenario is larger than for a P-G faults.

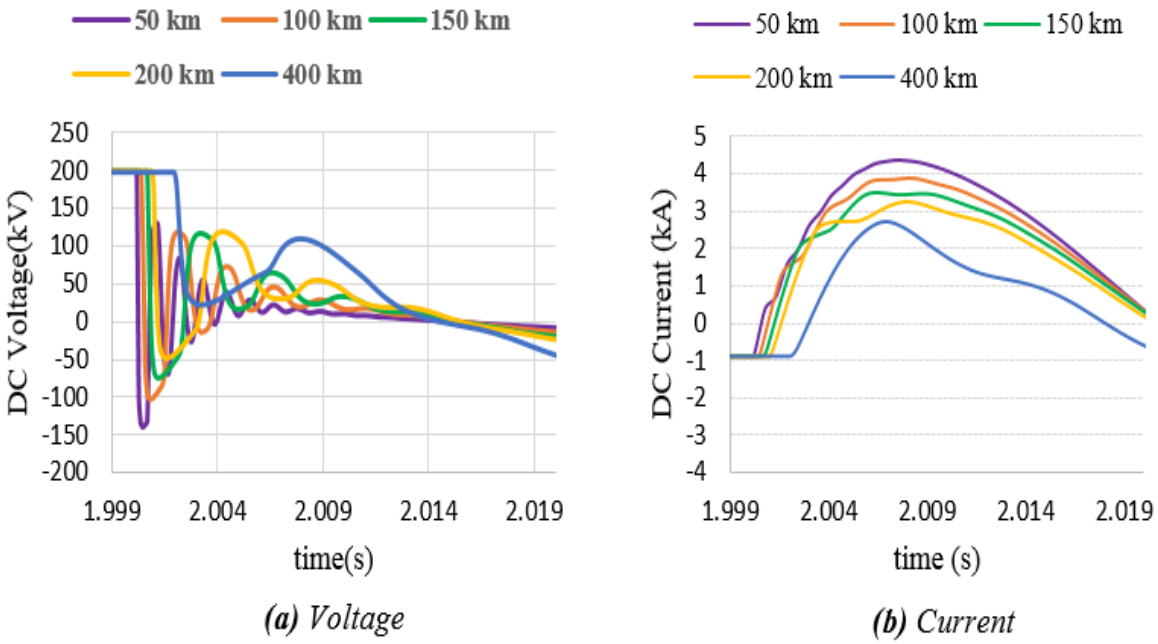


Fig. 4-27 *Effect of fault distance on current and voltage profile following a DC short circuit*

4.4.4 Effect of fault resistance

The effect of fault resistance (or R_f) on the voltage and current following the occurrence of fault was also investigated by simulations. For this purpose, the fault distance was kept fixed at 200km and the fault resistances were varied (50Ω, 100Ω, 200Ω, 300Ω, 400Ω and 500Ω). This was done to simulate various fault scenarios that could occur on the grid.

For the purpose of simplicity, the *P-G* faults are considered and all measurements were taken from the positive pole terminal.

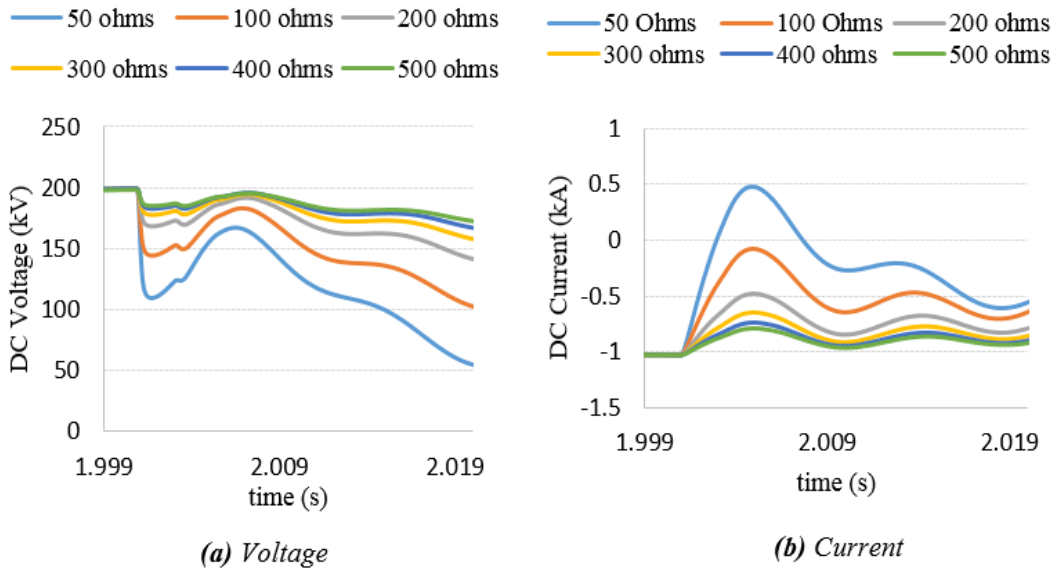


Fig. 4-28 *Effect of fault resistance on voltage and current profile during DC short Circuit*

The results presented in Figure 4.28 also revealed that the magnitude and the rate of rise of the current and voltage following the occurrence of fault depends largely on the fault resistance. The higher the fault resistance, the more the waveforms are damped thus reducing their magnitudes

4.4.5 Effect of DC inductor

Recall that the goal of this research is to provide discrimination between internal and external faults. In particular between a long-distance remote internal faults with high fault resistance and a low resistance external fault as shown in Figure 4.29. Generally, the network is representative of cable section 1 of Figure 4.18 with F_{int} representing a fault at the remote end of the cable section 1 while F_{ext} represent a fault occurring along cable section 2 close to the busbar B.

Fig. 4-29 *Two terminal transmission network showing critical condition for a local relay*

For this purpose, high fault resistances (R_f = 300Ω and 500Ω) were considered for the internal faults whilst a low resistance (R_f = 0.01Ω) was considered for external fault. These conditions are assumed to be the worst-case scenario for relay R_{12} in this study. The plots of the voltage and current considering F_{int} and F_{ext} for varying inductor sizes at the boundaries are presented in Figures 4.30. As shown, the magnitudes of the voltages and current is largely dependent on the inductors at the boundaries. The larger the size of the inductor, the more the voltages and currents are damped.

As shown in Figure 4.31 and 4.32, for an external fault with low fault resistance (F_{ext} = 0.01Ω), the magnitude of the current exceeds that for high resistance internal fault (F_{int} = 500Ω). Generally, this scenario represents the most critical conditions for relay R_{12} and may lead to faulty discrimination of any relay utilising the magnitude and/or rate of rise for fault identification and discrimination

However, by increasing the size of the DC inductor from *0.1H* to *0.5H*, the magnitudes of the voltages and currents were significantly reduced. This is a good strategy for discriminating between an internal and external fault, but not without incurring cost. Therefore, a compromise must be reached considering the cost of the DC inductor and the security and reliability of power delivery.

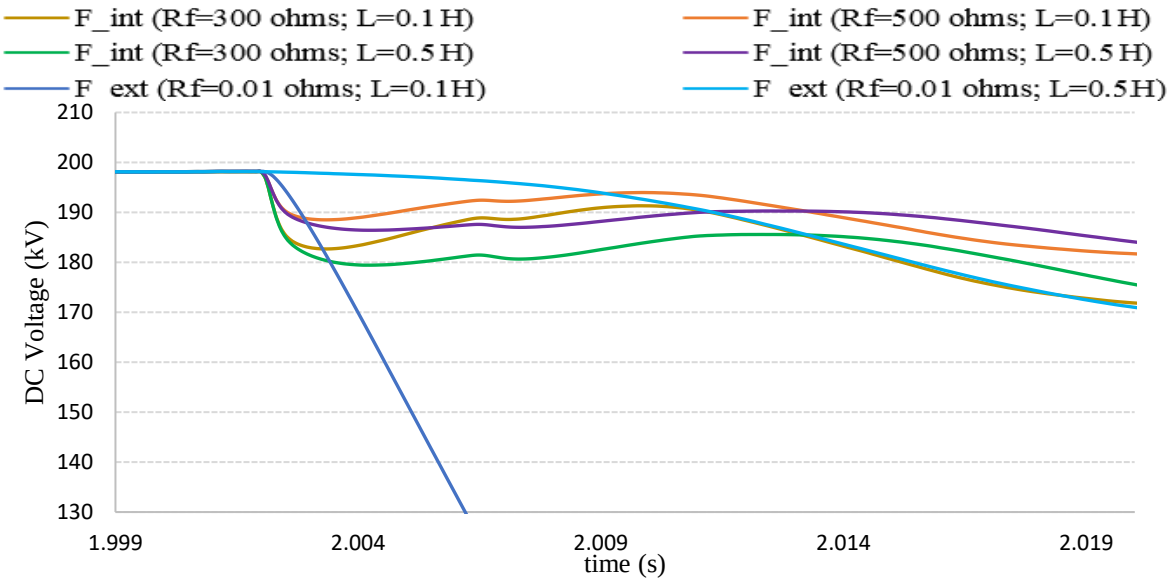


Fig. 4-30 *(Sensitivity analysis) Effect of DC inductor on the voltage profile*

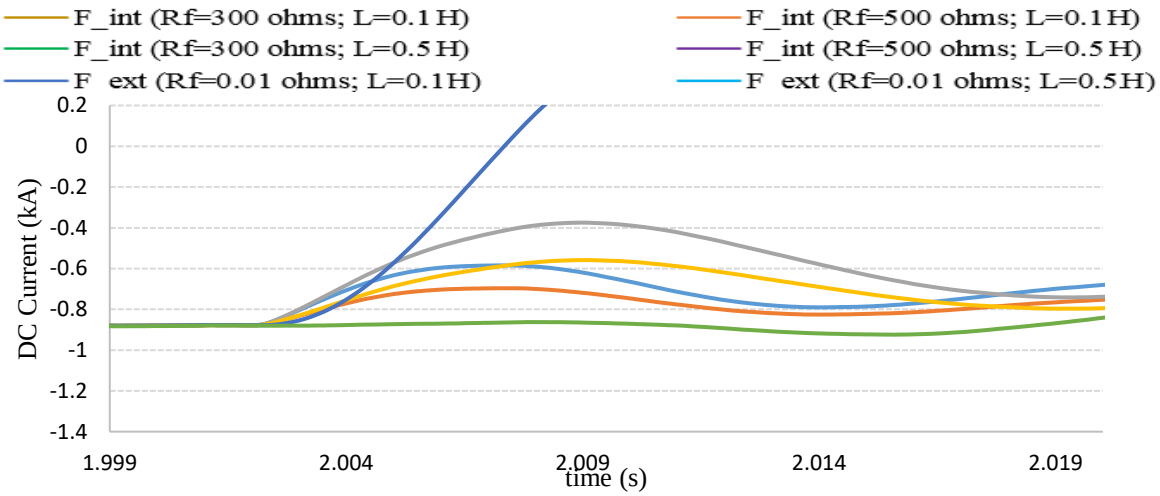


Fig. 4-31 *(Sensitivity analysis) Effect of DC inductor on the fault current profile*

4.5 Summary

The study carried out in this chapter has given an insight into the behaviour (magnitude and rate of rise) of fault current for different fault scenarios in DC systems based on lumped parameter modelling and full-scale simulations. Some existing techniques developed for DC traction systems were studied and compared, and the results presented

shows consistency in the different methods in estimating the initial magnitude and rate of rise of the fault current.

However, in order to fully account for the distributed nature of the line parameters as well as travelling wave effects, simulations were carried out based on full scale MMC HVDC grid. For this purpose, both the P-P and P-G faults were investigated. However, in the case of the *P-G* fault, the earthing arrangements as well as the ground resistance must be accounted for. However, this is not a major issue in this study as the goal is to detect a fault of the DC link, irrespective of whether or not it is a *P-P* or *P-G* fault. Once a DC side fault is declared, the decision of whether or not it is a *P-P* or *P-G* can be made based Table 4.8. The simulation results presented show that the current and voltage profile following fault inception is largely dependent on the following factors.

i. *The nature and type of fault (such as pole –to-pole or pole to ground faults.)* : For the same fault distance and fault resistance, the magnitude and rate of change of the current or voltage following fault inception is larger for a pole-to-pole than for a pole –to-ground.

ii. *The fault Resistance*: The magnitude of the current and voltage following fault inception decreases with increasing fault resistance.

iii. *The fault Distance*: The magnitude of the current and voltage following fault inception decreases with increasing fault distance. Generally, the impact of the fault resistance on the fault current or voltage is more than the impact posed by the fault distance.

iv. *The nature of discontinuity*: An inductive termination would in general produce a reduced magnitude and rate of change of current or voltage than a termination

without a DC inductor. Furthermore, the magnitude as well as the rate of change of current and voltage following fault inception also varies with the size of inductors. Large inductors would in general produce larger magnitudes and rate of change of current/voltage and vice versa. However, the choice for this will be a matter of compromise since increasing the size of the inductor will increase cost. Generally, the discriminative criteria between a forward internal fault and a forward external fault is largely due to the busbar and DC inductors.

In general, the use of traditional overcurrent or an under-voltage protection technique could result in spurious relay trips, noting that the magnitude of the fault current or voltage for a low resistance external faults may exceed those for high resistance remote internal fault. This is an undesirable condition for the relay and hence must be avoided.

Based on this, possible protection algorithms for DC grid was investigated, priority was given to the di/dt and travelling wave based protection philosophies. Furthermore, as the *di/dt* is a widely established in DC traction system and this research shall investigate its suitability for the protection of DC lines and for application to DC grid in the first instance. Furthermore, the majority of proposed DC grid protection techniques documented in literature are either based on *di/dt*, *dv/dt* or a hybrid of both techniques.

Considering that speed is also a major requirement in the protection of DC grid, the travelling wave based protection technique was also studied. Generally, travelling wave based protection techniques is fast in operation and still very much at the research stage, thus opening the door for further research. However, studies carried out on the *di/dt* based protection technique as well as the contribution made is presented in Chapter five in the first instance.

Chapter 5

5 Investigation of *di/dt* based protection Algorithm

5.1 Introduction

In this chapter, studies carried out on the di/dt based protection technique for the protection of HVDC lines are presented. Firstly, the di/dt techniques used in DC traction systems was critically evaluated to ascertain its suitability for application to DC grid. Following this, the di/dt techniques proposed for DC grid available in literature are also extensively studied using full scale MMC based HVDC systems. The chapter concludes by highlighting the advantages and short comings of the di/dt based protection technique for application to the DC grid.

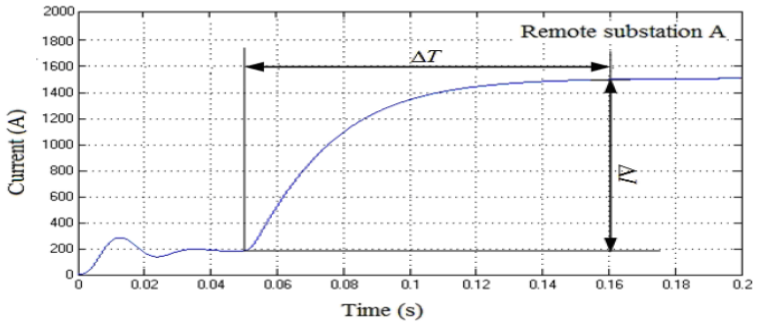
5.2 The di/dt based Protection Technique

As explained in Chapter 3, the current derivative or di/dt based DC line protection technique uses the initial rate of rise (or di/dt) of the fault current to determine whether a fault has occurred on a line under consideration. As previously stated, this technique is widely used in DC traction system as it measures the initial increase in the current thus detecting the presence of a fault before it reaches damaging levels. The technique relies on the initial gradient of the fault induced component of the current to detect the

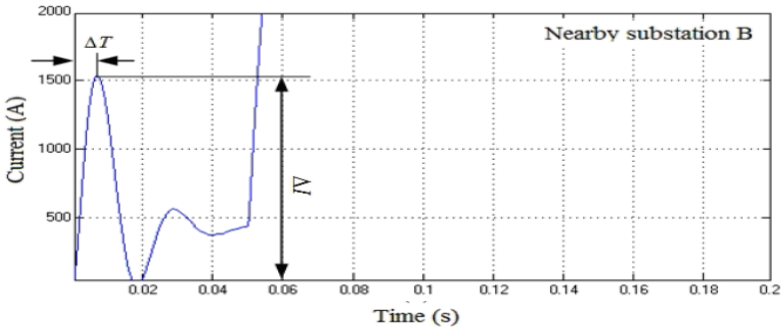
occurrence of a DC line fault. A relay utilising this principle is set to operate when the calculated initial di/dt following fault inception exceeds a pre-determined threshold or setting. The *di/dt* is usually computed by sampling, Thus

$$\left|\frac{di}{dt}\right| = \frac{i_{n+1} - i_n}{\Delta t} \qquad (5\text{-}1)$$

For DC traction applications, the *di/dt* technique is usually incorporated with a *ΔI* element to improve the sensitivity [50], [51]. However, a detailed knowledge of the system configuration is needed to ensure correct settings so that the device does not trip for the most severe train starting current. The major disadvantage of this technique is that, depending on the train location, the magnitude of the di*/dt* and *ΔI* of the fault current can be smaller than that of the train starting current (Figure 5.1) which can result in faulty relay discrimination as well as spurious trips. This phenomenon is largely due to the high series impedance of the traction supply.



(a) *Remote short circuit current of feeder line at substation A*



(b) *Train starting current of feeder line at substation B*

Fig. 5-1 *Fault current versus train starting current of feeder line* [51]

To address this challenge, a time setting or delay element ΔT, is incorporated in the *di/dt* element thus resulting in a $di/dt + \Delta T$ technique. As shown in Figure 5.2, the protection system has two settings, *di/dt* and ΔT, thus allowing the protection to trip the circuit breaker if the high *di/dt* persists beyond the time setting; otherwise the relay will remain stable. This criterion provides discrimination between long distance remote fault and the train starting current.

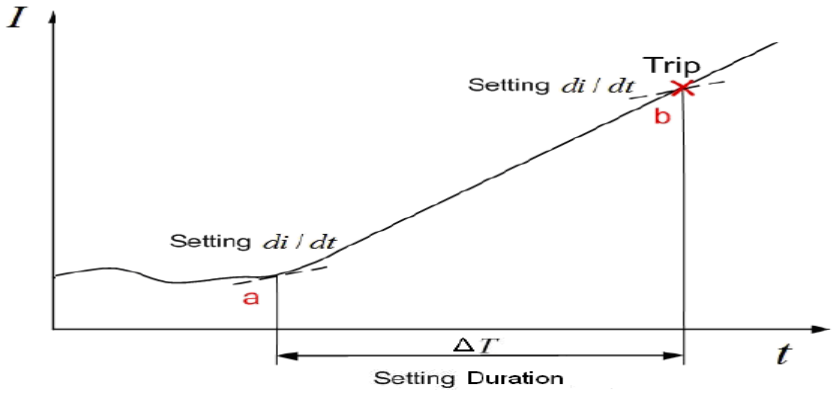


Fig. 5-2 *dt/dt protection principle for DC traction system*[51]

An improvement to this principle is the addition of a ΔI element, resulting in a *current differential* supervised by a *di/dt* element (Figure 5.3). In this case, the *di/dt* is made to trigger the ΔI element once a transient is detected. After a pre-determined time setting, ΔT, ΔI is measured. A trip signal is initiated when ΔI exceeds the pre-demined settings. For higher sensitivity, *di/dt* the element can be reduced thus offering higher sensitivity for remote faults whilst ΔT setting can be reduced to give sensitive for close-up faults, this is however a matter of compromise.

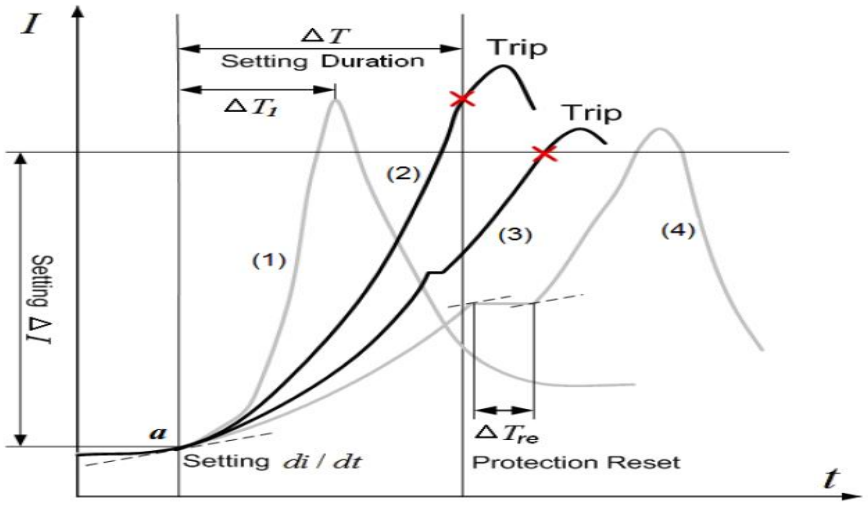


Fig. 5-3 *Current incremental-supervised current derivative protection for DC traction system* [51]

The details of the different plots (1,2,3 and 4) shown in Figure 5.3 are given hereunder.

1) As shown, the *di/dt* and ΔI are higher than the trip setting level. However, no trip signal will be sent since the time setting ΔT_i is less than the setting duration (ΔT).

2) In this scenario, ΔI is higher than the trip setting level and the duration is also longer than the setting duration (ΔT), hence a trip will be initiated.

3) The *di/dt* momentarily reduces to below the setting level. However, this duration is less than the time setting of protection reset element (ΔT_{re}), therefore, a trip is initiated.

4) In this scenario, *di/dt* reduces to below the setting level with a duration of more than the setting of protection reset element (ΔT_{re}), therefore the protection will not operate.

5.3 Determination of the initial *di/dt*

To investigate the *di/dt* protection method for its suitability for the protection of DC grid, a simple DC network supplying an arbitrary load of 100Ω was modelled in PSCAD based on Bergeron Line model, and neglecting the frequency dependency of the distributed line

parameter in the first instance (Figure 5.4). The transmission line parameters for this model are given in Table 5.2. The parameters used for this study was taken from reference[37]. For the sake of simplicity and clarity, the source parameter was assumed to be ideal. The plots obtained following the application of a dead circuit (R_f=*0*) fault at *0.3secs* from the start of the simulation on the DC line for varying fault distances; 25km, 50km and 100km are shown in Figure 5.5. The calculated initial di/dt based on Equation 5.1 is presented in Table 5.2.

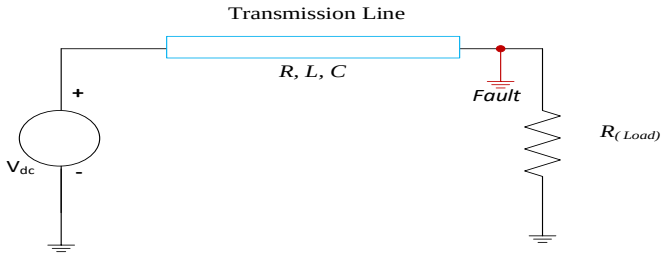


Fig. 5-4 *Basic Transmission Line Based on Bergeron Model*

Table 5-1 Parameter of Figure 5.1 [37]

DC Voltage , V_{dc}	*400kV*
Line resistance, R	*10mΩ/km*
Line Inductance, L	*0.6mH/km*
Line Capacitance, C	*0.15μF/km*

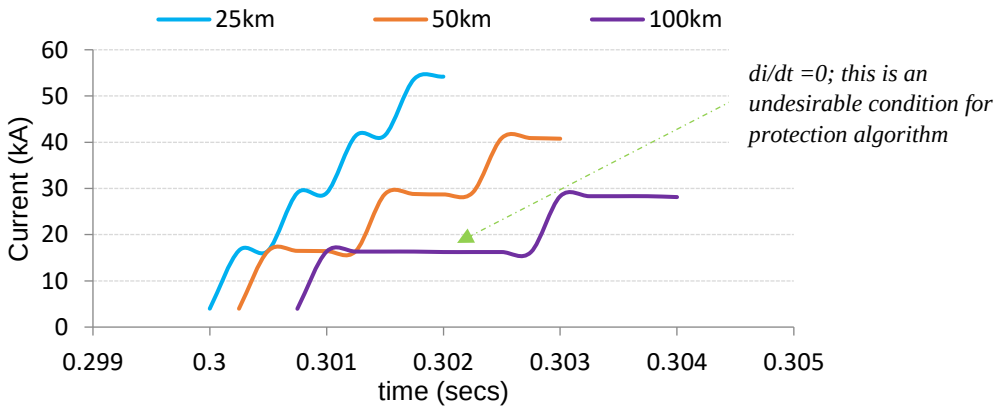


Fig. 5-5 *Fault Current profile Based on Figure 5.1*

Table 5-2 *Calculated Initial di/dt of Figure 5.2*

Fault Distance (km)	Initial *di/dt* (kA/ms)
25	50.30
50	50.00
100	49.50

As shown, the initial *di/dt* is dependent on the distance to the fault. This phenomenon is consistent with travelling wave propagation theory. However as shown, there are oscillations in the fault current profile which are largely due to the travelling wave effect. In practice, these effects can result in errors in extracting samples for calculating the actual di/dt. This is because the measurement time window may coincide with the time when the fault current profile attains its local maximum/minimum; or when it appears to have a zero di/dt for a considerable length of time. Also, depending on the measurement period or fault distance, the calculated di/dt may vary between positive and negative values. This is independent of the actual direction of the fault. Therefore, the time during which samples are taken still plays a major role in the directional discrimination provided by the relay.

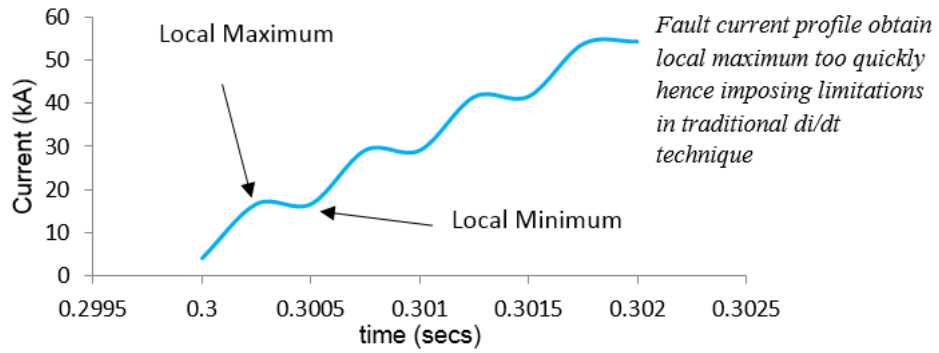


Fig. 5-6 *Fault Current profile showing local maximum and local minimum*

The above limitations impose in the use of the traditional *di/dt* techniques for DC traction systems as explained in section 5.2, where the *di/dt* can persist for a long time (hence

requiring a long-time window) before a decision is reached. The same scenario also holds for full scale simulations results shown in Figure 5.7; considering a *P-G* fault occurring along cable section 1 of Figure 4.18 (also shown in Figure 4.29).

Also shown in Figure 5.7, the initial di/dt for low resistance external fault approaches that for a long-distance remote internal fault which could result in faulty relay discrimination. Now, as the actual di/dt can either be positive for a forward directional or negative for reverse directional faults nuisance trips may result. This is because any measurement taken during the time soon after the local maximum/minimum in the fault current profile will indicate a reverse or forward directional fault respectively.

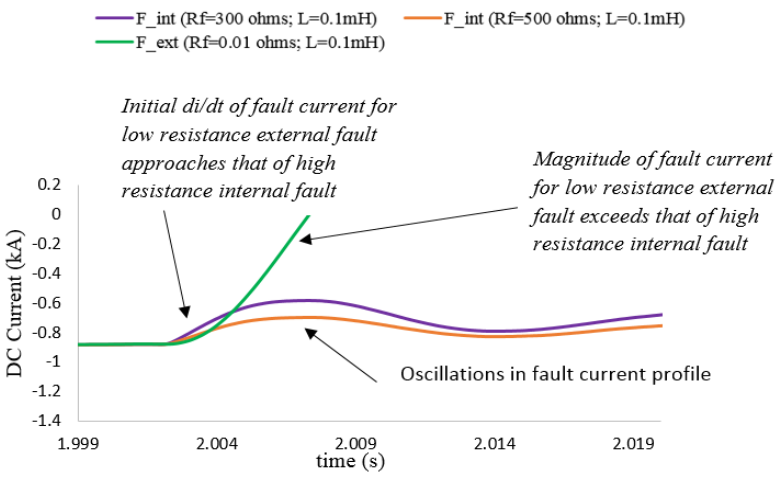


Fig. 5-7 *Comparison of initial di/dt for high resistance internal fault and low resistance external fault*

The converse is the case for measurements taken just before the local maximum/minimum. However, this may not be the case. To account for the oscillations, attempt was also made to determine the trend in *di/dt* (or average *di/dt*). The resulting findings are as presented below.

5.3.1 Determination of the average *di/dt*

As the name implies, the average rate of rise of the fault current following fault inception is used as a basis for fault detection. The principle is explained hereunder[105]

When a short circuit suddenly occurs in a transmission line, a wave of $-V_{DC}$ travels towards the source, reducing the line voltage to zero. This wave is accompanied by a current wave of magnitude V_{DC}/Z_C . Conventionally, it is assumed that the positive direction of current flow is from the source towards the transmission line. Generally, boundary conditions demand that at the short circuit, the voltage is zero and at the source, it is V_{dc}

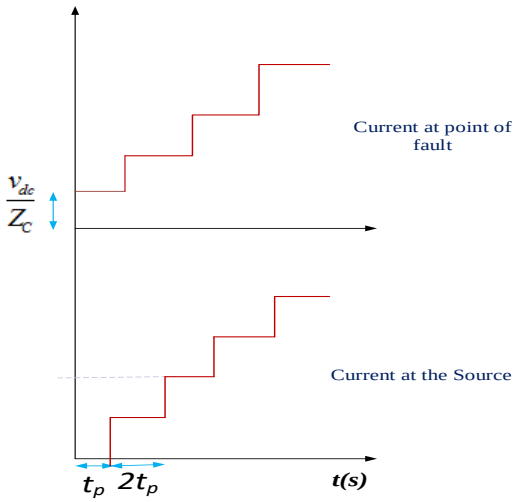


Fig. 5-8 *Ideal (Theoretical) Profile of Fault current during short circuit*

Now, when this wave reaches the source, a new wave of $+V_{DC}$ is reflected, and its associated current is V_{DC}/Z_C . This reflected wave from the source again reaches the short circuit and the cycle continues. The time taken for the wave to travel from the fault to the source is referred to as the transit time, t_p. This implies that the effect of the short circuit is not felt at the source until after t_p seconds. Based on this back and forth movement of the wave, the current at both the source and short circuit increases in discrete steps of $2V_{DC}/Z_C$ every 2τ seconds (Figure 5.8). Generally, this is an ideal case as the effect of

the resistive and dielectric losses will provide damping, and the current will attain steady state. The average rate of rise of the current is therefore given as

$$\left|\frac{di}{dt}\right|_{(Average)} = \frac{2V_{dc}}{2Z_C\, t_p} \qquad (5\text{-}2)$$

$$Z_C = \sqrt{L_c/C_c}\ ; \qquad t_p = l_f/c\ ; \qquad c = 1/\sqrt{L_c C_c}$$

Further simplification results in Equation 5.3. Thus

$$\left|\frac{di}{dt}\right|_{(Average)} = \frac{v_{dc}}{l_f\ L} \qquad (5\text{-}3)$$

Now, since the trend in the di/dt (or average di/dt) is proportional to the inductance, with the knowledge of inductance per unit length, a distance protection philosophy utilising the trend in di/dt could also be developed.

From Equation 5.3; and we can therefore write,

$$|di_{DC}/dt|_{\ trend} = \frac{V_{DC}}{l_f\ L_c} \qquad (5\text{-}4)$$

$$l_f = \frac{V_{DC}}{|di_{DC}/dt|_{\ trend}} \times \frac{1}{L_c} \qquad (5\text{-}5)$$

Where l_f and L_c represents their usual meaning.

As shown in Figure 5.9, this technique may only be suitable for estimating the distance to the fault, but may not be suitable for fault detection due to the time constraint. Another disadvantage is the time requirement as per DC grid protection requirements. This is because the technique requires at least the first two local maximum /minimum to estimate the fault distance, this is particularly the case for long distance faults. Furthermore, the frequency dependency of the distributed line parameters must also be accounted for to

guarantee accuracy. In practice, the trend in di/dt could be calculated by Least Squares Estimation, LSE and usually expressed as [106].

$$\left|\frac{di}{dt}\right|_{LSE} = \frac{n\sum_{i=1}^{i=n} i_{dc_i} t_i - \sum_{i=1}^{i=n} i_{dc_i} \sum_{i=1}^{i=n} t_i}{n\sum_{i=1}^{i=n} {t_i}^2 - \left(\sum_{i=1}^{i=n} t_i\right)^2} \quad kA/s \quad (5\text{-}6)$$

Based on Figure 5.8, the average di/dt was calculated by the use of Equation (5.6)

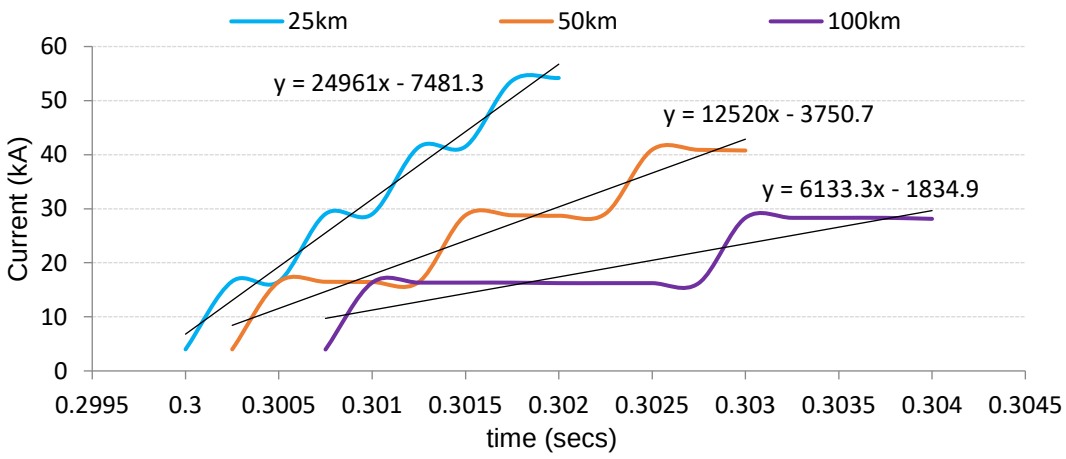


Fig. 5-9 *Plots of Figure 5.5 showing trend in di/dt (or averagedi/dt)*

Table 5-3 *Calculated Average di/dt*

Fault Distance (km)	di/dt (Equation 5.4)	di/dt (Equation 5.6)
25	26.70	25.0
50	13.30	12.5
100	0.67	0.62

The results presented shows consistency in using the Equations (5.3) and (5.6) to compute the average *di/dt*. However, for DC grid applications, this technique would require a long time window before a relay decision is made, hence incurring time delay. The full-scale simulation results presented in Figure 5.10 also shows the limitations in the use of the average di/dt in adopting this technique for the protection of DC grid. As shown in Figure 5.10, the technique will require a long-time window thereby posing limitations for DC grid protection considering the time needed to detect and clear the fault. For example, the plot of a 300Ω remote internal fault will require a minimum of *30ms* to obtain the require samples, as shown by the dotted line. This is not acceptable in the context of DC grid protection.

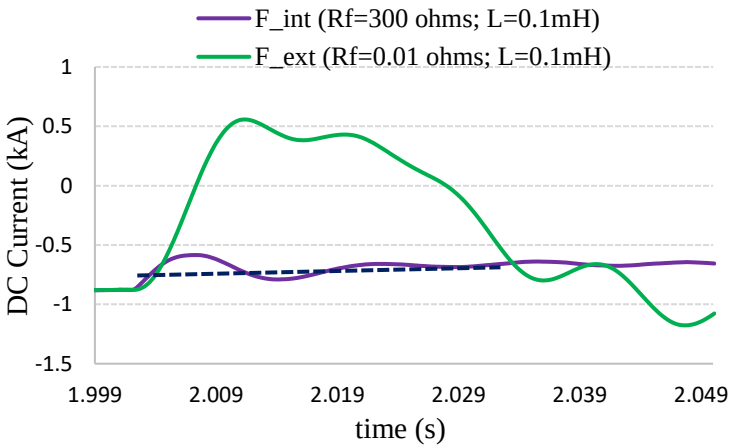


Fig. 5-10 *Full Scale simulation results showing average di/dt measurements*

5.4 Summary

The di/dt protection technique has been extensively investigated and evaluated with a view to ascertaining its suitability for the protection of DC grid. The studies carried out shows the suitability of the di/dt technique in low voltage applications such as the DC traction systems. However, in some cases, where a fault occurs at a considerable distance from the substation where the protection devices are situated, the fault current may be significantly less than the relay settings and as such would not operate the breaker. This

is particularly the case for P-G faults where fault resistance adds to the reduction in the magnitude of the fault current.

Some of the limitations of di/dt technique was found by using the travelling wave analysis to determine the fault current profile which demonstrated the oscillatory nature of the fault current. This can lead to errors in estimating the actual di/dt since the profile may attain its local maximum/minimum before or during the time window set for the measurement. Furthermore, depending on the direction of the fault with respect to a local relay, the actual di/dt could be positive (for a forward directional fault) or negative (for a reverse directional fault). However, the calculated di/dt may give erroneous results since any measurement taken during the time soon after the local maximum or local minimum in the fault current profile will indicate a reverse or forward directional fault respectively; irrespective of the actual fault direction. This however, may not be the true case.

Although the di/dt based protection technique is widely used in DC traction where the effect of distributed line capacitance can be neglected. However, from the study carried out the di/dt based protection technique suffers some disadvantages (such as oscillations, requirement of long time window and poor sensitivity) and as such, extreme care should be taken when deploying it for the protection of DC lines, in particular for the protection of MT-HVDC system; otherwise nuisance trips may result. Based on the study carried out on *di/dt* protection technique, the following conclusions were reached.

- The sensitivity of *di/dt* protection techniques decreases with fault distance and fault resistance
- The initial *di/dt* for external faults could be larger than that for high resistance remote internal faults.

- Long time window is also a major constraint in adopting the *di/dt* protection technique for DC grid Protection
- The sensitivity of the *di/dt* is also largely affected by oscillations resulting from travelling wave effect; particularly for short distance faults.
- For DC grid protection, the sensitivity of *di/dt* technique must be improved to ensure absolute selectivity thereby avoiding nuisance relay trips

Based on the studies carried out on *di/dt*, it was concluded that the technique is not adequate for the protection of DC grid. In the light of this, the TWBP philosophy was extensively investigated and evaluated. The findings revealed that the TWBP technique is a reliable method for the protection of DC grid. The findings are the findings, including the theoretical analysis and simulation results are presented in Chapter six and seven respectively.

Chapter 6

6 Theoretical analysis of the proposed travelling wave based protection (TWBP) principle

6.1 Introduction

This chapter presents the proposed travelling wave based protection (TWBP) principle for application to DC grids. The chapter starts with a brief overview of the fundamentals of TWBP principles including derived expressions for the voltage and current travelling wave. Thereafter, the proposed TWBP principle is presented.

6.2 Basic Concepts

In general, the occurrence of a fault on a transmission line will result in a voltage collapse and initiate a forward and backward travelling wave [62][63]. These waves propagate in both directions of the line or cable and travels back and forth between the relay terminals and the fault until the post fault steady state conditions are reached and the wave damps out.

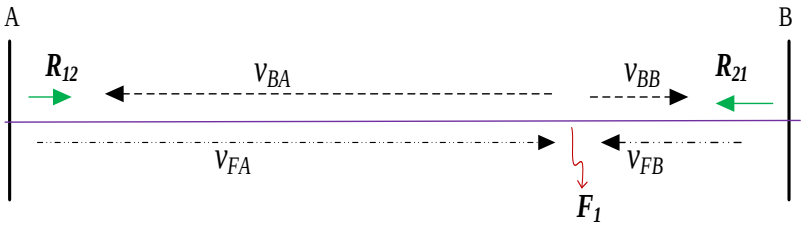


Fig. 6-1 *Travelling Wave on Transmission Lines*

Consider a two-terminal network shown in Figure 6.1, where terminals A and B represents busbar *A* and *B* respectively. As shown, the assumed positive (or reference) direction of current flow is the current flowing from the busbar terminals (*A* and *B* as shown) into the line. A forward voltage travelling wave (FVTW) with respect to the local relay, R_1 and R_2, is therefore defined as a wave travelling in the same direction as the assumed positive direction of current flow in the relay. The opposite wave is defined as the backward voltage travelling wave (BVTW). Generally, the FVTW and BVTW are also accompanied by a forward and reverse current travelling wave respectively (not shown in the diagram). From Figure 6.1, the following can be defined.

v_{FA} = *Forward voltage travelling wave (FVTW) with respect to relay* R_{12} *located at terminal A*

v_{BA}=*Backward voltage travelling wave (BVTW) with respect to relay* R_{12} *located at terminal A*

v_{FB} = *Forward voltage travelling wave (FVTW) with respect to relay* R_{21} *located at terminal B*

v_{BB}=*Backward voltage travelling wave (BVTW) with respect to relay* R_{21} *located at terminal B*

When a fault say F_1 occurs on the transmission line, two BVTWs (with respect to the relay terminal) v_{BA} and v_{BB} will flow in both directions from the point of fault towards the relay terminals as shown. At the relay terminals, two new FVTWs, v_{FA} and v_{FB} are reflected back towards the fault point. The waves continue to travel back and forth until they are damped and the post fault steady state conditions are reached. The transient fault signals recorded at the relay terminals will therefore contain multiple and successive reflections (Figure 6.2). The arrival times, t_{iA} and t_{iB} (i=1,2) are proportional to the distance travelled by the wave.

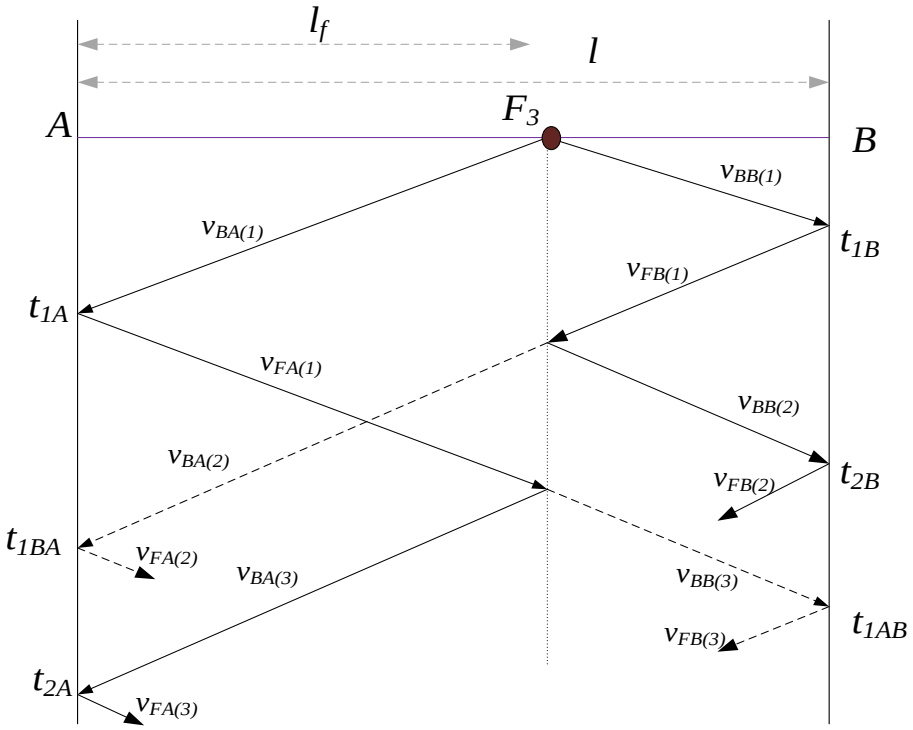


Fig. 6-2 *Bewley Lattice diagram showing wave propagation*

l_f, l represents the cable length and distance to fault respectively; c ($=\sqrt{LC}$) is the velocity of propagation of the wave whilst L and C are the per unit length of the inductance and capacitance respectively. The fault distance can be determined using the *single-ended* or *double-ended* fault location method. The single ended method makes use of information from the arrival times of the waves at only one terminal (terminal A as

shown). The double ended method relies on information from both terminals (terminals A and B as shown). The double ended method calculate the fault location by observing the relative arrival times of the fault generated transients at each terminal using GPS. The differences between the surge arrival times at the two terminals can be measured and used to calculate the fault location.

Considering Figure 6.2, the following equations can be written

$$c \times t_{1A} = l_f \tag{6-1}$$

$$c \times t_{2A} = 3\, l_f \tag{6-2}$$

$$c \times t_{1B} = L - l_f \tag{6-3}$$

Combining Equations (6.1) and (6.2);

$$l_f = \frac{(t_{2A} - t_{1A}) \times c}{2} \tag{6-4}$$

Combining Equations (6.1) and (6.3),

$$l_f = \frac{l - (t_{1B} - t_{1A}) \times c}{2} \tag{6-5}$$

Equations (6.4) and (6.5) are referred to as *single-ended* and *double-ended* methods respectively for fault location based on travelling wave principles and have been proposed and widely used for fault identification and location on major transmission and distribution lines including two-terminal HVDC systems [80]-[86]. A proposal regarding the application of travelling wave protection for DC grids utilising the reflections of the waves has also been reported in [87][88].

However, a major issue when adopted for the protection of DC grid is that it relies on reflections (or multiple reflections) between the fault and the relay terminals thereby incurring delay. This is because the wave propagation delay time may be longer than the time required to detect and clear the fault. Therefore time limitation is a major to be considered when deploying travelling wave based protection principle for application to DC grids. Therefore, new TWBP techniques are required for application to DC grids, hence the objective of this research.

6.3 Expressions for voltage and current travelling waves

Generally regardless of time and space variations, and considering Figure 6.1, the voltages and currents along a line in the transient mode caused by a switching, fault or any other change of state processes are related by the expression [62][63].

$$v_{FA}(x,t) = +Z_C\, i_{FA}(x,t) \tag{6-6}$$

$$v_{RA}(x,t) = -Z_C\, i_{BA}(x,t) \tag{6-7}$$

x represents the position of the wave at any instant in time. Z_C ($=\sqrt{L/C}$) is the lossless characteristic impedance of the line and which is assumed to be constant in this study. Generally, at a very high frequency the resistance is increased due to skin effects. Skin effect results from non-uniform distribution of current density in the conductor which

also slightly decrease the inductance. However, the effect of the skin effect on the inductance is assumed to be constant in this study and therefore Z_c will also constant.

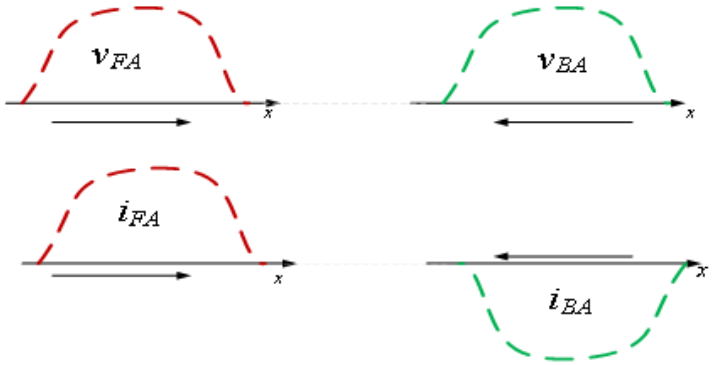


Fig. 6-3 *Polarity of Forward and Reverse Travelling Wave*

As illustrated in Figure 6.3, the current associated with the FVTW is directly proportional to its voltage, with its constant of proportionality being $+1/Z_c$ whereas the current associated with the BVTW is also directly proportional to its voltage, but with its constant of proportionality being $-1/Z_c$. Therefore, the FVTW and the associated current waves are of the same sign whereas the BVTW and the associated current are of opposite sign.

The general solution (as given by Equations 6.8 and 6.9) for the voltage and current along a line and as a function of time is therefore the superposition of two waves, whose amplitude is determined by the initial conditions and boundary conditions of the line. The velocity of propagation of the wave, $c\ (=1/\sqrt{LC})$ is independent of the magnitude of the steady state current or voltage; but determined only by the value of the line constants (the inductance and capacitance respectively). In real transmission lines, the velocity would vary due to the frequency dependency of the distributed line parameters. However, for simplicity. in this study, it is assumed that all points in the voltage and current envelope

(Figure 6.3) travels at a constant velocity without distortion (or change in shape). However, in practice these waves will be distorted and continuously attenuated.

$$v_T(x,t) = v_{FA}(x,t) + v_{BA}(x,t) \tag{6-8}$$

$$i_T(x,t) = \frac{1}{Z_C}\left(v_{FA}(x,t) - v_{BA}(x,t)\right) \tag{6-9}$$

$v_T,(x,t)$, $i_T(x,t)$ are the total voltages and currents on the line at any instant and point on the transmission medium assuming that a step voltage is applied to a de-energised network.

They represent the actual superimposed quantities (Δv_{DC} and Δi_{DC}) respectively) following the occurrence of faults on a transmission line. Thus

$$\Delta v_{DC} = v_{DC(inst)} - v_{DC(ss)} \tag{6-10}$$

$$\Delta i_{DC} = i_{DC(inst)} - i_{DC(ss)} \tag{6-11}$$

Where the subscripts, "*inst"* and "*ss"* represents the instantaneous and steady state components respectively

Equations (6.8) and (6.6) can be expressed as

$$\Delta v_{DC}(x,t) = v_{FA}(x,t) + v_{BA}(x,t) \tag{6-12}$$

$$\Delta i_{DC}(x,t) = \frac{1}{Z_C}\left(v_{FA}(x,t) - v_{BA}(x,t)\right) \tag{6-13}$$

From Equations (6.7) and (6.8) and noting that *x=0* at the relaying point, the following equations can therefore be written.

$$v_{FA}(t) = \frac{\Delta v_{DC}(t) + Z_C \Delta i_{DC}(t)}{2} \quad (6\text{-}14)$$

$$v_{BA}(t) = \frac{\Delta v_{DC}(t) - Z_C \Delta i_{DC}(t)}{2} \quad (6\text{-}15)$$

Equations (6.14) and (6.115) gives the general expression for calculating the FVTW and BVTW following the application of fault on a line or any other transient conditions. Under steady state conditions, Δv_{DC} and Δi_{DC} are ideally zero and no travelling wave is present. Generally, the voltage travelling wave is associated with the current travelling wave. In the same way, an expression for the forward and backward current travelling wave can also be written. Thus

$$i_{FA}(t) = \frac{\Delta v_{dc} + Z_c \Delta i_{dc}}{2Z_c} \quad (6\text{-}16)$$

$$i_{BA}(t) = -\frac{\Delta v_{dc} - Z_c \Delta i_{dc}}{2Z_c} \quad (6\text{-}17)$$

The negative sign associated with Equation (6.17) is accordance with Equation (6.2) as illustrated in Figure 6.2. Equations (6.14) - (6.17) have also been widely proposed for the protection of major transmission lines including two-terminal HVDC systems.

6.4 Power developed by a travelling wave

In general, as the waves propagate along the transmission medium, power is developed due to the energy content of the waves. Generally, for equal voltages the power is far higher in cables than in overhead transmission lines (OTL) owing to the smaller surge impedance of cables. The large power accompanying these travelling waves can produce strong effects in high voltage transmission systems, however these effects are limited by

the high frequency of propagation since the duration of the effects at any point will be short.

Now, since the power, P is the product of current and voltage, the power developed by the superimposed components of voltage and current, P_{DC} at the relay terminal following the occurrence of a fault is the product of the superimposed voltage and current (Δv_{DC} and Δi_{DC} respectively).

Therefore, from Equations (6.8) and (6.9), the following can be written.

$$P_{DC}(t) = (v_{FA}(t) + v_{BA}(t)) \times \frac{1}{Z_C} \ (v_{FA}(t) - v_{BA}(t)) \tag{6-18}$$

$$P_{DC}(t) = \frac{1}{Z_C} \ (v_{FA}(t)^2 - v_{BA}(t)^2) \tag{6-19}$$

The power contained in the forward and reverse travelling wave P_{FW} and P_{RW} can therefore be expressed as

$$P_{FW}(t) = \frac{1}{Z_C} v_{FA}(t)^2 \tag{6-20}$$

$$P_{BW}(t) = -\frac{1}{Z_C} v_{BA}(t)^2 \tag{6-21}$$

The power contained in the forward travelling wave has positive polarity whereas that contained in the reverse travelling wave has negative polarity. From Equations (6.14) and (6.15), Equations (6.20) and (6.21) can be re-written.

Thus

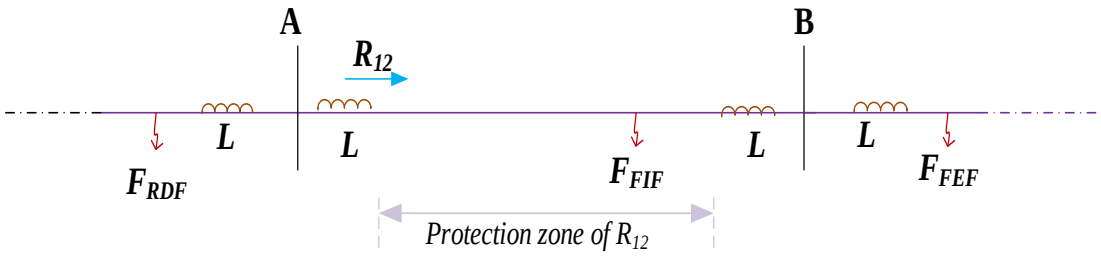
$$P_{FW}(t) = \frac{1}{4Z_C}(\Delta v_{DC}(t)^2 + 2\,\Delta v_{DC}(t)\;\Delta i_{DC}(t)\,Z_C + \Delta i_{DC}(t)^2\,Z_C{}^2) \quad (6\text{-}22)$$

$$P_{BW}(t) = -\frac{1}{4Z_C}(\Delta v_{DC}(t)^2 - 2\,\Delta v_{DC}(t)\;\Delta i_{DC}(t)\,Z_C + \Delta i_{DC}(t)^2\,Z_C{}^2) \quad (6\text{-}23)$$

Equations (6.22) and (6.23) represents the derived expression for the power developed by the forward and backward travelling wave following the occurrence of a fault and forms the basis for the protection principle proposed in this research.

6.5 Fault discriminative characteristics based on travelling wave power

Now consider the schematic diagram of a two-terminal transmission network shown in Figure 6.4



F_{FIF} : Forward Internal fault ; F_{FEF}: Forward External fault; F_{RDF}: Reverse Directional fault

Fig. 6-4 Two terminal transmission line showing internal and external faults

The inductors, *L* shown are representative of *di/dt* limiting inductors as per HVDC circuit breaker or fault current limiters (*FCL*). Recall from section 4.4 that F_{FIF} and F_{FEF} are forward fault with respect to relay R_{12} whereas F_{RDF} is a reverse fault. However, F_{FIF} is an internal fault and F_{FEF} and F_{RDF} are external faults. The goal is to operate the relay only for faults along its protection zone. The propagation of travelling waves along the transmission line (or cable) and across the boundaries based on the three fault scenarios is presented below.

6.5.1 Forward and reverse fault

Considering Figure 6.5, when the *BVTW* from fault F_{FIF} reaches the relay terminals (say terminal *A*), the first incident wave at the relay R_{12} is v_{BA}, which is reflected to produce v_{FA}. (Figure 6.5)

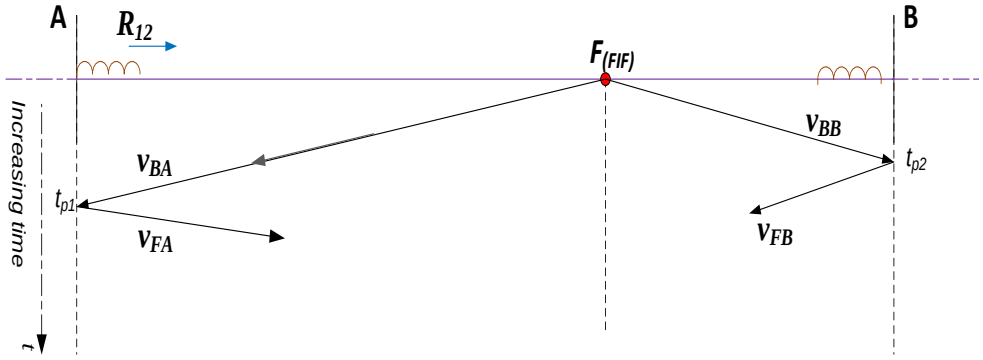


Fig. 6-5 *Travelling wave propagation based on forward internal fault (FIF)*

In practice, the reflected waves at a boundary has lower magnitude compared with the magnitude of the incident wave. Hence v_{FA} is less than v_{BA} for a specified short period of time following fault inception. Therefore,

$$v_{BA} > v_{FA}$$

or

$$\frac{v_{FA}}{v_{BA}} < 1 \qquad (6\text{-}24)$$

Therefore, from the derived power Equations given in Equation 6.17 and 6.18, the following can be written

$$\frac{|P_{FW}|}{|P_{BW}|} < 1 \qquad (6\text{-}25)$$

Now considering Figure 6.6, and with a fault $F_{(RDF)}$ (which is "*reverse"* with respect to relay R_{12}), the first wave seen by relay R_{12} is v_{FA}. This reflected wave is "*forward*" with

respect to relay R_{12}. A significant amount of time will therefore elapse before the arrival of v_{RA} at terminal *A* following a reflection at terminal B (Figure 6.6).

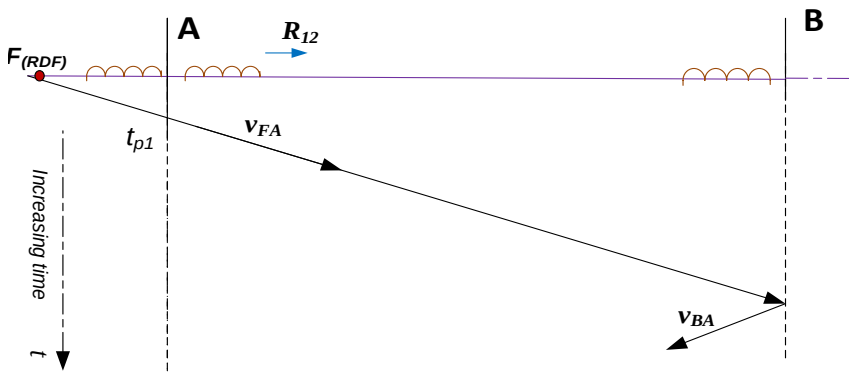


Fig. 6-6 *Travelling wave propagation based on reverse directional fault (RDF)*

Therefore for fault F_{RDF}, the magnitude of v_{FA} is greater that v_{BA} for a specified and brief period of time following fault inception, say $2t_p > t \geq t_p$ and we can write,

$$v_{FA} < v_{BA}$$

or

$$\frac{v_{FA}}{v_{BA}} > 1 \qquad (6\text{-}26)$$

Also from Equation 6.17 and 6.18, the following can also be written

$$\frac{|P_{FW}|}{|P_{BW}|} > 1 \qquad (6\text{-}27)$$

Equations (6.25) and (6.27) therefore provide the discriminative criteria between a forward directional and a reverse directional fault (or FDF and RDF) based on voltage travelling waves. The conditions are given in Table 6.1

Table 6-1 *Conditions for forward and reverse directional faults*

Condition for Fault	Fault with respect to a Local Relay
$\lvert P_{FW}\rvert / \lvert P_{BW}\rvert < 1$	Forward Directional Fault
$\lvert P_{FW}\rvert / \lvert P_{BW}\rvert > 1$	Reverse Directional Fault

6.5.2 Forward internal and forward external faults

In Figure 6.7, relay R_{12} sees a much attenuated *FVTW* and *BVTW*, due to the discontinuity or boundary at terminal B.

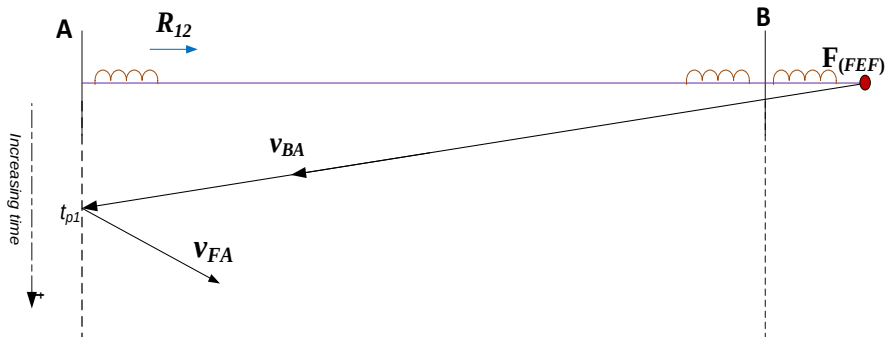


Fig. 6-7 *Travelling wave propagation based on forward external fault (FEF)*

This is largely due to the DC inductor located at each of the line ends, which provides attenuation to the high frequency components resulting from an external fault. However, the attenuation of a travelling wave due to *FIF* such as F_{FIF} of Figure 6.5, is much smaller. Therefore, for a *FIF* the magnitude of the FVTW and BVTW must be greater than that for a FEF during the same measurement period. The effect of fault resistance are explained in section 7.4. Assuming a setting of $v_{FA(set)}$ and $v_{BA(set)}$, then the following can be written.

For a FIF,

$$v_{FA} > v_{FA}\,(set) \qquad (6\text{-}28)$$

$$v_{BA} > v_{BA}(set) \qquad (6\text{-}29)$$

For a FEF,

$$v_{FA} < v_{FA}\,(set) \qquad (6\text{-}30)$$

$$v_{BA} < v_{BA}(set) \qquad (6\text{-}31)$$

From Equations 6.28 - 6.31, the following discriminative characteristics between a FIF and FEF can also be derived. Thus,

For a FIF,

$$P_{FW} > P_{FW}(set) \quad (6\text{-}32)$$

$$P_{BW} > P_{BW}(set) \quad (6\text{-}33)$$

For a FEF,

$$P_{FW} < P_{FW}(set) \quad (6\text{-}34)$$

$$P_{BW} < P_{BW}(set) \quad (6\text{-}35)$$

The derived general conditions for the declaration of an internal fault with respect to a local relay on a meshed HVDC grid utilising travelling wave power is summarised in Table 6.2. As shown, it comprises the *ratio criteria* and the *magnitude criteria*. Once the ratio criteria is satisfied indicating a *FDF*, either the magnitude of P_{FA} or P_{BA} for a preset time following the occurrence of fault gives the condition for a *FIF*.

Table 6-2 *General conditions for internal fault based on travelling wave power*

Condition	*Type*
$\frac{P_{FW}}{P_{BW}} < 1$	Ratio check
$P_{FW} > P_{FW}(set)$	Magnitude check 1
$P_{BW} > P_{BW}(set)$	Magnitude check 2

6.6 Energy of a travelling wave

In general, a travelling wave can be considered as a wave of energy propagating along a transmission line. In physical terms, the current and voltage travelling waves can be regarded as two aspects of the same wave of energy propagating along a transmission medium. Therefore, the energy components of the travelling wave was also extracted for fault identification, noting that the energy is proportional to the power developed by the travelling wave.

Generally, the energies in the forward and backward travelling waves can now be obtained by integrating the expressions for the power over time. Thus

$$E_{FW} = \int_{t_0}^{t_N} P_{FW}(t)dt \qquad (6\text{-}36)$$

$$E_{BW} = \int_{t_0}^{t_N} P_{BW}(t)dt \qquad (6\text{-}37)$$

E_{FW} and E_{BW} are the forward and backward travelling wave energy, *FTWE* and *BTWE* respectively.

The quantity, $t_N - t_0$ is the time interval when measurements are taken.

t_0 is the time of the occurrence of the fault.

In this thesis, E_{FW} and E_{BW} were obtained by the well-known Simpson's digital integral algorithm. Thus

$$E_{FW} = \frac{\Delta t}{3}\left(P_{FW_0} + 4P_{FW_1} + 2P_{FW_2} + 4P_{FW_3} + 2P_{FW_4} + \cdots + 2P_{FW_{N-1}} + 4P_{FW_{N-1}} + P_{FW_N}\right) \quad (6\text{-}38)$$

$$E_{BW} = \frac{\Delta t}{3}\left(P_{BW_0} + 4P_{BW_1} + 2P_{BW_2} + 4P_{BW_3} + 2P_{BW_4} + \cdots + 2P_{BW_{N-1}} + 4P_{BW_{N-1}} + P_{BW_N}\right) \quad (6\text{-}39)$$

Δt = compute step or step size and is expressed as

$$\Delta t = \frac{t_f - t_o}{N} \quad (6\text{-}40)$$

N=total number of sampling points.

6.6.1 Fault discriminative characteristices based on travelling wave energy

From Equations (6.25) – (6.27), the condition for an internal and external fault with respect to a local relay located on a line /cable section of the grid can also be established based on travelling wave energy; noting that the magnitude of the energy in the travelling waves is a function of the power developed by the travelling wave.

Thus, we can write,

For a FDF,

$$\frac{E_{FA}}{E_{BA}} < 1 \quad (6\text{-}41)$$

And for a RDF,

$$\frac{E_{FA}}{E_{BA}} > 1 \quad (6\text{-}42)$$

Therefore,

For a FIF,

$$E_{FA} > E_{FA}\,(set) \tag{6-43}$$

$$E_{BA} > E_{BA}(set) \tag{6-44}$$

For a FEF,

$$E_{FA} < E_{FA}\,(set) \tag{6-45}$$

$$E_{BA} < E_{BA}(set) \tag{6-46}$$

Table 6-3 *General conditions for internal fault based on travelling wave energy*

Condition	*Type*
$\frac{E_{FA}}{E_{BA}} < 1$	Ratio check
$E_{FA} > E_{FA}\,(set)$	Magnitude check 1
$E_{BA} > E_{BA}\,(set)$	Magnitude check 2

6.7 Summary

In this chapter, the theoretical analysis of the proposed TWBP principle for application to DC grid was presented. Firstly, an expression for the voltage and associated current travelling wave following the occurrence of faults were derived. Thereafter, an expression for the power as well as the energy contents of the forward and backward travelling waves were formulated. Based on the derived equations, the fault discriminative characteristics and criteria were established. These include the directional comparison criteria as well as the magnitude criteria. The directional comparison criteria provide discrimination between a forward directional and reverse directional fault whilst the magnitude comparison provide discrimination between a forward internal and forward external fault.

For a forward directional fault with respect to a local relay, the ratio between the forward and backward travelling wave power, or between the forward and backward travelling wave energy must be less than unity. However, this ratio is less than unity for a reverse directional fault. Furthermore, for a forward internal fault, the magnitude of the forward and backward travelling wave power, or the forward and backward travelling wave energy must exceed a predetermined settings otherwise, the fault is regarded as forward external fault.

The protection principles were implemented in MATLAB and the algorithms were validated on a full scale MMC-HVDC grid and the findings are reported in chapter 7

Chapter 7

7 Validation of the proposed travelling wave based protection technique by simulations

7.1 Introduction

This chapter validates the proposed TWBP technique for application to DC grids. The proposed technique utilises the "power" and "energy" of the forward and backward travelling wave following the occurrence of a fault to determine whether or not a fault is internal or external. All simulations were carried out in PSCAD and the data exported to a text file; and thereafter to MATLAB work space for post processing.

7.2 The test model

The test model used for the validation is shown in Figure 4.18, but has been reproduced in Figure 7.1 to reflect the scenario for this study. The cable are of frequency dependent model and as such the losses has been accounted for. As stated earlier, the inductors located at the ends of the cable sections are *di/dt* limiting inductor that help to limit the fault current during DC short circuits. However, as explained in section 6.4, these inductors also help to create the discriminative characteristics between an internal and

external fault. Generally, both relays located on the cable section are expected to operate autonomously following the detection of a DC short circuit. As shown in Figure 7.1, for a fault along cable section 1, R_{12} and R_{21} will operate; for faults along cable section 2, R_{23} and R_{32} will operate; for faults along cable section 3, R_{34} and R_{43} will operate; for faults along cable section 4, R_{14} and R_{41} will operate. The relay reference direction of current flow is from the busbar into the cable. This is independent of the direction of current flow in the converter. As previously stated, all MMCs are of half bridge submodules and as such HVDC breakers (not shown in the diagram) are assumed to be placed at both ends of each cable section. Each cable section has a length of 200km.

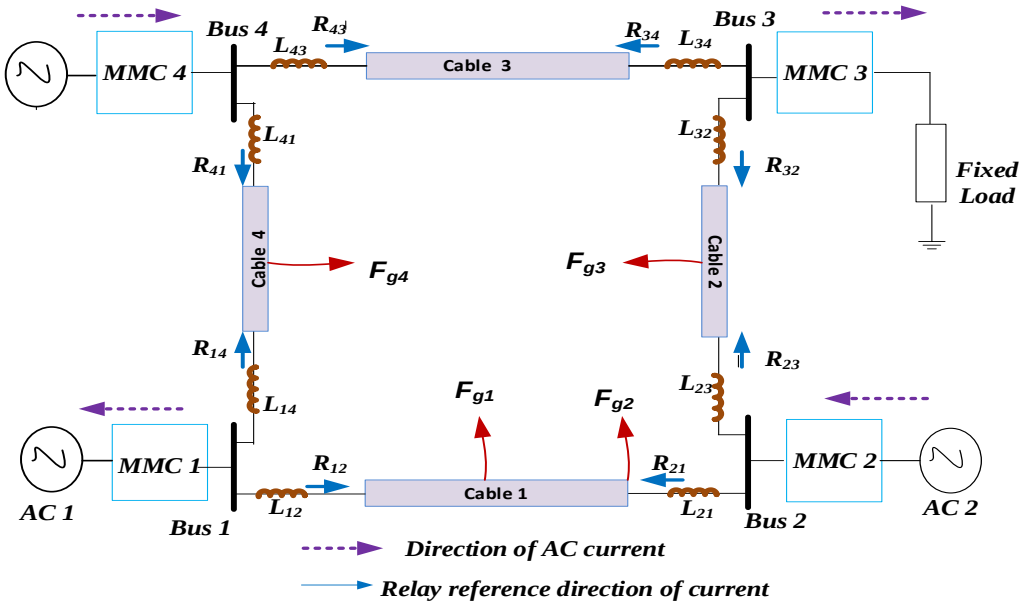


Fig. 7-1 *HVDC test model showing fault scenario for travelling wave*

As shown in Figure 7.2, the DC voltages and currents, v_{DC} and i_{DC} respectively at the respective relay terminals are sampled at a frequency of *96 kHz* as per IEC guidelines [7] to obtain the incremental quantities, Δv_{DC} and Δv_{DC} respectively. Thereafter the travelling wave power and energy were computed.

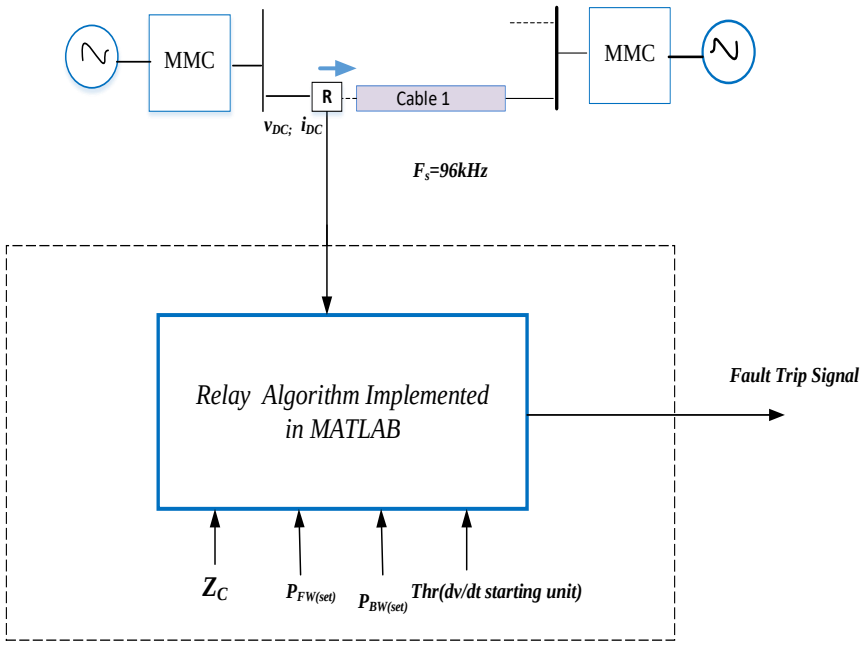


Fig. 7-2 *Section of the DC grid showing data acquisition for processing*

7.3 Proposed protection scheme

Firstly, the suitability of utilising the TWP was investigated. The block diagram for the protection scheme is shown in Figure 7.3.

In ***Unit "A",*** the instantaneous DC voltage and DC current, $v_{DC}[n]$ and $i_{DC}[n]$ respectively are sampled based on a three-point moving average filter to obtain the average DC voltages and current, $v_{DC(AV)}[n]$ and $i_{DC(AV)}[n]$ respectively. This was done to reduce the effect of the spikes resulting from the fault generated transient.

Thus

$$v_{DC(AV)}[n] = \frac{1}{3}\sum_{i=0}^{i=2} v_{DC}[i] \quad (7\text{-}1)$$

$$i_{DC(AV)}[n] = \frac{1}{3}\sum_{i=0}^{i=2} i_{DC}[i] \quad (7\text{-}2)$$

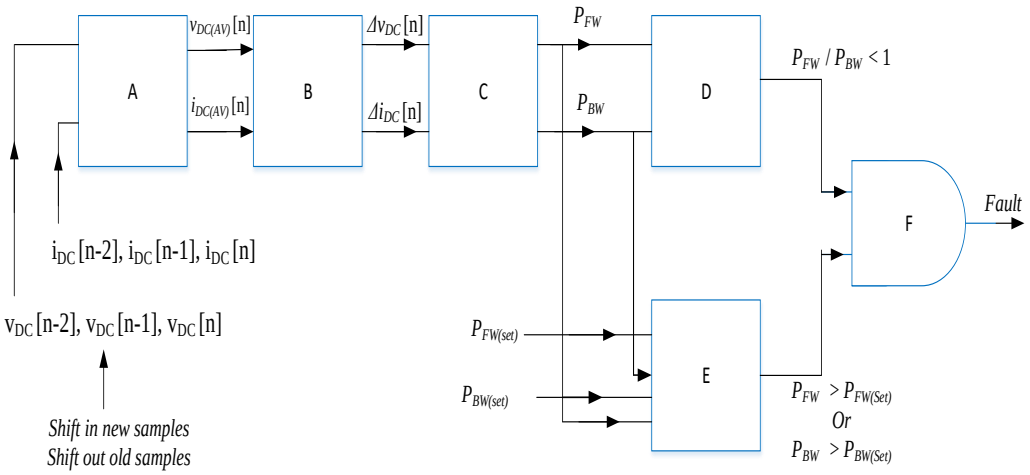


Fig. 7-3 *Block diagram for the protection scheme (TWP)*

Unit "B" computes the incremental quantities, $\Delta v_{DC(AV)}[n]$ and $\Delta v_{DC(AV)}[n]$ respectively. Thus from Equations (6.10) and (6.11), the following are obtained.

$$\Delta v_{DC(AV)}[n] = v_{DC(AV)}[n] - v_{DC(pre-fault)} \tag{7-3}$$

$$\Delta i_{DC(AV)}[n] = i_{DC(AV)}[n] - i_{DC(pre-fault)} \tag{7-4}$$

In ***unit C***, the *FTWP* and *BTWP* (P_{FW} and P_{BW} respectively) are calculated using Equations (6.22) and (6.23) respectively. Thus

$$P_{FW}\,[n] = \frac{1}{4Z_c} \times \Big((\Delta v_{DC(Av)}\,[n])^2 + (2\Delta v_{DC(Av)}[n]\,\Delta i_{DC(Av)}[n] \times Z_c) + \big(\Delta i_{DC(Av)}[n]\,\times Z_c\big)^2 \Big) \tag{7-5}$$

$$P_{BW}\,[n] = \frac{1}{4Z_c} \times \Big((\Delta v_{DC(Av)}\,[n])^2 - (2\Delta v_{DC(Av)}[n]\,\Delta i_{DC(Av)}[n] \times Z_c) + \big(\Delta i_{DC(Av)}[n]\,\times Z_c\big)^2 \Big) \tag{7-6}$$

Unit "*D*" computes the ratio, $\frac{P_{FW}}{P_{BW}}$ to determine whether or not it is less than unity during the measurement period whilst unit "*E*" checks the calculated P_{FW} against a pre-set value, $P_{FW}\ (set)$.

An internal fault (*FIF*) is declared when the conditions in **unit "*F*"** are satisfied.

7.4 Simulation studies

As shown in Figures 7.1 and 7.2, faults F_{g1}, F_{g2}, F_{g3} and F_{g4} are arbitrary fault scenarios on the grid and were assumed to be a positive *P-G* fault in the first instance with a fault resistance of 0.01Ω. All fault scenarios indicated were applied at *2sec* from the start of the simulation and with measurements taken from the positive pole terminal of the DC cable. Following PSCAD simulations, the DC voltages and currents recorded at the relay terminal during pre-fault and post-fault conditions were stored in a text file and thereafter exported to MATLAB work space for post-processing as shown in Figure 7.2

7.4.1 Sampling frequency and window length

As per *IEC* guidelines for DC protection [7], the sampling frequency, f_s used in this thesis was *96 kHz*. The measurement time window, t_W or window length for the relay decision must be within a pre-determined time frame following the detection of transient. Since travelling waves damp quickly, typically less than *1ms* following the arrival of the first incident wave at the relay terminal, t_W was taken to be $500\mu s$ in this study. Generally, this is a matter of compromise and therefore could vary depending on the designer and grid configuration.

Since $f_s = 96kHz$,

Sampling period, $T_s = \frac{1}{96kHz}$

The total number of samples for relay decision, N_T was obtained thus

$$N_T = \frac{t_W}{T_s} \tag{7-7}$$

$$N_T = \frac{500\mu s}{10.42\mu} \approx 48\ samples$$

7.4.2 Simulation results

Still considering Figure 7.1, under steady state condition, *MMC1* and *MMC3* operate as rectifiers and as such import power from the AC side whilst *MMC2* and *MMC4* operate as inverters exporting power to the load and AC grid. The steady state bus bar voltages and the respective relay currents are given in Table 7.1. As shown, faults F_{g1}, F_{g3} and F_{g4} occur at the middle of the cable sections 1, 2 and 3 respectively, whilst F_{g2} occurs at the remote end of cable section 1.

Table 7-1 *Steady State DC voltage and current based on Figure 7.1*

Relay	Steady state DC Voltage ($V_{DC(ss)}$)	Steady state DC current ($i_{DC(ss)}$)
R_{12}	198.54	-1.032
R_{21}	200.81	1.037
R_{23}	200.87	0.198
R_{32}	200.46	-0.195
R_{34}	200.56	-0.051
R_{43}	200.72	0.059
R_{14}	200.64	-0.897
R_{41}	198.64	0.899

Response of Relay R_{12}: The measured travelling wave power components (P_{FW} and P_{BW} respectively) using Equations 7.5 and 7.6 with R_{12} as a reference relay are shown in Figures 7.4 – 7.7.

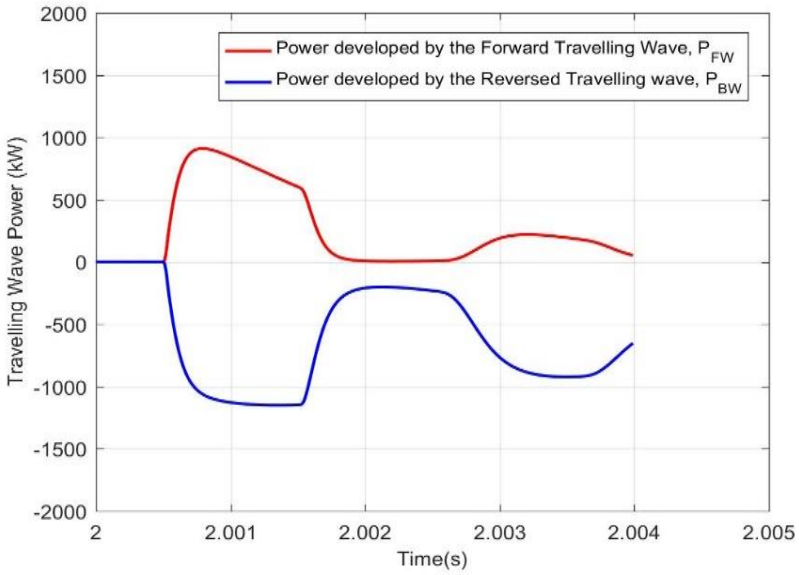


Fig. 7-4 *Forward internal fault (FIF), F_{g1}*

As shown in all plots, under steady state conditions, no travelling waves are generated therefore the *FTWP* and *BTWP* (P_{FW} and P_{BW} respectively) will also be zero. However, at the instant of fault inception (at *t=2s* in this case), travelling waves are generated and propagates along the cables and as such P_{FW} and P_{BW} are developed by the travelling waves.

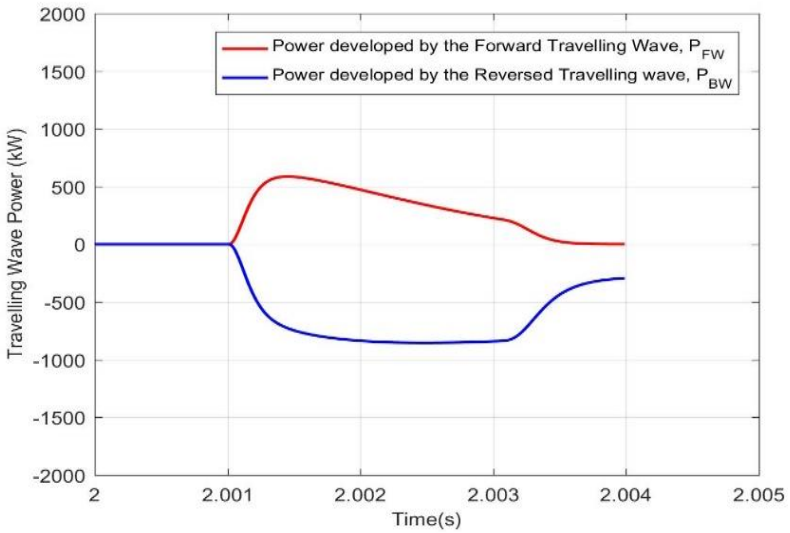


Fig. 7-5 *Forward internal fault (FIF)- F_{g2}*

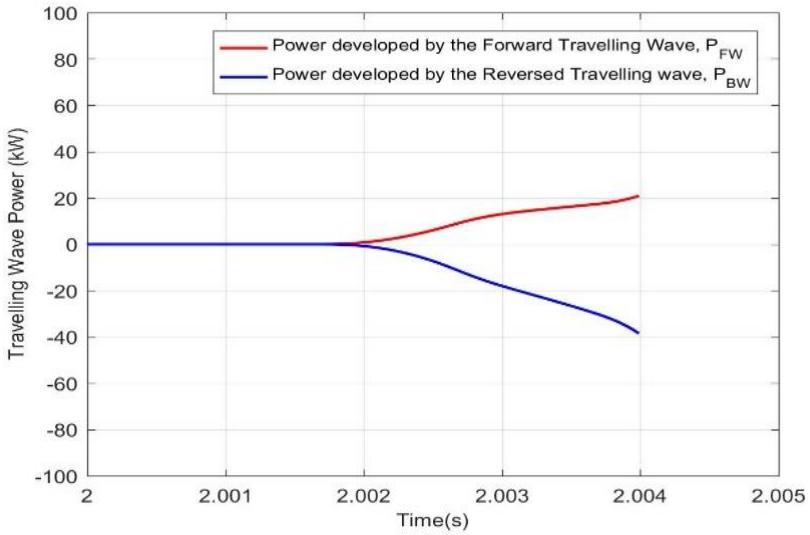


Fig. 7-6 *Forward external fault (FEF) - F_{g3}*

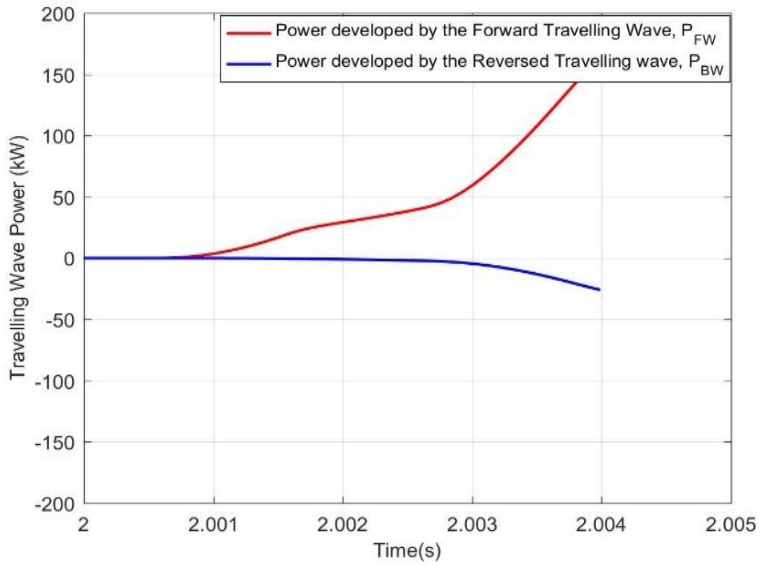


Fig. 7-7 *Reverse directional Fault (RDF) - F_{g4}*

Generally, a significant amount of time will elapse (depending on the distance between the relay terminal and the fault) until the travelling wave component arrives at the relay terminal. This is attributed to the time taken for the travelling wave to propagate from the fault point to the relay terminal. For example, the travelling wave resulting from faults

F_{g1} and F_{g2} shown in Figures 7.4 and 7.5 respectively arrives at the relay terminal (reference relay is R_{12} in this case) at *t=2.00051s* and *t=2.00102s* respectively, noting that F_{g2} is further away from the relay R_{12} that F_{g1}. This is consistent with travelling wave propagation theory and the phenomenon has been widely used for fault location on major transmission lines.

It can also be seen that the travelling wave resulting from fault F_{g3} arrives at a much later time (*t=2.00112s*) than F_{g2} whilst the travelling wave resulting from fault F_{g4} arrives much earlier at *t=2.00003s*. Generally, F_{g4} is much closer to relay R_{12} in the reverse direction. However, these will not pose any problem to the relay because as far as the relay is concerned, the arrival time of the first incident wave at its terminal is regarded as t_0. Generally, the relay unit is expected to be triggered into operation at $t = t_o$.

$$t_o = t_f - t_p \tag{7-8}$$

t_o= arrival time of the first incident wave at the relay terminal
t_f= actual time of fault occurrence
t_p= propagation delay time of the travelling wave on the cable.

Forward directional fault: Still considering Figures 7.4, 7.5 and 7.6 (corresponding to plots for F_{g1}, F_{g2} and F_{g3}), the magnitude of P_{BW} recorded at the relay terminals during the first few milliseconds following the arrival of the first incident wave exceeds that of P_{FW} indicating that fault F_{g1}, F_{g2} and F_{g3} are *FDF* with respect to relay R_{12}. Therefore, the ratio P_{FW}/P_{BW} during the same measurement period will be less than unity. However, the magnitude of P_{FW} and P_{BW} due to fault F_{g1} is significantly larger than that for fault F_{g2}. This is also consistent with travelling wave propagation theory since the waves continuously gets attenuated as they travel along the cable; noting that fault F_{g2} is further away from the relay than fault F_{g1}.

Forward internal versus forward external fault: It can be seen from Figure 7.6 that the magnitude of P_{FW} for F_{g1} and F_{g2} exceeds that for F_{g3}. This is due to the fact that the high frequency contents of the fault generated transient components resulting from fault F_{g3} are attenuated at the boundary at busbar 2 (inductor L_{21} and L_{23} respectively). Generally, the ratio of P_{FW} to P_{BW} will also be less than unity since F_{g3} is a *FDF* with respect to relay R_{12}.

Clearly, the significant reduction in the travelling wave components resulting from fault F_{g3} compared to that of F_{g1} and F_{g2} indicates a *FEF* with respect to relay R_{12} as per magnitude criteria stipulated in Table 6.2.

Reverse directional fault: As shown in Figure 7.7, the magnitude of P_{FW} exceeds that of P_{BW} during the first few milliseconds following the arrival of the first incident wave indicating that F_{g4} is a *RDF* with respect to relay R_{12}, and therefore the ratio P_{FW}/P_{BW} will be greater than unity. This is because the forward travelling wave from fault F_{g4} arrives at the relay terminal before the reverse travelling wave.

Generally, as per the conditions stipulated in Table 6.2, relay R_{12} must operate for faults F_{g1} and F_{g2} but not operate for F_{g3} and F_{g4}. The same also applies to relay R_{21}. Generally, since F_{g1} occurs in the middle of cable section 1, the response of relay R_{21} with respect to fault F_{g1} will be the same as that of R_{12}. The relay settings are arrived at by considering critical conditions for the relay. This is explained in section 7.4. However, the responses of other relays located on the grid is explained hereunder.

7.4.3 Grid relay responses to an external fault

The responses of other relays located on the healthy section of the grid considering fault F_{g1} are shown in Figures 7.8 – 7.13.

Relays R_{23} and R_{32}: Considering the response of relay R_{23} given in Figure 7.8, the first incident wave arriving at its terminal is a forward travelling wave (with respect to its reference direction of current) and hence a *FTWP*, P_{FW} is developed. However, the reverse travelling wave and hence P_{BW} arrives after few milliseconds, following a reflection at busbar 3. Therefore, the ratio of P_{FW} to P_{BW} will be greater than unity and hence satisfying the conditions for *RDF* in Table 6.1. Furthermore, the magnitude of P_{FW} and P_{BW} seen by relay R_{23} are significantly reduced compared to those seen by relay R_{12} and R_{21}. This also indicate that F_{g1} is external to relay R_{23} and hence it will not operate.

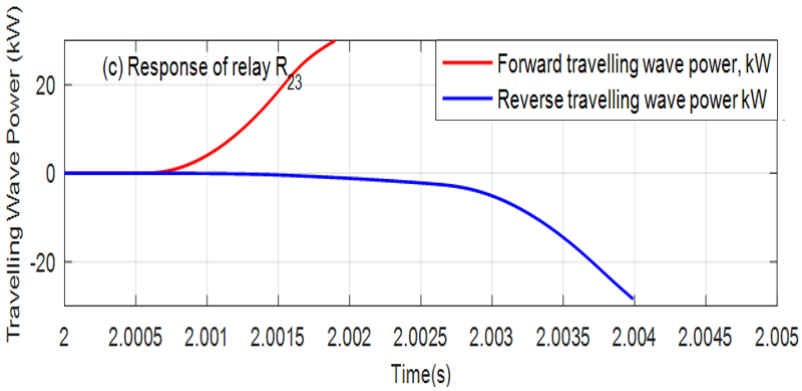


Fig. 7-8 *Response of relay R_{23} to fault F_{g1}*

The same scenario also holds for relay R_{32} shown in Figure 7.9, but in this case, the backward travelling wave arrives before the forward travelling wave, indicating that *Fg1* is a *FDF* with respect to R_{32}.

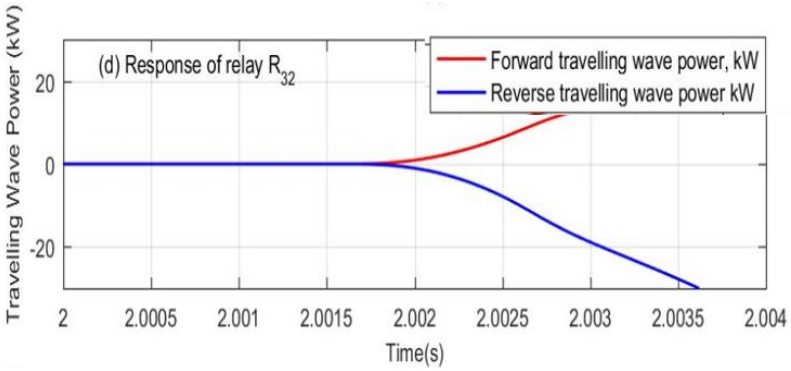


Fig. 7-9 *Response of relay R_{32} to fault F_{g1}*

Relays R_{34} and R_{43}: As shown in Figures 7.10 and 7.11 (responses of R_{34} and R_{43} respectively), P_{FW} exceeds P_{BW} during the first few milliseconds following the arrival of

the first incident wave, satisfying the conditions for *RDF*. However, in this case and depending on the distance from the fault to the relay terminal from either the clockwise or anti-clockwise direction, the ratio of P_{FW} to P_{BW} may be less than or greater than unity. Generally, this is not a major issue as the magnitude criteria (since the threshold is not reached) will not be satisfied and as such relays R_{34} and R_{34} will not operate for fault $F_{g1.}$

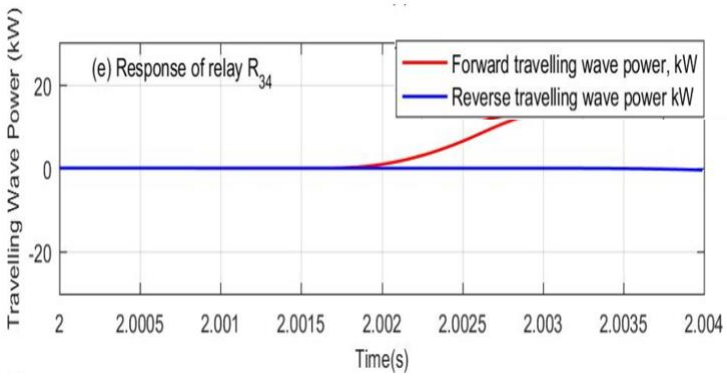


Fig. 7-10 *Response of relay R_{34} to fault F_{g1}*

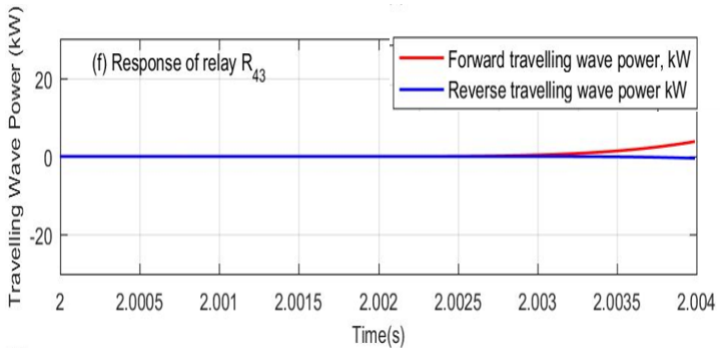


Fig. 7-11 *Response of relay R_{43} to fault F_{g1}*

Considering Figure 7.12, relay R_{41} sees a backward travelling wave and hence P_{BW} is developed until the arrival of the forward travelling wave and P_{FW} is developed. Therefore, P_{FW} / P_{BW} is less than unity, satisfying the criterial for *FDF*. However, the magnitudes of P_{FW} and P_{BW} are significantly attenuated and hence the magnitude criteria (Table 7.2) is not met, therefore R_{41} will not operate

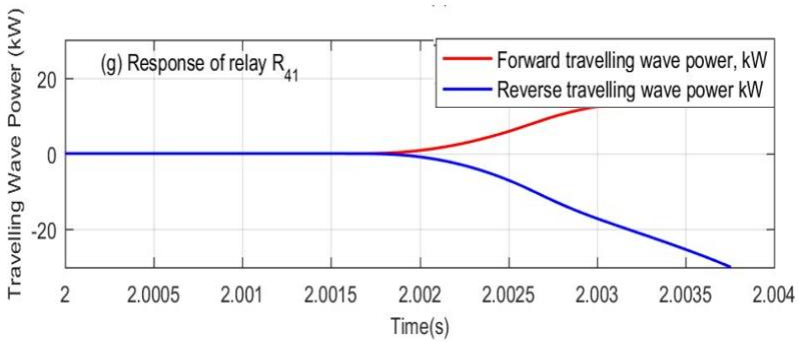


Fig. 7-12 *Response of relay R_{41} to fault F_{g1}*

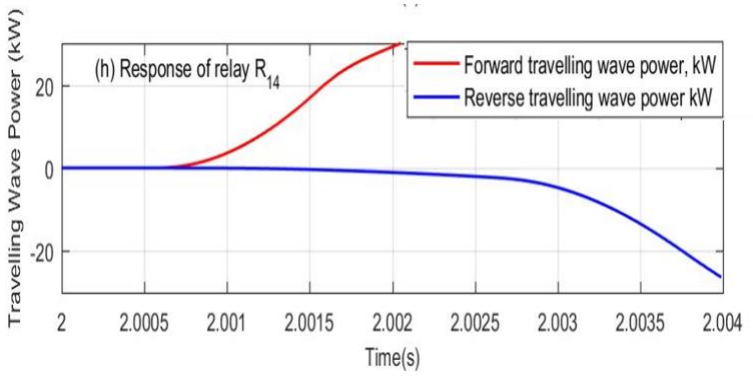


Fig. 7-13 *Response of relay R_{14} to fault F_{g1}*

Relays R_{14} and R_{41}: Considering the response of relay R_{14} shown in Figure 7.13, the relay sees a forward travelling wave before a reverse travelling wave, hence P_{FW} is developed before P_{BW} and hence making the ratio of P_{FW} / P_{BW} to be greater than unity indicating the presence of a RDF with respect to its relay reference direction of current as shown. In this case, both the ratio and magnitude criteria are not met.

7.5 Sensitivity analysis

In order to investigate the sensitivity of the proposed protection strategy and with a view to arriving at a suitable protection threshold for the relays, further simulations were carried out considering fault $F_{(FIF),}$ and $F_{(FEF)}$ in Figure 7.1. Generally, this scenario is representative of the most critical condition for relay R_{12}. Ideally this is a high resistance

remote FIF (say R_f = 300Ω, 500Ω respectively) against a low resistance FEF (say R_f =0.01Ω). For the purpose of this analysis, both *P-G* and *P-P* faults were simulated.

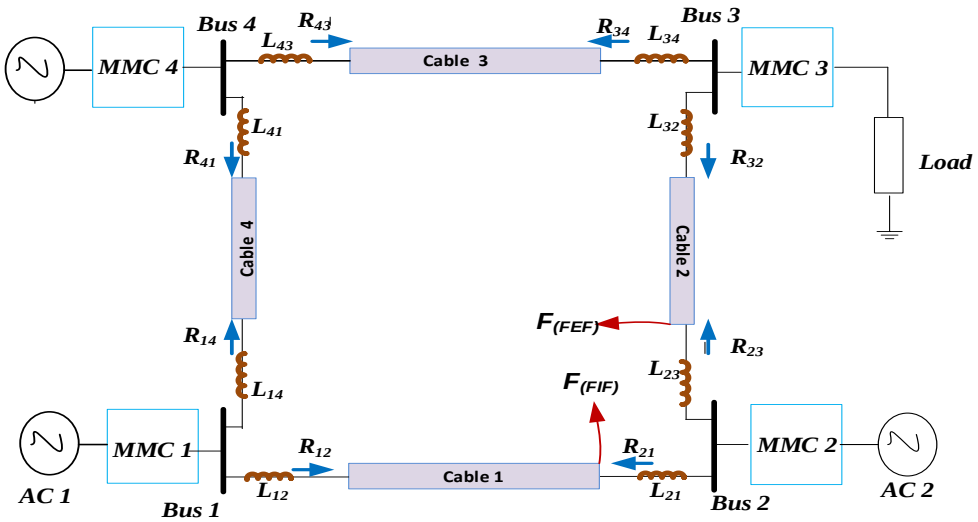


Fig. 7-14 *HVDC test model showing fault scenario for travelling wave*

As shown in Figure 7.14, $F_{(FIF)}$ is a high resistance remote internal fault with respect to relay R_{12}, whilst $F_{(FEF)}$ is a low resistance external fault. This scenario is assumed to be the most critical condition for relay R_{12}. Ideally, this is a high resistance FIF versus a low resistance FIF. The simulation results presented in Figures (7.15) - (7.18) considering $F_{(FIF)}$ and $F_{(FEF)}$ for a P-G and P-P fault respectively, shows that the calculated magnitude of the *FTWP* and *BTWP* for $F_{(FEF)}$ is significantly lower than that of $F_{(FIF)}$ even for a fault resistance of 500Ω *FIF*.

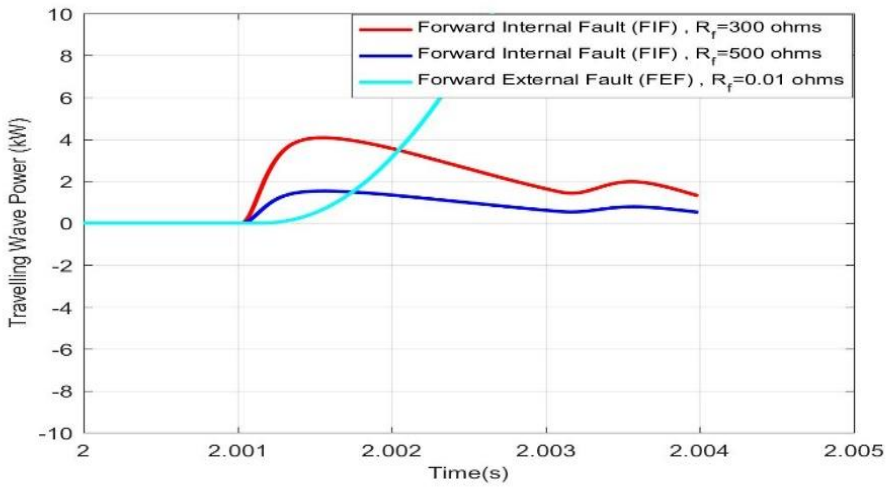


Fig. 7-15 *Forward Travelling wave power (FTWP) - P-G fault*

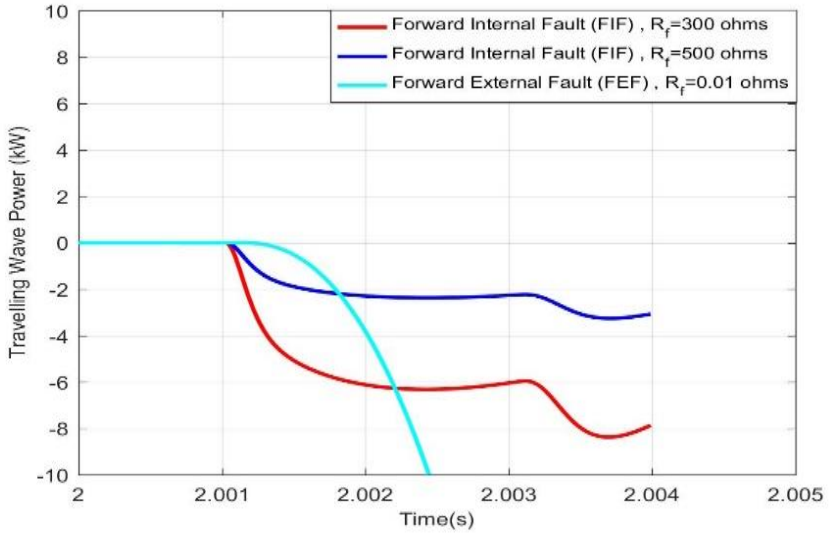


Fig. 7-16 *Backward Travelling wave power (BTWP) - P-G fault*

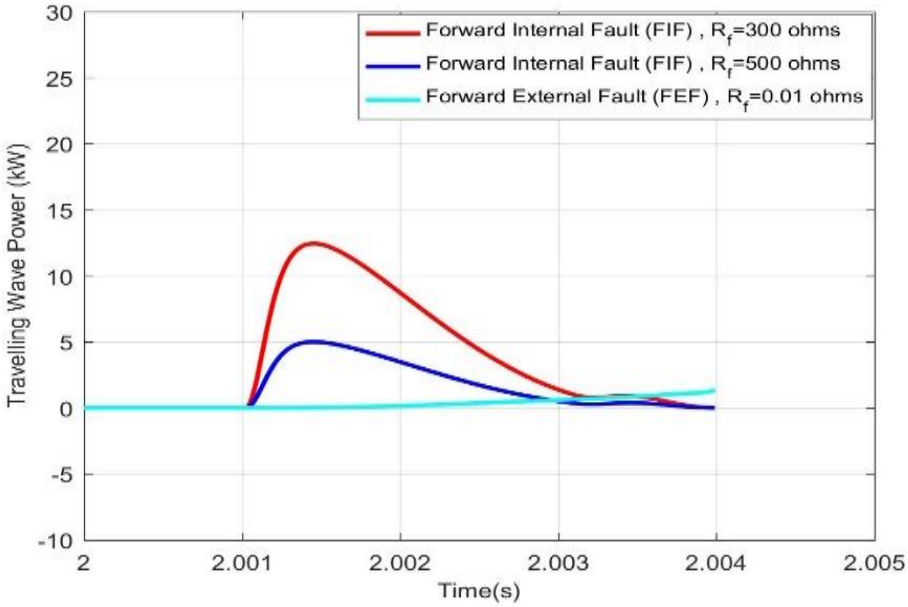


Fig. 7-17 *Forward Travelling wave power (FTWP) - P-P fault*

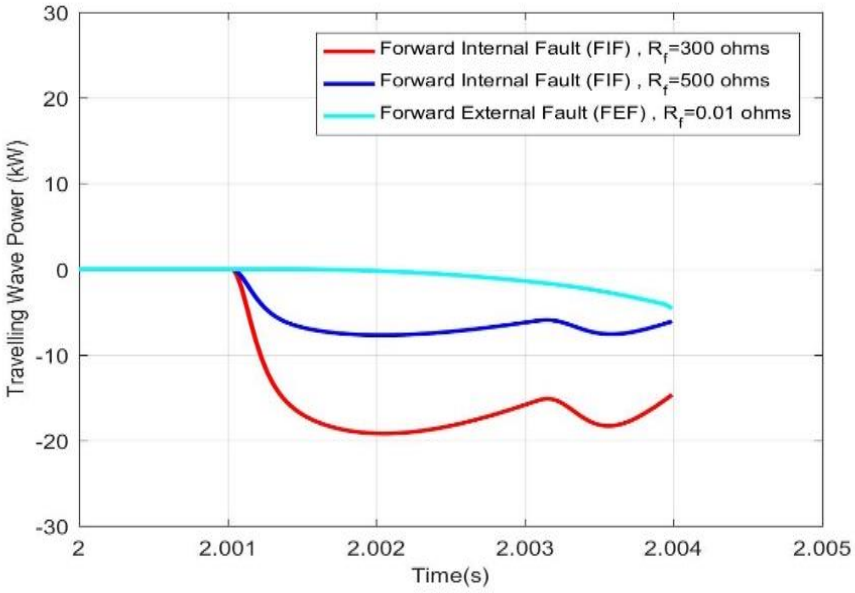


Fig. 7-18 *Backward Travelling wave power (BTWP) - P-P fault*

As shown on the expanded scale the measurements were taken at *0.5ms* following the detection of the first incident wave. The calculated travelling wave power during the first *0.5ms* presented in Table 7.2 also shows consistency with the conditions stipulated in Table 7.2 as per magnitude and ratio criteria. In all, the ratio of the *FTWP* to *BTWP* is less than unity, indicating a *FDF*. Furthermore, the magnitudes of the calculated P_{FW} and P_{BW}.

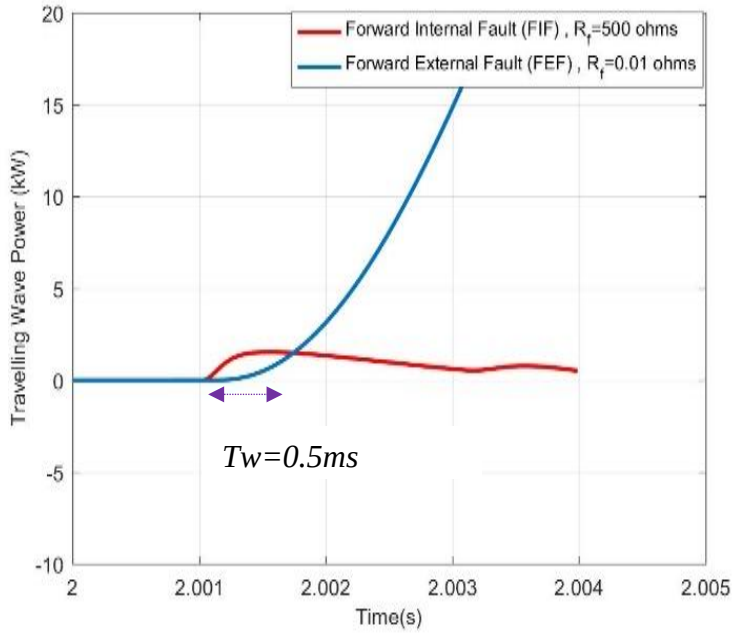


Fig. 7-19 *Critical condition for Relay R_{12} (P-G Fault)*

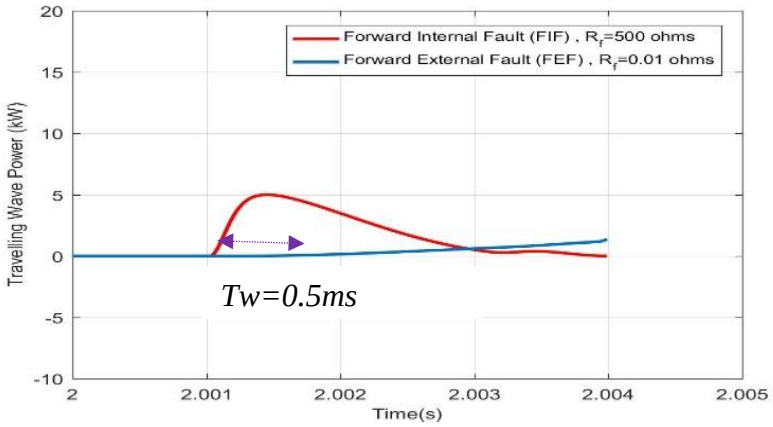


Fig. 7-20 *Critical condition for Relay R_{12} (P-P Fault)*

Generally, since travelling wave damps quickly, measurements must be taken soon after the occurrence of the fault (this is the first incident wave arriving at the relay terminal) since the magnitude P_{FW} and P_{BW} for a low resistance *FEF* after few milliseconds may exceed that of high resistance *FIF* (as in Figure 7.15). This is an undesirable condition that can lead to a spurious relay trip. The relay response during the *0.5ms* time window following the arrival of the first incident wave are presented in Figure 7.21. Assuming a protection setting of *1.52kW* it can be seen from Figure 7.21 that relay R_{21} would operate for all internal fault and not operate for all external faults indicated. It is hypothesised that once a local relay can provide the discrimination for this scenario (critical condition), then the relay will operate for all other fault along the cable section. The same holds for the remaining relays located on the grid. Generally, the threshold for this study assumes a 500Ω remote internal fault, however for cables this is not usually the case. This implies that reducing the fault resistance will results in higher protection threshold and hence further improving the sensitivity of the protection algorithm.

Each relay has been tested against six fault scenarios, therefore this study assumes a total number of 48 scenarios which are representative of the possible fault scenarios that can

exist on the grid. It can be seen from Table 7.2 that in all cases presented and considering both *P-G* and *P-P* faults, the magnitude of P_{FW} and P_{BW} for the internal faults are larger than those for external faults. Also, the ratio of P_{FW} to P_{BW} is less than unity indicating a *FDF* with respect to the local relay.

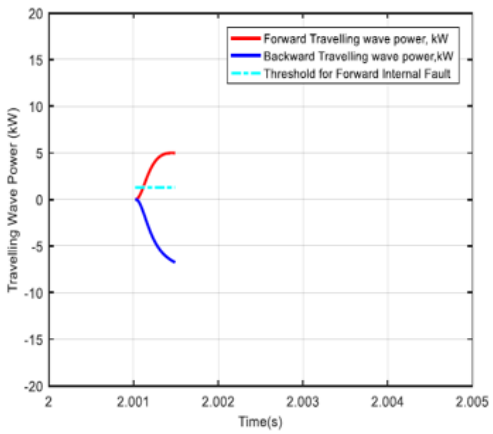
Table 7-2 *Calculated Forward and backward travelling wave power (TWP)*

Fault name	$\lvert P_{FW} \rvert$ *(kW)*	$\lvert P_{BW} \rvert$ *(kW)*	$\lvert P_{FW} \rvert / \lvert P_{BW} \rvert$
$FIF_{(Rf=300\Omega)\ P\text{-}G}$	*4.05*	*5.03*	*0.81*
$FIF_{(Rf=500\Omega)P\text{-}G}$	*1.52*	*1.82*	*0.81*
$FEF_{(Rf=0.01\Omega)P\text{-}G}$	*0.75*	*0.82*	*0.92*
$FIF_{(Rf=300\Omega)\ P\text{-}P}$	*12.40*	*16.83*	*0.74*
$FIF_{(Rf=500\Omega)\ P\text{-}P}$	*4.98*	*6.75*	*0.74*
$FEF_{(Rf=0.01\Omega)\ P\text{-}P}$	*0.063*	*0.076*	*0.84*

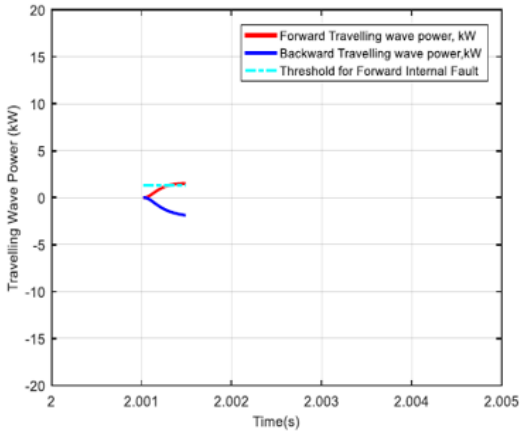
FIF: forward internal fault FEF: Forward external fault

(a) *Forward internal fault (FIF),* R_f*=300Ω* ***(b)*** *Forward internal fault (FIF),* R_f*=500Ω*

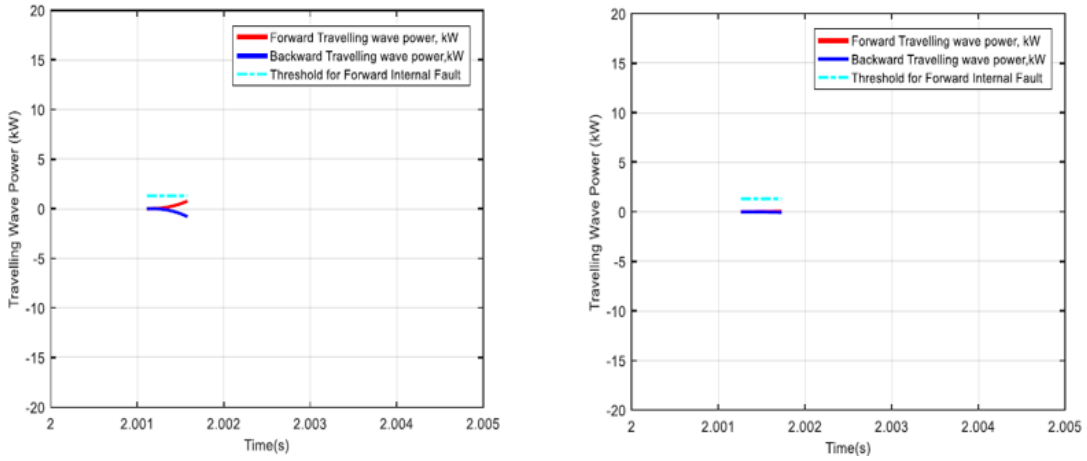
The flow chart for the protection scheme utilising TWP is shown in Figure 7.22 whilst the complete protection algorithm implemented in MATLAB is given in Appendix A7.1.



(a) *Forward internal fault (FIF),* R_f*=300Ω*



(b) *Forward internal fault (FIF),* R_f*=500Ω*



(c) Reverse directional fault (RDF), R_f=0.01Ω *(d) Forward external fault (FEF), R_f=0.01Ω*

Fig. 7-21 *Actual Relay response for internal and external faults during measurement time window*

7.5.1 The protection starter

In order to ensure that the protection scheme remains stable during normal operating conditions, a protection starter was incorporated into the protection scheme. The protection starter used in this scheme is a *dv/dt* element. Once the threshold set for the starting element is exceeded, the main protection system is triggered into operation. The measurement time window, t_w or window length must be within a pre-determined time frame following the detection of transient as determined by the protection starter. Since the travelling wave on a transmission damps out quickly, typically less than *1ms*, t_w was taken to be $500\mu s$ in this thesis

$$t_w = t_m - t_d \qquad (7\text{-}9)$$

t_d = Arrival time of the first incident wave at the local relay terminal

t_m = Relay trip time; which also corresponds to the measurement time.

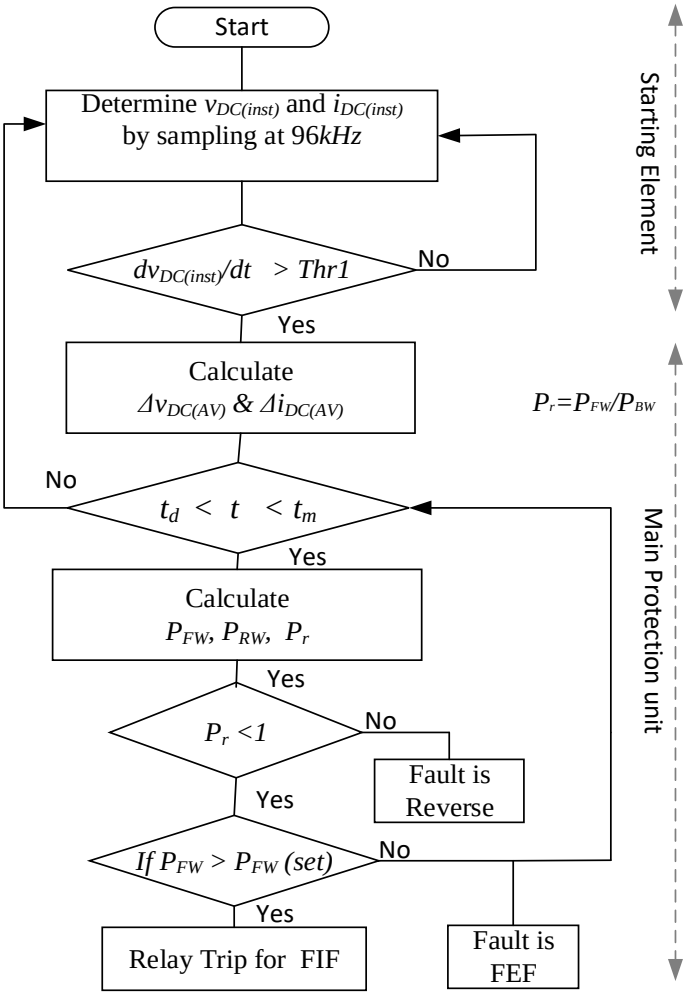


Fig. 7-22 *Flow chart for the proposed protection scheme utilising travelling wave power*

In this study, a *dv/dt* of $1V/\mu s$ was taken as the threshold for the starting element. Since all cable sections are assumed to be the same length (=200km) in this study, this value was consistent for all local relays indicated. This value was arrived at by considering a FEF occurring at remote end of an adjacent feeder with respect to a local relay. For example, with respect to relay R_{12} on Figure 7.5, this will be a fault F_{32}.

Based on Equations 6.33 and 6.34, the *FTWE* as well as the *BTWE* were calculated as shown in Figure 7.23. The results presented in Table 7.3 also shows consistency with the conditions of Table 6.3.

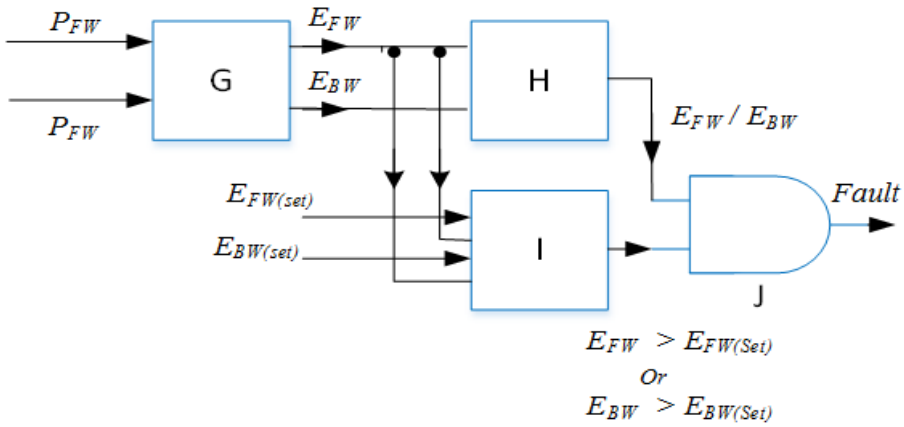


Fig. 7-23 *Block diagram for the protection scheme (TWE)*

Table 7-3 *Calculated Forward and backward travelling wave energy (TWE)*

Fault name	$\lvert E_{FW} \rvert$ *(kJ)*	$\lvert E_{BW} \rvert$ *(kJ)*	$\lvert E_{FW} \rvert / \lvert E_{BW} \rvert$
$FIF_{(Rf=300\Omega)P\text{-}G}$	0.0013	0.0014	0.88
$FIF_{(Rf=500\Omega)\ P\text{-}G}$	4.7573e-04	5.3396e-04	0.89
$FEF_{(Rf=0.01\Omega)P\text{-}G}$	1.1224e-04	1.1713e-04	0.95
$FIF_{(Rf=300\Omega)\ P\text{-}P}$	0.0041	0.0049	0.83
$FIF_{(Rf=500\Omega)\ P\text{-}P}$	0.0016	0.0020	0.84
$FEF_{(Rf=0.01\Omega)\ P\text{-}P}$	1.0947e-05	1.1637e-05	0.94

FIF: forward internal fault FEF: Forward external fault

It can also be seen from Table 7.3 that in all cases presented and considering both *P-G* and *P-P* faults, the magnitude of E_{FW} and E_{BW} for the internal faults are larger than those for external faults. Also, the ratio of E_{FW} to E_{BW} is less than unity indicating a *FDF* with respect to the local relay. Generally, this is expected as energy is proportional to power. Generally, either the *TWP* or *TWE* can be used for fault identification. However, this study adopts the calculated magnitude of the *TWE* during the first $500\mu s$ following the detection of the transient for fault identification and detection. The flow chart for the protection scheme utilising TWE is shown in Figure 7.24 and the MATLAB code is presented in Appendix A7.1.

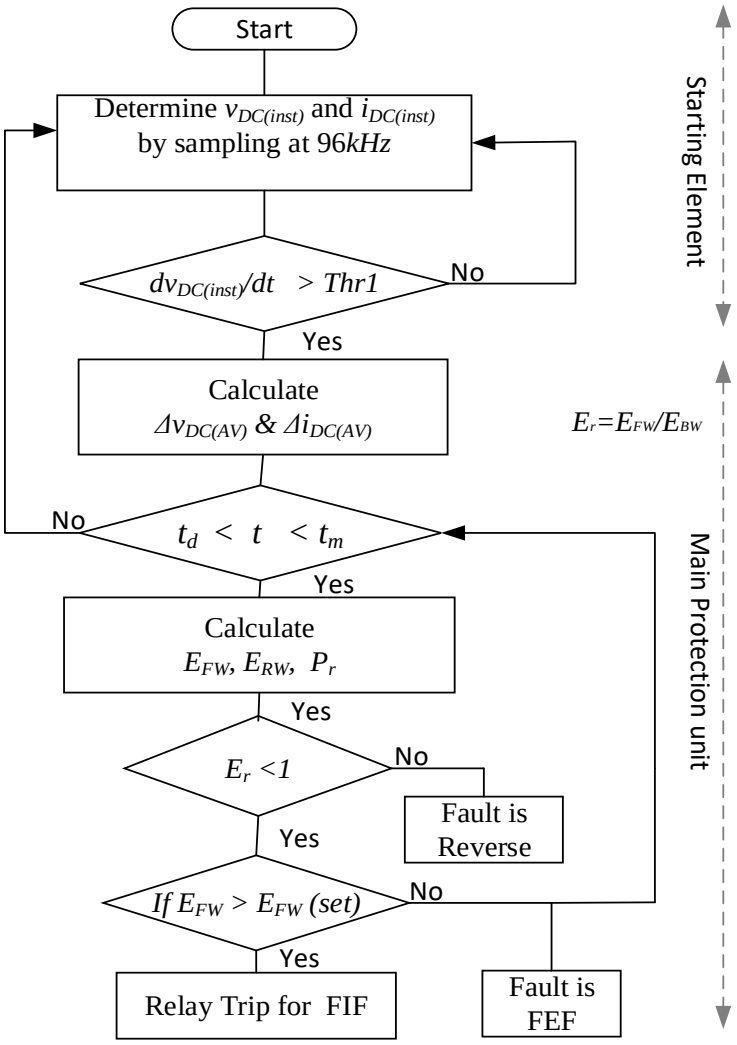
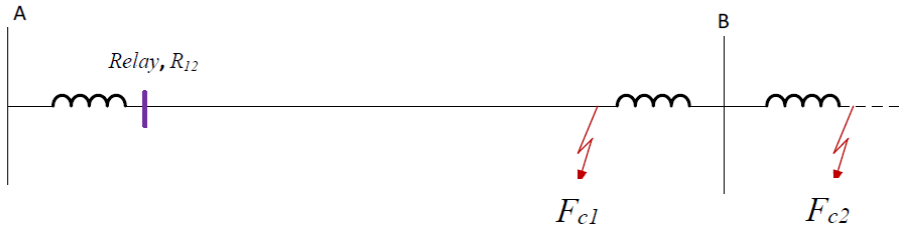


Fig. 7-24 *Flow chart for the proposed protection scheme utilising travelling wave energy*

An advantage of using the TWE over the TWP is that the former uses the energy over a predetermined period of time whereas the latter uses the instantaneous value of the power. This advantage is of high significance in discriminating between high resistances FIF against a low resistance FEF; nothing that the actual magnitude for FEF may be larger than FIF and as such may lead to faulty relay discrimination.

7.5.2 The Protection threshold

In this study, the most critical condition for a local relay (R_{12} in this case) was used as a basis for arriving at the relay settings. This is a 500Ω *FIF* versus 0.01Ω remote *FEF* as shown in Table 7.2, and considering a P-G fault. Generally, the magnitude of the TWP and TWE for P-G faults are significantly lower than those for a P-P fault.



F_{c1}: *High resistance remote internal fault; say* R_f=500Ω
F_{c2}: *Low resistance external fault; say* R_f=0.01Ω

Fig. 7-25 *Determination of the protection threshold*

Generally, either the *TWP* or the *TWE* can be used for fault identification. The protection threshold for the *TWP* and *TWE* are given in Tables 7.4 and 7.5 respectively.

Table 7-4 *Protection threshold utilising travelling wave power (TWP)*

Travelling wave Power, TWP (kW)	
FTWP	*1.50*
BTWP	*1.80*

Note: length of cable = 200km

Table 7-5 *Protection threshold utilising travelling wave energy (TWE)*

Travelling wave Power, TWE (kJ)	
FTWE	4×10^{-4}
BTWE	5×10^{-4}

Note: length of cable = 200km

Based on this calculated threshold for the *TWP* and *TWE*, further studies were carried out considering wider cases of fault scenarios for varying fault resistances and fault locations as shown in Figure 7.23. For this purpose, each relay was tested against the most critical scenarios.

The *dv/dt* threshold was arrived at by considering a remote internal fault occurring at an adjacent feeder with respect to a local relay. For example, with respect to relay R_{12} of Figure 7.25, the *dv/dt* element for a fault occurring at F_{32} is used as the starting element and was calculated to be 1000kV/s. Generally, this a matter of compromise depending on the designer.

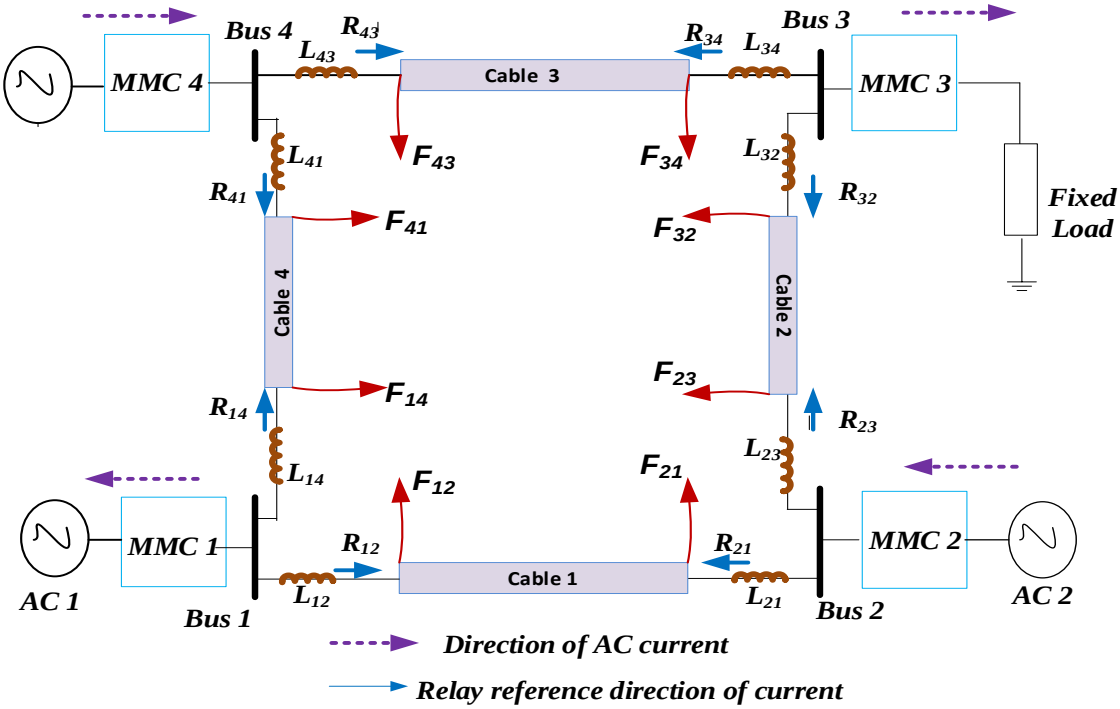


Fig. 7-26 HVDC grid considering wider cases of fault scenarios

For example, considering cable section 1, the most critical condition is to provide discrimination between F21 and F23; while that of R21 is F12 versus F14. Details are shown in Table 7.6. It has been hypothesised that once the relay can provide discrimination as indicated in Tables 7.4 and 7.5, the relay should provide discriminations

for all external faults. This is in anticipation that the system operating conditions remain unchanged. This study assumes a worst case scenario of 500Ω remote internal external fault against a low resistance (0.01Ω) external fault to arrive at the protection threshold. However, for improved sensitivity, the fault resistance can be reduced, and this will be a matter of compromise and depending on the designer. In practice, a fault resistance of 500μs; therefore it can be hypothesised that once the relay provide fault discrimination for this setting, then it will operate for all possible fault scenario which can occur on the DC grid. The calculated values of the TWP and TWE for both P-P and P-G faults considering the fault scenarios indicated in Figure 7.25 are presented in Tables 7.7 - 7.10. The results presented (for P-G and P-P faults respectively) shows consistency with expected results as per the conditions for internal versus external fault (the ratio and magnitude criteria stipulated in Table 6.2). In all cases, all local relays are tested against their most critical condition. For example, Considering Table 7.6, and for all relays indicated, the calculated magnitude of P_{FW} and P_{BW} for all high resistance FIF during the first 500μs exceeds that of FEF.

Table 7-6 *Critical conditions for relays of Figure 7.25*

Relay	Most Critical Conditions
R_{12}	F_{21} *(Rf=500Ω) versus* F_{23} *(Rf=0.01)*
R_{21}	F_{12} *(Rf=500Ω) versus* F_{14} *(Rf=0.01)*
R_{23}	F_{32} *(Rf=500Ω) versus* F_{34} *(Rf=0.01)*
R_{32}	F_{23} *(Rf=500Ω) versus* F_{21} *(Rf=0.01)*
R_{34}	F_{43} *(Rf=500Ω) versus* F_{41} *(Rf=0.01)*
R_{43}	F_{34} *(Rf=500Ω) versus* F_{32} *(Rf=0.01)*
R_{41}	F_{14} *(Rf=500Ω) versus* F_{12} *(Rf=0.01)*
R_{14}	F_{41} *(Rf=500Ω) versus* F_{43} *(Rf=0.01)*

Therefore, considering a protection setting of 1.52 and 1.82 for $P_{FW(set)}$ and $P_{(BW(set)}$ respectively, all relays indicated will operate for *FIF* and not operate for *FEF*. As earlier stated, either P_{FW} and P_{BW} can be used for fault identification. can be seen that with the protection settings indicated in Tables 7.4 and 7.5 for TWP and TWE respectively. As shown, the calculated magnitude of the travelling wave components falls within the settings given in Tables 7.4 and 7.5.

Table 7-7 Calculated *FTWP*, P_{FW} and *BTWP*, P_{BW} based on Figure. 7.13 (Pole-ground fault)

Local relay	*Fault Location*	*Fault type with respect to local relay*	*Fault Resistance(Ω)*	$\lvert P_{FW}\rvert$ *(kJ)*	$\lvert P_{BW}\rvert$ *(kJ)*	$\lvert P_{FW}\rvert$ / $\lvert P_{BW}\rvert$
	F_{21}	*FIF*	*300*	*4.25*	*5.03*	*0.84*
R_{12}	F_{21}	*FIF*	*500*	*1.52*	*1.82*	*0.81*
	F_{23}	*FEF*	*0.01*	*0.75*	*0.82*	*0.92*
	F_{12}	*FIF*	*300*	*4.16*	*5.13*	*0.81*
R_{21}	F_{12}	*FIF*	*500*	*1.61*	*1.97*	*0.82*
	F_{14}	*FEF*	*0.01*	*0.91*	*0.98*	*0.92*
	F_{32}	*FIF*	*300*	*4.27*	*5.32*	*0.80*
R_{23}	F_{32}	*FIF*	*500*	*1.65*	*2.04*	*0.81*
	F_{34}	*FEF*	*0.01*	*1.29*	*1.45*	*0.88*
	F_{23}	*FIF*	*300*	*4.41*	*5.40*	*0.82*
R_{32}	F_{23}	*FIF*	*500*	*1.71*	*2.10*	*0.81*
	F_{21}	*FEF*	*0.01*	*1.18*	*1.34*	*0.88*
	F_{43}	*FIF*	*300*	*4.46*	*5.38*	*0.83*
R_{34}	F_{43}	*FIF*	*500*	*1.74*	*2.09*	*0.83*
	F_{41}	*FEF*	*0.01*	*0.96*	*1.15*	*0.83*
	F_{34}	*FIF*	*300*	*4.46*	*5.54*	*0.80*
R_{43}	F_{34}	*FIF*	*500*	*1.76*	*2.18*	*0.81*
	F_{32}	*FEF*	*0.01*	*1.16*	*1.37*	*0.85*
	F_{14}	*FIF*	*300*	*4.32*	*5.08*	*0.85*
R_{41}	F_{21}	*FIF*	*500*	*1.78*	*2.17*	*0.82*
	F_{23}	*FEF*	*0.01*	*1.01*	*1.11*	*0.91*
	F_{41}	*FIF*	*300*	*4.18*	*5.17*	*0.81*
R_{14}	F_{41}	*FIF*	*500*	*1.71*	*2.09*	*0.82*
	F_{43}	*FEF*	*0.01*	*1.09*	*1.31*	*0.83*

FIF: Forward internal fault FEF: Forward external fault

The same also holds for Table 7.8 for P-P fault, however a protection threshold arrived at using the setting for a P-G fault would accurately protect the entire line. In all cases

shown, the ratio of P_{FW} to P_{BW} for both the P-G and P-P is less than unity indicating a FDF. Considering Table 7.8 and 7.9, it can also be seen that the calculated magnitudes of EFW and EBW for FIF exceeds those of FEF during the measurement period. It can also be seen that for a protection setting $P_{FW(set)}$ and $P_{BW(set)}$ of 4e-5 and 5e-5 respectively, the relay would provide discrimination between FIF and FEF. The same also holds in Table 7.10 for a P-P fault.

Table 7-8 *Calculated FTWP, P_{FW} and BTWP, P_{BW} based on Figure 7.13 (Pole-Pole fault)*

Local relay	*Fault Location*	*Fault type with respect to local relay*	*Fault Resistance(Ω)*	$\lvert P_{FW} \rvert$ *(kJ)*	$\lvert P_{BW} \rvert$ *(kJ)*	$\lvert P_{FW} \rvert / \lvert P_{BW} \rvert$
	F_{21}	FIF	300	12.4	16.83	0.75
R_{12}	F_{21}	FIF	500	4.98	6.75	0.74
	F_{23}	FEF	0.01	0.063	0.076	0.84
	F_{12}	FIF	300	12.52	16.89	0.74
R_{21}	F_{12}	FIF	500	5.24	7.01	0.74
	F_{14}	FEF	0.01	0.062	0.086	0.72
	F_{32}	FIF	300	12.67	17.07	0.74
R_{23}	F_{32}	FIF	500	5.34	7.42	0.72
	F_{34}	FEF	0.01	0.052	0.062	0.839
	F_{23}	FIF	300	13.70	17.58	0.86
R_{32}	F_{23}	FIF	500	5.38	6.12	0.88
	F_{21}	FEF	0.01	0.048	0.058	0.83
	F_{43}	FIF	300	12.53	16.90	0.74
R_{34}	F_{43}	FIF	500	5.24	7.06	0.74
	F_{41}	FEF	0.01	0.063	0.088	0.72
	F_{34}	FIF	300	13.4	18.03	0.75
R_{43}	F_{34}	FIF	500	5.53	7.40	0.75
	F_{32}	FEF	0.01	0.050	0.058	0.86
	F_{14}	FIF	300	12.7	17.0	0.74
R_{41}	F_{21}	FIF	500	5.03	6.98	0.72
	F_{23}	FEF	0.01	0.071	0.081	0.88
	F_{41}	FIF	300	13.90	17.89	0.77
R_{14}	F_{41}	FIF	500	5.77	6.64	0.87
	F_{43}	FEF	0.01	0.056	0.071	0.79

FIF : Forward internal fault FEF : Forward external fault

Generally, irrespective of the operating conditions such as the steady state operating current (see Table 7.1) which is largely dependent on the load parameters as well as the voltage drop along the cables, the calculated travelling wave components, P_{FW}, P_{BW}, E_{FW} and E_{BW} remains comparably the same.

Table 7-9 Calculated *FTWE*, E_{FW} and *BTWE*, E_{BW} based on Figure. 7.13 (Pole-ground fault)

Local relay	*Fault Location*	*Fault type with respect to local relay*	*Fault Resistance(Ω)*	$\lvert E_{FW} \rvert$ *(kJ)*	$\lvert E_{BW} \rvert$ *(kJ)*	$\lvert E_{FW} \rvert / \lvert E_{BW} \rvert$
	F_{21}	FIF	300	0.0013	0.0014	0.88
R_{12}	F_{21}	FIF	500	4.3e-4	5.3e-3	0.89
	F_{23}	FEF	0.01	1.12e-4	1.17e-4	0.95
	F_{12}	FIF	300	0.0013	0.0015	0.89
R_{21}	F_{12}	FIF	500	5.12e-4	5.7e-4	0.89
	F_{14}	FEF	0.01	1.55e-4	1.62e-4	0.91
	F_{32}	FIF	300	0.0014	0.0015	0.88
R_{23}	F_{32}	FIF	500	5.2e-4	5.9e-4	0.88
	F_{34}	FEF	0.01	2.1e-4	2.3e-4	0.92
	F_{23}	FIF	300	0.0014	0.0016	0.88
R_{32}	F_{23}	FIF	500	5.38e-4	6.12e-4	0.88
	F_{21}	FEF	0.01	1.41e-4	1.57e-4	0.90
	F_{43}	FIF	300	0.0014	0.0016	0.90
R_{34}	F_{43}	FIF	500	5.51e-4	6.1e-4	0.90
	F_{41}	FEF	0.01	1.2e4	1.4e-4	0.85
	F_{34}	FIF	300	0.0014	0.0016	0.88
R_{43}	F_{34}	FIF	500	5.52e-4	6.3e-4	0.87
	F_{32}	FEF	0.01	1.22e4	1.47e-4	0.83
	F_{14}	FIF	300	0.0013	0.0015	0.86
R_{41}	F_{21}	FIF	500	5.53e-4	6.1e-4	0.90
	F_{23}	FEF	0.01	1.2e4	1.4e-4	0.86
	F_{41}	FIF	300	0.0014	0.0016	0.88
R_{14}	F_{41}	FIF	500	7.5e-4	8.1e-4	0.92
	F_{43}	FEF	0.01	1.2e-4	1.4e-4	0.85

FIF: Forward internal fault FEF: Forward external fault

This underpins the fact that the travelling wave is largely dependent on the superimposed components (or incremental quantities) but not the actual magnitude of the current or

voltage. Based on this, the effect of the varying DC inductor on the accuracy of the protection scheme was investigated.

Table 7-10 Calculated *FTWE, E_{FW}* and *BTWE, E_{BW}* based on Figure. 7.13 (Pole-Pole fault)

Local relay	*Fault Location*	*Fault type with respect to local relay*	*Fault Resistance(Ω)*	*$\|E_{FW}\|$ (kJ)*	*$\|E_{BW}\|$ (kJ)*	*$\|E_{FW}\| / \|E_{BW}\|$*
	F_{21}	*FIF*	*300*	0.0042	0.0050	*0.84*
R_{12}	*F_{21}*	*FIF*	*500*	0.0016	0.0020	*0.84*
	F_{23}	*FEF*	*0.01*	*1.1e-5*	*1.2e-5*	*0.94*
	F_{12}	*FIF*	*300*	*0.0042*	*0.005*	*0.84*
R_{21}	*F_{12}*	*FIF*	*500*	*0.002*	*0.0026*	*0.77*
	F_{14}	*FEF*	*0.01*	*1.2e-5*	*1.3e-5*	*0.92*
	F_{32}	*FIF*	*300*	*0.0042*	*0.005*	*0.84*
R_{23}	*F_{32}*	*FIF*	*500*	*0.0018*	*0.0022*	*0.809*
	F_{34}	*FEF*	*0.01*	*1.2e-5*	*1.26e-5*	*0.95*
	F_{23}	*FIF*	*300*	*0.0045*	*0.0052*	*0.86*
R_{32}	*F_{23}*	*FIF*	*500*	*0.002*	*0.0024*	*0.83*
	F_{21}	*FEF*	*0.01*	*0.9e-5*	*1.2e-5*	*0.75*
	F_{43}	*FIF*	*300*	*0.0014*	*0.0016*	*0.88*
R_{34}	*F_{43}*	*FIF*	*500*	*5.14e-4*	*5.84e-4*	*0.88*
	F_{41}	*FEF*	*0.01*	*1.58e-4*	*1.67e-4*	*0.95*
	F_{34}	*FIF*	*300*	*0.0045*	*0.0053*	*0.85*
R_{43}	*F_{34}*	*FIF*	*500*	*0.018*	*0.022*	*0.81*
	F_{32}	*FEF*	*0.01*	*1.01e-5*	*1.2e-5*	*0.84*
	F_{14}	*FIF*	*300*	0.0049	0.0060	*0.82*
R_{41}	*F_{21}*	*FIF*	*500*	0.0023	0.0029	*0.79*
	F_{23}	*FEF*	*0.01*	*1.31e-5*	*1.46e-5*	*0.90*
	F_{41}	*FIF*	*300*	*0.0065*	*0.0081*	*0.80*
R_{14}	*F_{41}*	*FIF*	*500*	*0.0029*	*0.0040*	*0.72*
	F_{43}	FEF	0.01	*1.11e-5*	*1.46e-5*	0.76

FIF : Forward internal fault FEF : Forward external fault

7.5.3 Effect of Variations in the DC inductor

For this purpose, a P-G fault was applied to cable section 1 considering a 300Ω remote internal fault with respect to a local relay as shown. The DC inductor at both ends of the cable was varied (L=0.01H, 0.25H and 0.5H respectively). The results presented in Table

7.11 shows that the travelling wave components is only slighted affected by the variation in the DC link inductors.

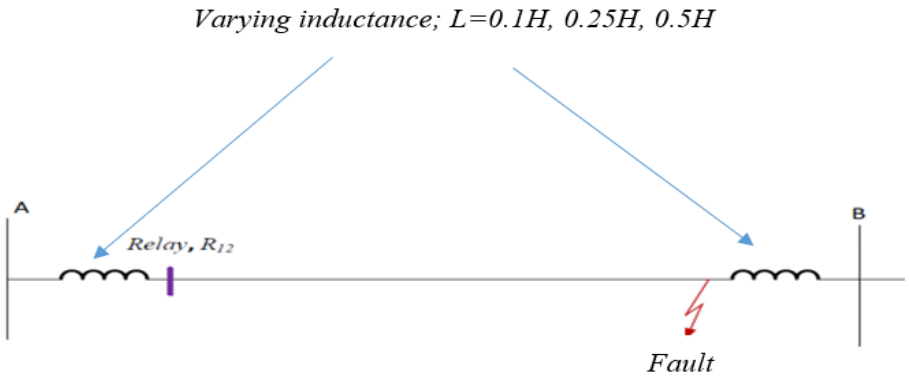


Fig. 7-27 *Section of DC grid showing varying DC side inductance*

Table 7-11 *Effect of varying DC link Inductance on the sensitivity of the protection scheme (R_f=300Ω)*

Parameter	***L=0.1H***	***L=0.25H***	***L=0.5H***
P_{FW} *(kW)*	4.25	5.186	5.67
P_{BW} *(kW)*	5.03	6.24	6.85
E_{FW} *(kJ)*	0.0013	0.0015	0.0016
E_{BW} *(kJ)*	0.0014	0.0018	0.0020
P_{FW}/P_{BW}	0.81	0.83	0.83
E_{FW}/E_{BW}	0.88	0.84	0.81

7.5.4 Effect of fault distance

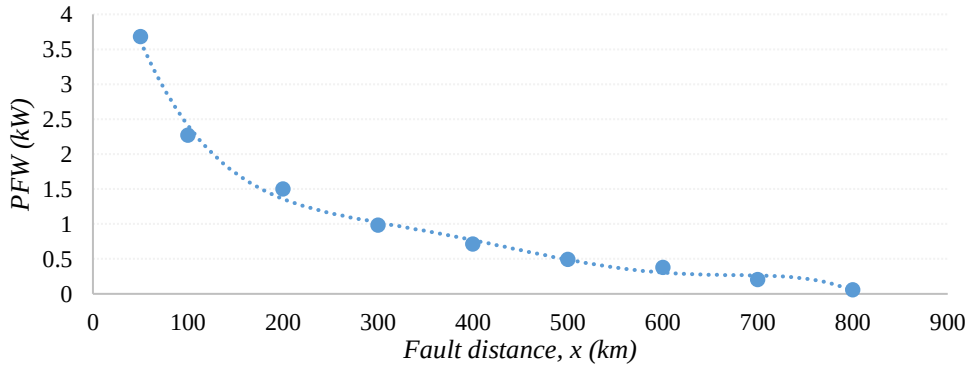
Further studies were also carried out to investigate the effect of fault distance on the proposed protection scheme. For this purpose, the fault resistance was kept at the most critical condition (Rf=500Ω in this study) and the fault distance was arbitrary varied, thus 50km, 100km, 200km, 300km, 400km, 500km, 600km, 700km and 800km. The results obtained considering a P-G and P-G fault for P_{FW} and E_{BW} are given in Table 7.11. The plots of the P_{FW} and E_{FW} against the fault distance are presented in Figures 7.28 – 7.31.

The results as presented show an exponential decrease in the magnitude of the travelling wave components, P_{FW}, P_{BW}, E_{FW} and E_{BW} respectively.

Table 7-12 *Calculated values of travelling wave components versus distance*

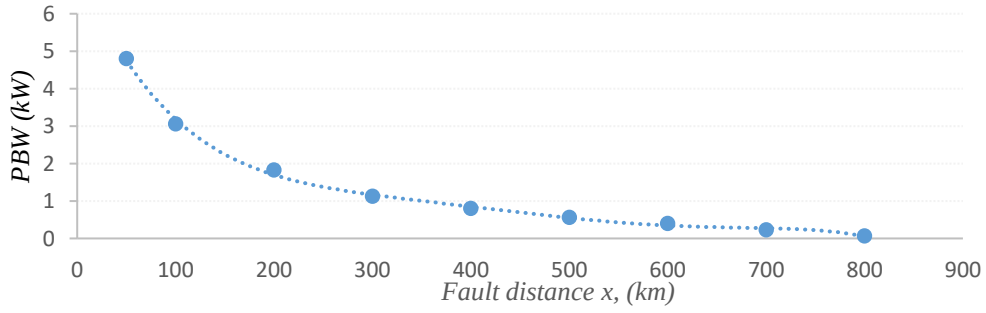
Fault Distance (km)	P_{FW} *(kW)*	P_{BW} *(kW)*	E_{FW} *(kJ)*	E_{BW} *(kJ)*
50	3.6801	4.8004	1.41×10^{-4}	1.68×10^{-4}
100	2.2717	3.0612	1.04×10^{-4}	1.25×10^{-4}
200	1.5003	1.8237	4.31×10^{-5}	5.42×10^{-5}
300	0.9812	1.1278	2.78×10^{-5}	2.95×10^{-5}
400	0,7146	0.801	2.00×10^{-5}	2.40×10^{-5}
500	0.4942	0.5607	1.33×10^{-5}	1.87×10^{-5}
600	0.3775	0.4013	1.01×10^{-5}	1.28×10^{-5}
700	0.2054	0.228	6.00×10^{-6}	7.36×10^{-6}
800	0.0584	0.064	1.16×10^{-6}	1.20×10^{-6}

Note: All measurements taken at 500μs following the detection of the transient



$$P_{FW} = -(2\times10^{-13}x^5 - 6\times10^{-14}x^4 + 5\times10^{-7}x^3 - 0.0002x^2 + 0.05x + 5.65)$$

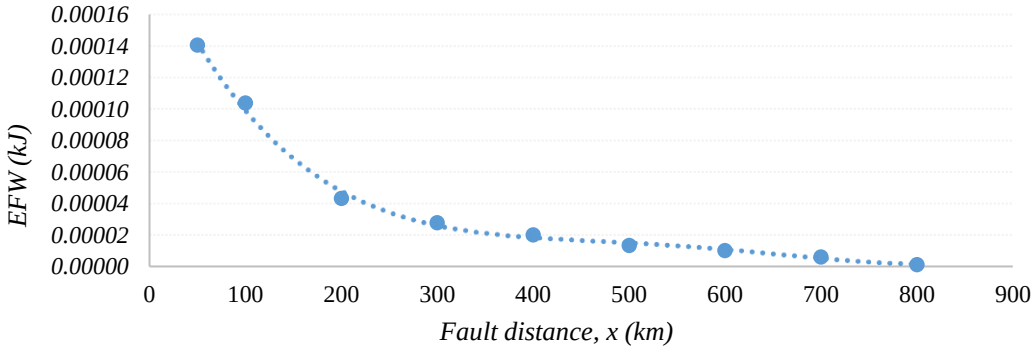
Fig. 7-28 *Section of DC grid showing varying DC side inductance*



$$P_{BW} = -(2\times10^{-13}x^5 - 6\times10^{-14}x^4 + 6\times10^{-7}x^3 - 0.0003x^2 + 0.06x + 7.23)$$

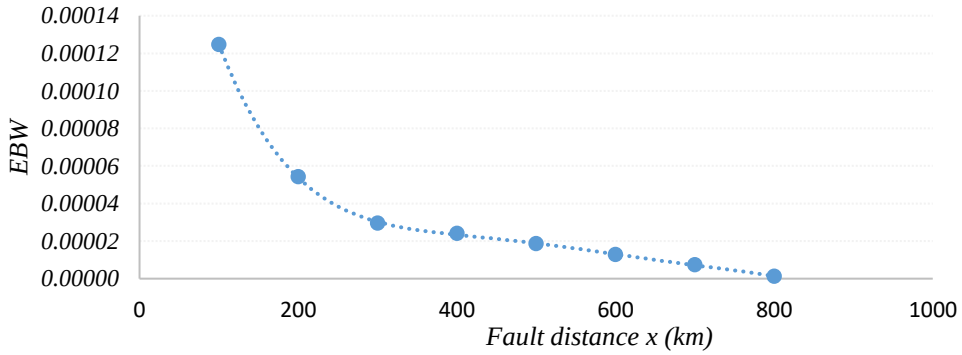
Fig. 7-29 *Section of DC grid showing varying DC side inductance*

As shown, a polynomial function of 5th degree accurately represents the variation of the travelling wave components with the fault distance. This implies that the plots can be used to estimate the protection threshold for varying cable length



$$E_{FW} = -(3 \times 10^{-19}x^2 - 3 \times 10^{-15}x^4 + 5 \times 10^{-12}x^3 - 4 \times 10^{-9}x^2 + 1 \times 10^{-6}x + 0.0002)$$

Fig. 7-30 *Section of DC grid showing varying DC side inductance*



$$E_{BW} = -(5 \times 10^{-18}x^5 - 1 \times 10^{-14}x^4 + 2 \times 10^{-11}x^3 - 9 \times 10^{-9}x^2 + 2 \times 10^{-6}x + 0.0003)$$

Fig. 7-31 *Section of DC grid showing varying DC side inductance*

7.6 Fault discriminative characteristics based on travelling wave – power concavity

Generally, as the fault resistance increases, the sensitivity of the protection scheme decreases. In order to improve the sensitivity of the protection scheme, the wave shape of P_{FW} for FIF and FEF was investigated to identify any distinguishing characteristics.

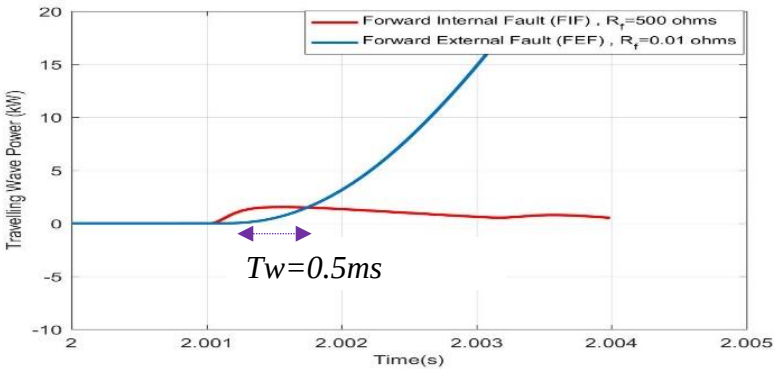
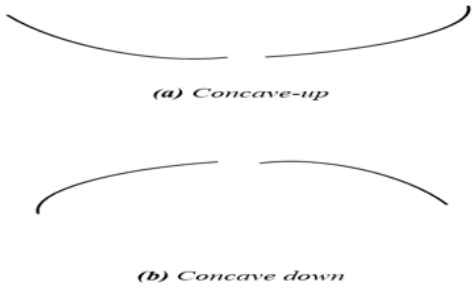


Fig. 7-32 *Critical condition for Relay R_{12} (P-G Fault)*

The plots shown in Figure 7.8 – 7.13 for all external faults with respect to the local relays indicated, shows similarity in the wave shape compared to those of internal faults Figures 7.4 and 7.5. In general, the shape of the "*travelling wave power curve"* during the measurement period (or soon after the first incident wave arrive at the relay terminal) is a parabola and therefore can be likened to a polynomial of order 2; having an equation,

$$f(x) = at^2 + bt + c\,. \qquad \textbf{(}7\text{-}10\textbf{)}$$

Generally, the coefficient of t^2, determines the shape of the parabola. For example, if $a > 0$, (or positive), the parabola has a minimum point and tends to open upwards, and is regarded as *concave-up*. However, if this is less than 0, the parabola has a maximum point and tends to open downward, and is regarded as *concave-down*. This is illustrated in Figure 7.33



7-33 *Concavity of a parabola*

Clearly, the sign of the second derivative reveals the information about its concavity. Considering Figure 7.33a, the first derivative $df(x)/dt$ is increasing as a function of time, therefore df/dt is an increasing function of *t*. Since the derivative of an increasing function is positive, the second derivative, $d^2f(x)/dt^2$ will also be positive (> 0).

In Figure 7.33(b), as *t* increases, $df(x)/dt$ decreases, therefore since the derivative of a decreasing function is negative, $d^2f(x)/dt^2$ will be negative (< 0).

7.6.1 General condition for concaving –upwards or concaving-downwards

Now, for the above condition to hold, the coefficient of the t^2 in Equation 7.10 must be positive for case 1 or Figure 7.33a (concave-up) and negative for Figure 7.33b (*Concave down*). This criteria was also adopted in this research as a criteria for distinguishing between internal and external fault.

7.6.2 Condition for internal or external fault

For an internal fault with respect to a local relay, the second derivate of the travelling wave power curve (d^2P_{FW}/dt^2) or (d^2P_{BW}/dt^2) is negative (***-VE***), whereas, this is positive (***+VE***) for an external fault.

Table 7-13 *Internal versus external fault based on wave shape concavity*

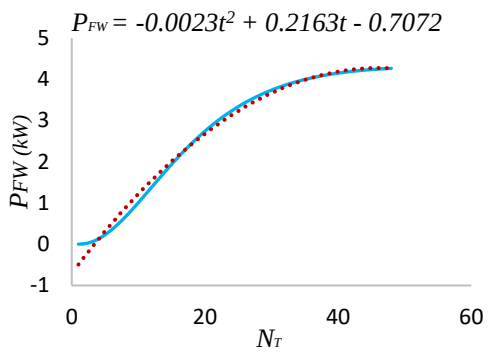
Internal fault	*External fault*
$(d^2P_{FW}/dt^2) < 1$	$(d^2P_{FW}/dt^2) > 1$

The plots of P_{FW} and P_{BW} considering the fault scenarios given in Figure 7.34 are shown in Figures 7.35 *(a)* – *(d)*; where N_T is the sampling instant. As shown, the coefficient of t^2 are negative in Figures 7.35 a & b, and hence the second derivative must be negative indicating a "*concave down*" travelling wave components. This satisfies the conditions for internal fault given in Table 7.13. However, in Figures 7c & d, the travelling wave components show a "*concaving-upwards*" characteristics, and therefore the second derivative of the function is positive, indicating an external fault.

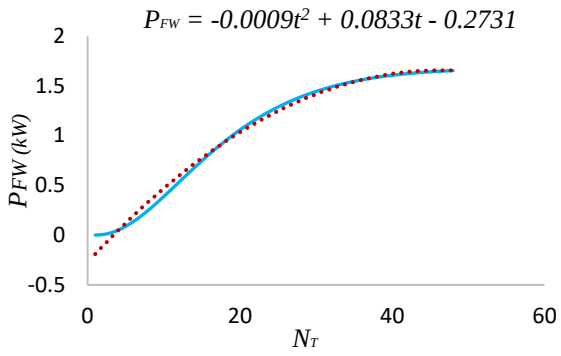
FIF : Forward internal fault FEF: Forward external fault RF: Reverse fault

Fig. 7-34 *Critical condition for Relay R_{12} (P-G Fault)*

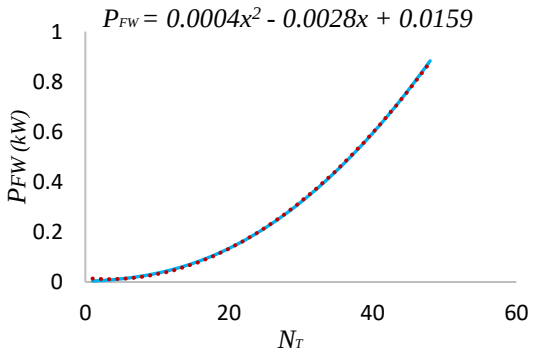
This phenomenon is largely due to the reflection and refraction characteristics at the boundary. However, transients resulting from internal faults such as *FIF* do not under go any reflection or refraction before arriving at the relay terminal.



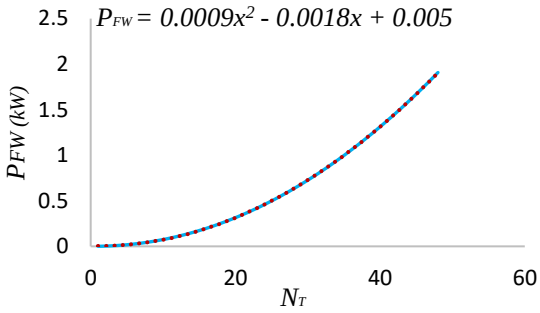
(a)FIF (R_f =300Ω)



(b) FIF (R_f =500Ω)



(c) FEF (R_f =0.01Ω)



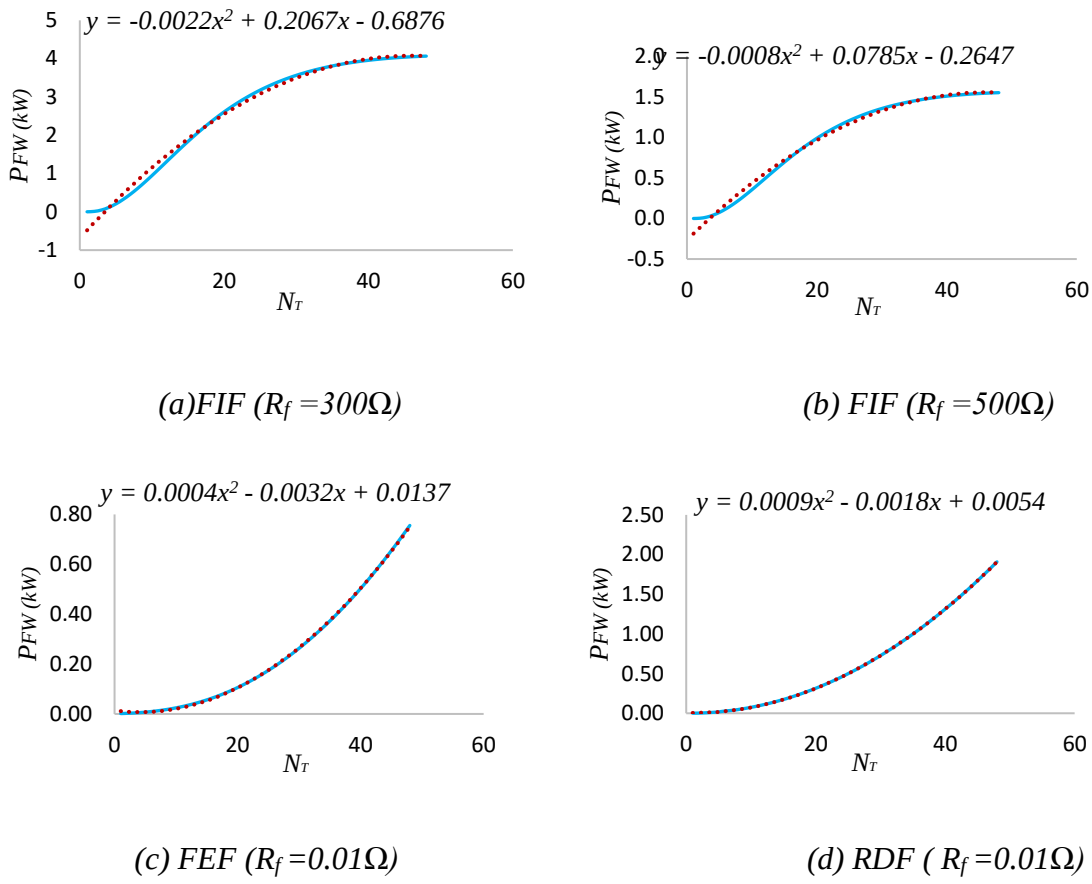
(d) RDF (R_f =0.01Ω)

Fig. 7-35 *Travelling wave power curve showing concavity of internal and external fault (P-G) for relay R_{12}*

The same scenario also holds in Figure 7.36 considering relay R_{21}.

FIF : Forward internal fault FEF: Forward external fault RF: Reverse fault

***Fig. 7-36** Critical condition for Relay R_{21} (P-G Fault)*



(a)FIF (R_f =300Ω) *(b) FIF (R_f =500Ω)*

(c) FEF (R_f =0.01Ω) *(d) RDF (R_f =0.01Ω)*

Fig. 7-37 *Travelling wave power curve showing concavity of internal and external fault (P-G) for relay R_{21}*

It can be seen that the sensitivity of the technique is not affected by the fault resistance, but largely dependent on the resulting wave shape of the travelling wave component following the detection of the transient. This is a major advantage of this technique. Other advantages are the same as those associated with the travelling wave power / energy fault discriminative criteria such as less computational burden, non-requirement of communication links, speed and among others.

Generally, following the occurrence of a fault, samples are obtained and a polynomial is generated from the waveform based on second order polynomial as in Equation 7.10. Thereafter, the second derivative with respect to time is computed. If the resulting value

is negative, then an internal fault is declared. However, if this value is positive, then the fault is an external fault.

Thus

...if $(d^2P_{FW}/dt^2) < 0$,
Fault is internal,
...else if $(d^2P_{BW}/dt^2) > 0$,
Fault is external,
End

7.7 Proposed back-up protection scheme utilising travelling wave power/ energy

Generally, the the travelling wave power ratio, P_{ratio} $(=P_{FW}/P_{BW})$ *or* E_{ratio} $(=E_{FW}/E_{BW})$ alone could be used to discriminate between internal faults, thus providing a back-up or secondary protection as in the so-called "unit-protection scheme". A typical arrangement is shown in Figure 7.38

The superimposed components of the voltage and current recorded at both relay terminals following fault inception is computed and thereafter P_{FW} and P_{BW} and *or* E_{FW} *and* E_{BW} determined.

For an internal fault, P_{ratio} and E_{ratio} at both the local and remote relay terminals must be less than unity. However, for an external fault, this ratio is less than unity at one terminal and greater than on the other terminal. These information can be determined at the local and remote end relays and the data transferred via a communication channel as shown. An optical fiber is proposed in this thesis to relay a GOOSE message.

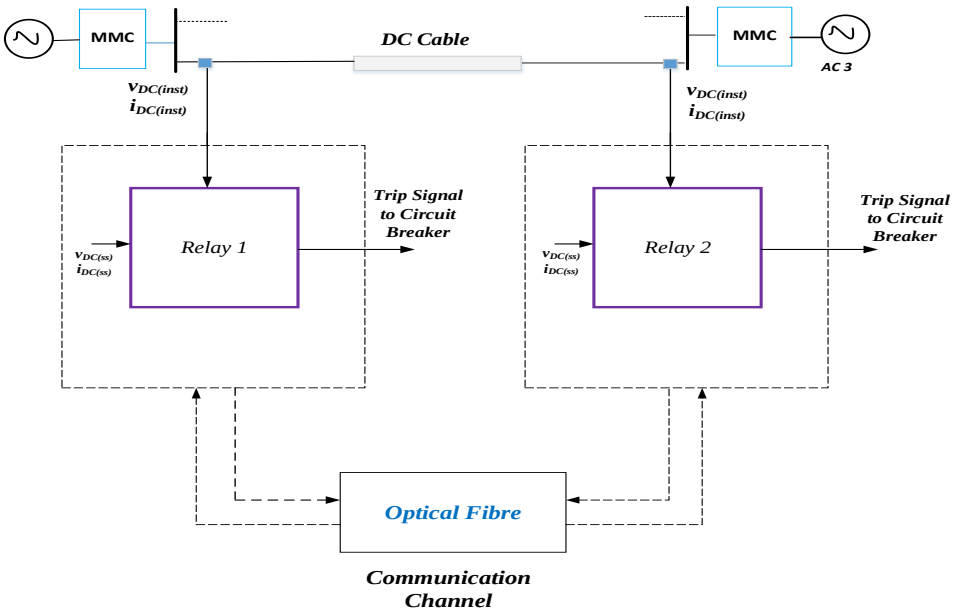


Figure 7-38 *Proposed unit TWBP scheme*

The protection algorithm for TWP is written, thus

...if $(P_{FW1}/P_{BW1}) < 1$ & $(P_{FW2}/P_{BW2}) < 1$

Fault is internal,

...else if $(P_{FW1}/P_{BW1}) < 1$ & $(P_{FW2}/P_{BW2}) > 1$

OR

$(P_{FW1}/P_{BW1}) > 1$ & $(P_{FW2}/P_{BW2}) < 1$

Fault is external,

End

The subscript, 1 and 2 represents measurements at the local and remote relays respectively. The same also holds for the *TWE*, thus

...if $(E_{FW1}/E_{BW1}) < 1$ & $(E_{FW2}/E_{BW2}) < 1$

Fault is internal,

...else if $(E_{FW1}/E_{BW1}) < 1$ & $(E_{FW2}/E_{BW2}) > 1$

OR

$(E_{FW1}/E_{BW1}) > 1$ & $(E_{FW2}/E_{BW2}) < 1$

Fault is external,

End

Clearly from the simulation results presented in sections 7.4 and 7.5, the two-relay protection strategy (or unit protection scheme) will provide discrimination between internal and external fault. Generally, it is not intended to investigate this further as the focus of this research is the development of "non-unit" protection scheme for HVDC grids.

7.8 Summary

This chapter validates the proposed novel DC line protection technique utilising travelling wave power and energy (*TWE and TWP* respectively) for application to DC grids. The proposed protection principle was validated with a full scale MMC based HVDC models utilising half bridge sub-module arrangements, and made available in PSCAD. However, some modifications were made to the model to formulate a meshed DC and to reflect the scenarios under consideration. Firstly, the ratio between the forward travelling wave power/energy (*FTWP* and *FTWE* respectively) and the backward travelling wave power/energy (*BTWP* and *BTWE* respectively) was used to provide directional discrimination. Secondly, the magnitude of the (*FTWP* and *BTWP) or (FTWE and BTWE)* for a pre-set time duration following the occurrence of fault provided discrimination for forward external fault. For an internal fault, both the ratio criteria (less than unity) and magnitude criteria exceeding a predetermined setting) must be satisfied. Clearly, the

characteristic differences between the travelling wave component between internal and external fault is largely due to the DC inductors located at the cable ends. Therefore the capability of the proposed protection scheme relies on the DC inductor. The larger the value of these inductors , the more the travelling wave is damped , but not without incuring huge amount of costs as inductors are very expensive. Therefore a compromise must have to be reached considering the cost involved and the security of power delivery.

Although the proposed relay equations were formulated based on a lossless cable model, however the results presented following validations with a full scale DC grid utilising a dependent cable model shows the effectiveness of the technique. It has been assumed in this study that all AC side faults would be significantly attenuated as the fault generated transients propagate across the converter and would be cleared by using AC side circuit breakers (not shown). Hence, they were not considered in this study. In an analogous way, the bus-bar and the DC inductor are also assumed to have a self- protecting element. The study presented in this paper assumes a DC cable fault and as such all AC side faults, converter internal faults as well as busbar faults are regarded as "*external"* with respect to all relays indicated in the first instance. In all scenarios presented, the protection technique presented provides discrimination between internal and external faults. The results presented show that the travelling wave components arriving at the relay terminal is largely dependent on the pre-fault steady state voltage as well as the fault resistance and less affected by the source parameters. Therefore, irrespective of the load current, the sensitivity of the proposed scheme is not affected. The results presented also revealed that the variation in the DC side inductance has insignificant effect on the accuracy of the protection scheme. For these reasons, the relay settings can be done off site, provided the cable parameters as well as the steady stage DC voltage are known. This eliminates the need for accurate converter modelling in order to arrive at the relay settings, hence eliminating computational burden.

The results presented also show a non-linear relationship between the travelling wave power and the fault distance, thus paving the way for a distance protection strategy. Although it is not intended to investigate this further in this research but will serve as a basis for future work. However, the derived empirical equation from the curve will serve as a basis for determining suitable relay settings for the travelling wave components for varying fault distances

The results presented also revealed a discriminative characteristic in the wave shape of the *TWP* components following the occurrence of fault. This characteristic is particularly important during long distance remote internal fault with large fault resistances where the magnitude of the resulting travelling wave components from *FEF* may exceed those of *FIF*. For this reason, the concavity of P_{FW} was used as a basis for fault detection. For an internal fault, the resulting wave shape of P_{FW} exhibits a *concave-downwards* parabolic curve whereas, it exhibits a *concave-upwards* parabola for an external fault.

A two-relay protection strategy relying on communication between the local and remote end relay was also proposed For an internal fault, P_{ratio} and E_{ratio} at both the local and remote relay terminals must be less than unity. However, for an external fault, this ratio is less than unity at one terminal and greater than on the other terminal. Although, if an optical fibre communication is assumed, but the integrity of the channel remains a major issue. It is not intended to investigate this further as the goal of this research is to develop a non-unit protection scheme. Generally, it will be a suitable back-up protection scheme

Generally, the simulation results revealed that the main fault characteristics are embedded in the travelling wave components (voltage and accompanying current wave) and extracting these components for fault identification has proven very reliable. In physical terms, the voltage and current travelling waves are two different components of the same "*wave of energy*" propagating along a transmission line following an abrupt injection.

Key advantages of this technique are as follows.

- It is fast in operation as it utilises the characteristics of the first incident wave arriving at the relay terminals
- It is a non-unit protection hence no communication delays are incurred
- The accuracy of the proposed scheme is not affected by oscillations
- The discrimination between internal and external faults can be achieved within $500\mu s$ following fault inception.
- As it time domain based, it does not require complex computational DSP techniques and or filters.
- As the computational burden is low, it will require less minimum resources, thus saving cost.

To further investigate the suitability of the proposed *TWBP* principles for its suitability in practical applications as well as its potential for real world applications, two proof of concept (*P-o-C*) experimental platforms were developed. They are the Arduino-Microcontroller experimental platform and the LabVIEW/Compact-RIO experimental platform.

The findings of the experiment carried out are presented in Chapter 8.

Chapter 8

8 Proof-of-Concept (P-o-C) implementation of the proposed travelling wave based protection (TWBP) technique

8.1 Introduction

This chapter presents the results of the implementation of the proposed TWBP technique as per proof of concept (P-o-C). For this purpose, two experimental platforms were developed. The first was based on low cost "*Arduino UNO ATmega328 Microcontroller"* experimental platform whilst the second was a more robust LabView Compact RIO experimental platform. The findings and results obtained are presented hereunder.

8.2 P-o-C implementation using Arduino UNO Microcontroller

The algorithm was implemented on an *Arduino UNO Microcontroller* as per rapid control prototyping. This was made possible by using the MATLAB® support package for Arduino® hardware. This platform enables MATLAB® to interactively communicate with the Arduino board, and see the results from I/O instructions and results viewed immediately without the need to compile it. An advantage is that it creates flexibility in the use of this platform, since the algorithm can be easily edited and modified to arrive at suitable settings.

8.2.1 The Experimental Set-up

The experimental set-up comprises the hardware and software. As shown in Figure 8.1, the hardware consists of a computer, an Arduino® *UNO ATmega328* Microcontroller board and LED; together with other accessories such as bread board and connection leads. Communication between the computer and the Arduino board was established by using a USB cable as shown. The software consists of a MATLAB® support package for Arduino® hardware.

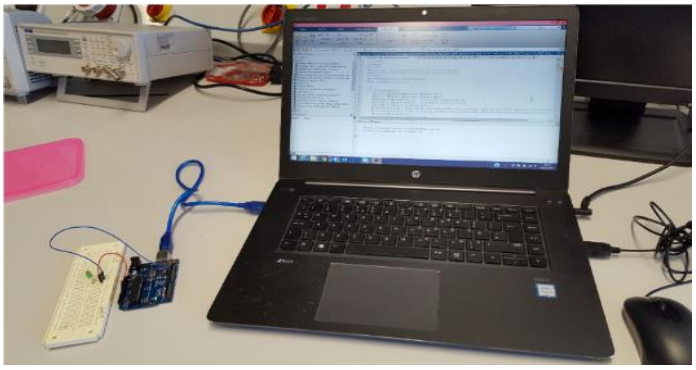


Fig. 8-1 *Experimental set-up of the P-o-C implementation on an Arduino board*

Generally, an Arduino is an open-source electronic platform based on easy to use hardware and software with the capability of fast prototyping of control algorithms and for stand-alone applications.

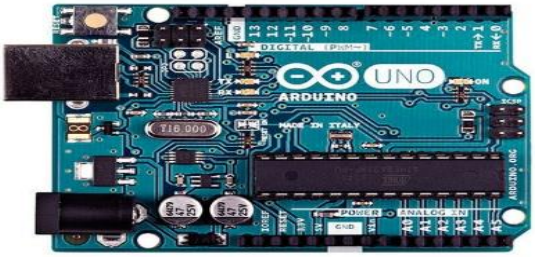


Fig. 8-2. *The Arduino UNO ATmega328 Microcontroller*

Arduino boards are able to read inputs, such as a sensor or an analogue signal stored in the form of data from a MATLAB work space and display an outputs such as activating a relay or an LED. This is usually made possible by sending sets of instructions to the micro-controller on the board. As shown in Figure 8.2, it has 14 digital input/output pins (6 of them can be used as Pulse Width Modulation outputs), and 6 analogue inputs. Details of the technical specifications as well as the description of the different parts are given in Appendix 8.1.

8.2.2 Programming the Micro-Controller

The algorithm implementation involves evaluating the derived algebraic expressions in Chapter 6 on the Arduino Board. This is as given in Equations 6.17 and 6.18 for the TWP (P_{FW} and P_{BW} respectively); as well as Equations 6.33 and 6.34 for the TWE (E_{FW} and E_{BW} respectively). As in section 7, the test signals used were obtained from PSCAD simulations as per Figure 7.1. For the sake of simplicity, only the plots obtained considering relay R_{12} of Figure 7.26. However as is presented in the preceding section, this scenario is representative of the critical conditions of the relay. The resulting data (current and voltage) from the PSCAD simulations were stored in the MATLAB work space and read by the Arduino board. An internal fault is declared by sending a trip signal via a digital output pin of the Arduino board unto which an LED is connected. The results are stored in the MATLAB workspace and also displayed in the form of waveforms (Figure 8.4). In general, the algorithm for the relay based on the TWP can be expressed as:

If

$$\frac{P_{FW}}{P_{BW}} < 1 \ and \ P_{FW} \ > P_{FW}(set),$$

```
WriteDigitalPin (a, 'D12', 1)
else
WriteDigitalPin (a, 'D12', 0)
End.
```

For TWE,

If

$$\frac{E_{FW}}{E_{BW}} < 1 \ and \ E_{FW} > E_{FW}(set),$$

```
WriteDigitalPin (a, 'D12', 1)
else
WriteDigitalPin (a, 'D12', 0)
End.
```

"a" is the Arduino board

"D12" indicates pin No 12 of the Arduino board unto which the LED was connected

"1" indicates a digital output "ON"

"0" indicates a digital output "OFF"

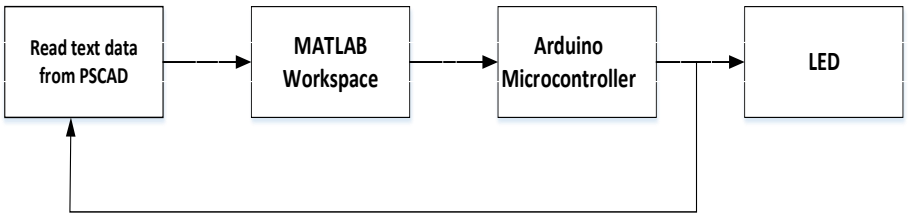
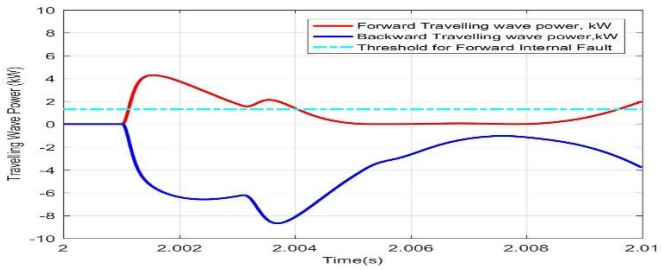
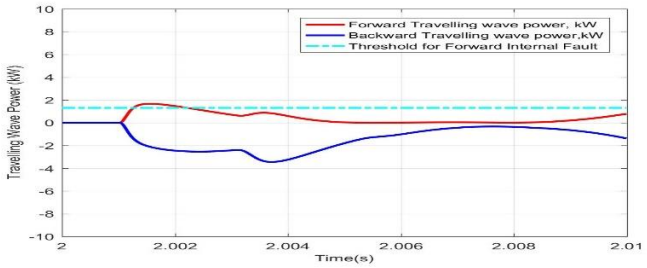


Fig. 8-3. *Block diagram of P-o-C platform using MATLAB – Arduino experimental platform*

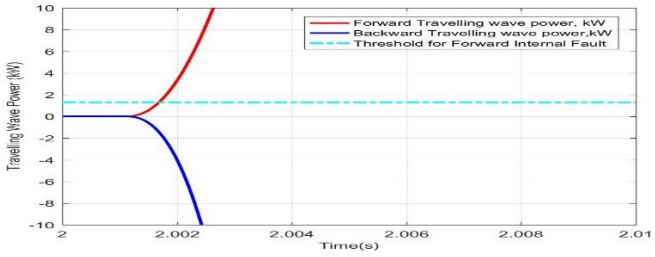
The complete MATLAB code is presented in Appendix A8.2. The threshold is the same as those used in section 7.5. The results and waveforms obtained are consistent with those obtained in chapter 7. In all cases, the LED glows for internal fault, but not glow for external faults.



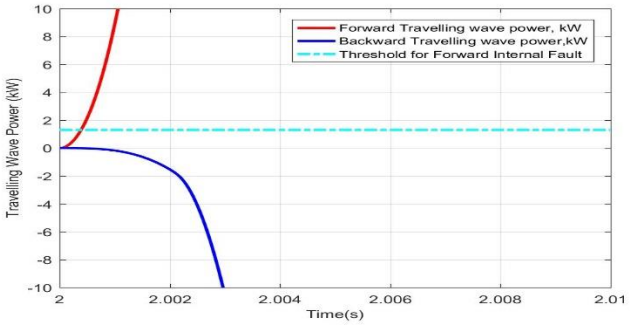
(a) Forward Internal fault, R_f =300Ω



(b) Forward Internal fault, R_f =500Ω



(c) Forward Eternal fault, R_f =0.01Ω



(d) Reverse fault, R_f =0.01 Ω

Fig. 8-4. *Plots of PFW and PBW obtained from the Arduino Experimental text bed*

The plots shown in Figure 8.4 are the results obtained for the entire simulation period. In each case, the travelling wave power components as well as the energies developed were

calculated. However, measurements taken for the controller decisions were taken during the first *500μs* following the application of the fault. All results obtained were consistent with those of Chapter 7. However, in this case the controller sent a digital output "1" (thus lighting an LED) for an internal fault whereas a digital output "0" was sent for all external faults.

8.3 P-o-C implementation using LabVIEW/Compact-RIO Platform

An experimental test bed based on LabVIEW/FPGA was also set up for the purpose of investigating the practicability of the proposed protection principle. As in section 8.1, the simulation results from PSCAD was exported to and stored in a text file, in a *Tab Delimited* format. Thereafter the data was imported into the LabVIEW work space using the "*read from spreadsheet"* function as shown in Figure 8.7. These data are the voltage (V_{DC}) and current (i_{DC}), recorded at the relay terminals as per the HVDC grid text model shown in Figure 7.26. For simplicity, only cable section 1 is considered, and with R_{12} being the reference relay. Generally, and as in Table 7.7 – 7.10, this scenario is a representative of other cable sections on the grid.

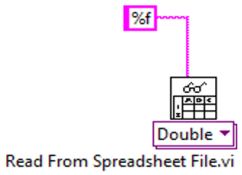


Fig. 8-5 *LabVIEW read from spreadsheet function*

8.3.1 The experimental set-up

A pictorial view of the CRIO is shown in Figure 8.6. As shown, it comprises the main parts, the real time module or controller and the Field Programmable Gate Array (FPGA)

module, unto which and external connection is made via the chassis. The module consist of 8 CRIO I/O modules for direct connection to either a scope or an industrial sensors/actuators.

A communication is established with the host PC using an Ethernet cable. *Generally*, the CRIO Controller combines a real-time processor, the user-programmable FPGA, and industrial I/O, thus giving the performance and flexibility to meet desired application requirements.

(a) Chassis

(b) Modular I/O

Fig. 8-4 Pictorial view of the Compact-RIO (NI CRIO-9961)

The integrated systems couple the CRIO real-time controller with an 8-slot backplane in a single chassis which includes the user-programmable FPGA. The entire unit work with the easy-to-use NI LabVIEW graphical programming environment thus enabling the development of real-time and FPGA applications. The modular *I/Os* enable connection to the FBGA via the chassis. The I/O could be any of the following analogue input/output, digital input/output, industrial communication, synchronisation or a motion

Based on the derived traveling wave equations in Chapter 6, the TWBP algorithm was implemented on the Compact Rio. The pictorial diagram is shown in Figure 8.6.

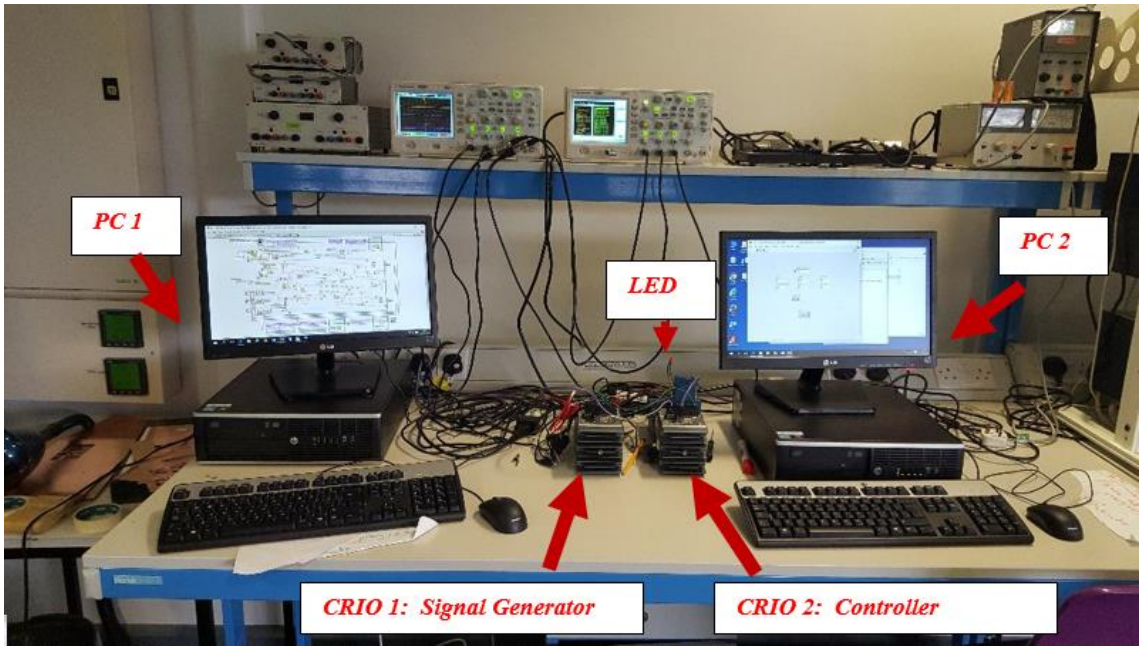
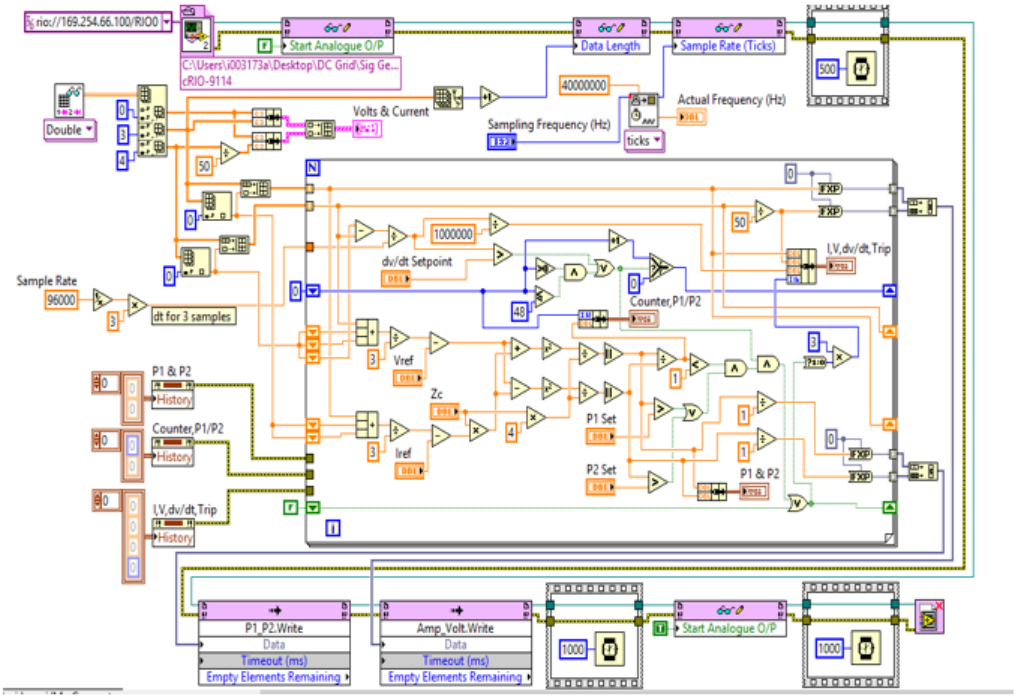
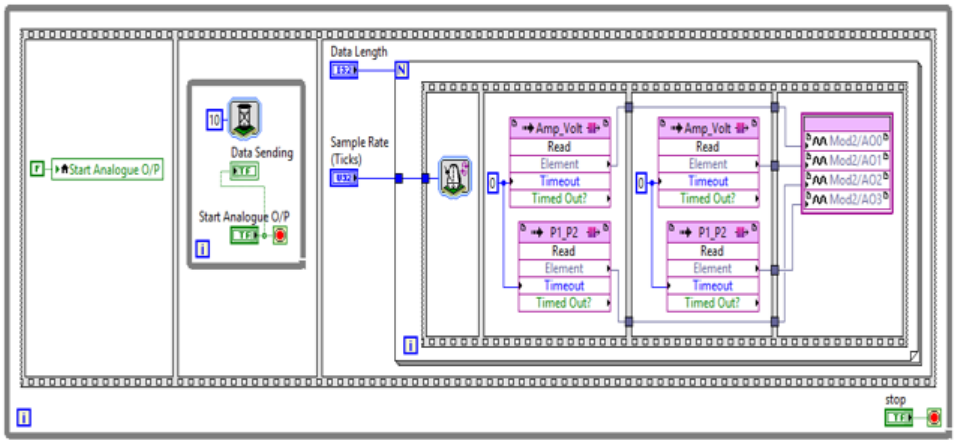


Fig. 8-6 *Pictorial diagram of the LabView Compact-RIO Experimental Set up*

The software comprises the LabView whilst the hardware comprises of two Compact RIOs (CRIO 1 and CRIO2 respectively), two Personal Computers, oscilloscope, connecting leads and other accessories as shown. CRIO 1 serves as the signal generator that simulate an analogue signal based on the data store in the real time host (PC1). The resulting analogue output from CRIO1 is sampled at *96kHz* based on a three point moving average and the resulting signal fed into CRIO2, onto which the algorithm has been implemented. A digital output which is representative of a relay trip signal is displayed via an LED connected to the digital output of CRIO2 as shown. The block diagram for the real time and FPGA implementation for CRIO1 and CRIO2 are shown in Figures 8.7 and 8.8 respectively.

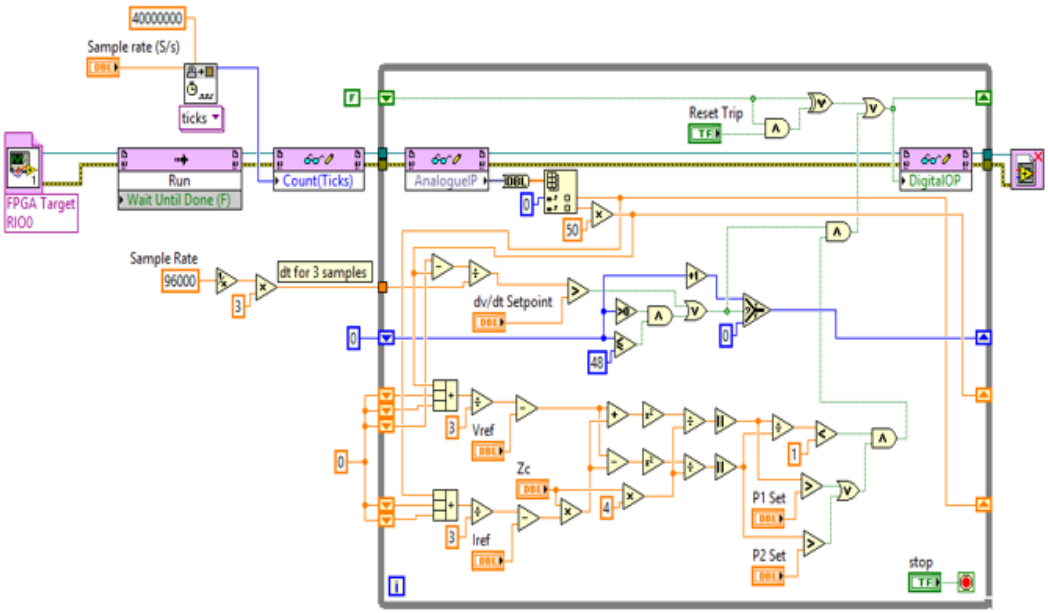


(a) Block diagram for the Real Time

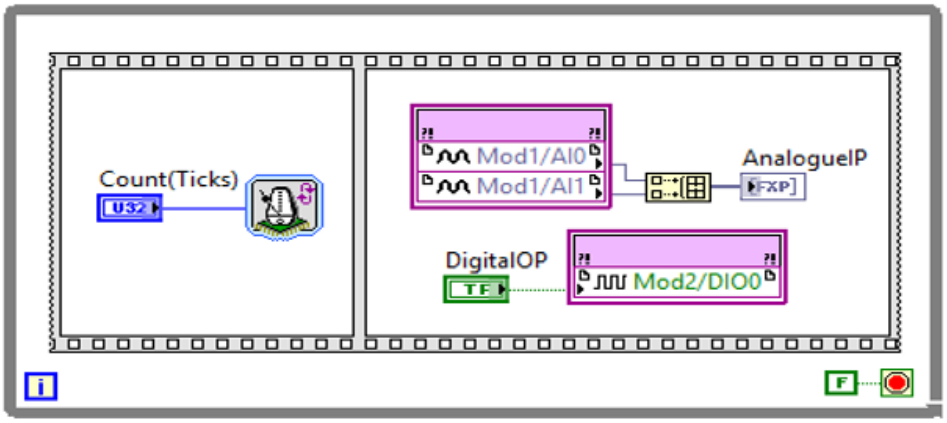


(b) Block diagram as implemented on FPGA

***Fig. 8.7** Implementation on CRIO 1 (Analogue Generator)*



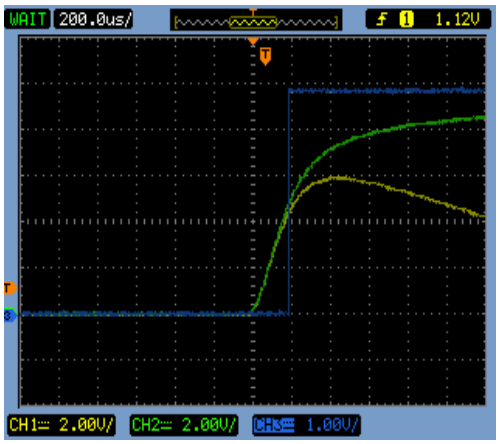
(a) Block diagram for the Real time



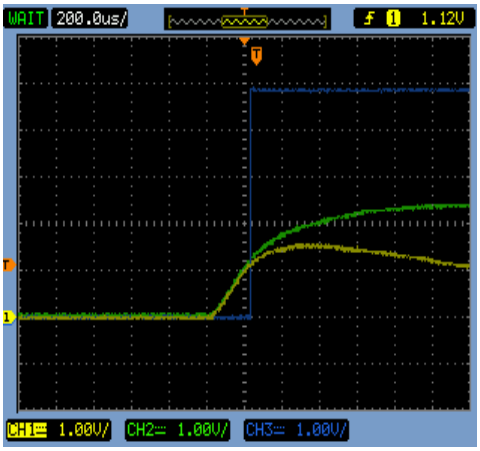
***(b)** Block diagram as implemented on the FPGA*

***Fig. 8.8** Implementation on CRIO 1 (Analogue Generator)*

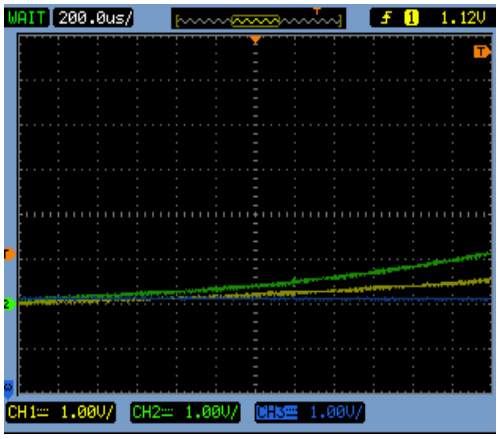
The resulting plots obtained as well as the controller action following the application of the fault are presented in Figure 8.9 *a-d*. In each case, the magnitude of P_{FW} and P_{BW} were calculated. The response of the controller following the application of the fault is also shown.



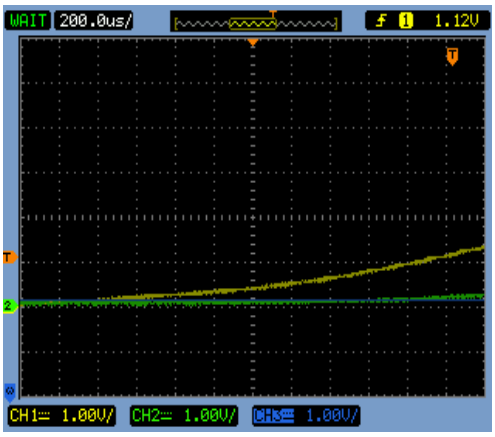
(a) *Forward Internal fault, R_f =300Ω(1div=1kW)*



(b) *Forward Internal fault, R_f =500Ω (1div=1kW)*



(c) *Forward external fault, R_f =0.01Ω (1div=50kW)*



(d) *Reverse fault, R_f =0.01Ω(1div=50kW)*

Green: Backward travelling wave power, PBW
Yellow: Backward travelling wave power, PBW
Blue: Relay tripping signal

Fig. 8.8 *Snap shot of the calculated travelling wave power components*

Generally, all plots (Figure 8.10 – 8.13) are consistent with the conditions given in Table 6.2 as per ratio and magnitude criteria. Thus for a FDF, P_{FW} is less than P_{BW} whilst P_{FW} is greater than P_{BW} for RDF. Furthermore, for a FIF, the magnitude of P_{FW} and P_{BW} during the measuring period exceeds that for a FEF. The protection threshold is the same as those used in section 7 (Table 7.2); *PFW = 1.5kW, PBW=1.8kW*. Generally, once the pre-set time duration is exceeded (500μs in this study), any measurement made is not used for fault identification since the travelling wave is assumed to be damped after this period. As in section 7.5, the *dv/dt* starting element was set at *1V/μs.*

Generally for all internal faults, the travelling wave power components exceeds their respective thresholds (Figures 8.8a &b) whereas for external faults, the components will be below their threshold and hence no trip signal will be sent to the relay (Figures 8.8c&d).

Chapter 9

9 Conclusions and future work

9.1 Conclusions

This chapter concludes the research. The key contributions as well as possible research direction for future studies are also presented.

9.2 Conclusions

The availability of fast fault detection algorithms is a prerequisite for the secure and reliable operation of Multi-terminal HVDC systems (or DC grids). This thesis presents a novel time domain protection technique for application to HVDC grids. The technique utilises the power and energy of the forward and backward travelling waves produced by a fault to distinguish between internal and external faults. Key advantages of the proposed techniques are:

- It is fast in operation as it utilises the character of the first incident wave arriving at the relay terminals hence no communication delays
- The accuracy of the proposed scheme is not affected by oscillations in the voltage or current profile.

- The discrimination between internal and external faults can be achieved within *1ms* following fault inception
- As it is time domain based, it does not require complex computational technique and DSP techniques.
- It will require less hardware resources, thus saving cost and time.
- The proposed *unit* scheme is suitable as a back up protection.

9.3 Author's contributions and achievements

Extensive literature review was carried out to study the state of art in DC line protection. The findings were reported and presented during progress review meetings at the collaborating company in the form of progress report. Fault characterisation was carried out on DC traction systems to investigate the characteristic foot prints of DC line fault current. Extensive fault characterisation was also carried out considering wider cases of fault scenarios on a full scale MMC based HVDC Meshed Grid.

The following were investigated -

- Characteristic differences between a Pole-to-Pole (P-P) and Pole-to-Ground (P-G) faults.
- Effect of Varying fault distances on the current and voltage profile following the occurrence of DC short circuit
- Varying fault resistances on the current and voltage profile following the occurrence of DC short circuit
- Effect of boundary characteristics such as the DC link inductors on the current and voltage profile following the occurrence of DC short circuit

Following fault characterisation on DC traction systems and HVDC systems the protection technique utilising current derivative (or *di/dt*) was extensively evaluated. The

studies carried on *di/dt* revealed some limitations in adopting it for the protection of HVDC grids. This includes oscillation in the fault current profile as well as the requirement of long time window, thereby making it inadequate for the protection of DC lines. These findings were disseminated at 13th IET International Conference on Development in Power System Protection (DPSP), Edinburgh.

Extensive study and further literature search led to the investigation of travelling wave based protection principles developed for HVAC systems as well as those proposed for two – terminal HVDC systems. Thereafter, a novel "*time domain DC line protection technique*" was developed. The protection technique utilises the power and energy of a travelling wave following the occurrence of a fault to discriminate between internal and external fault with respect to a local relay.

Generally, the following novel protection principles and techniques have been proposed and therefore forms part of the original contributions made in this research.

- Directional comparison technique utilising "traveling wave power"
- Directional comparison technique utilising "travelling wave energy"
- Internal fault identification technique utilising "travelling wave power"
- Internal fault identification technique utilising "travelling wave energy"
- Internal fault identification technique utilising "travelling wave power concavity"
- A backup (unit) protection technique utilising "travelling wave power / energy".

The protection algorithms were implemented in MATLAB and validated based on PSCAD/EMTDC simulations considering a full scale MMC-based HVDC grid test model made available by Manitober HVDC Research. Following this, two experimental

platforms were developed as per proof-of-concep. One platform utilises the Arduino UNO micro-controller whilst the seacond is based on LABView Compact RIO experimental platform. This was done to investigate the suitability of the proposed algorithm for practical applications (when fully deployed to a micro-controller based relay). All results obtained for the different fault scenarios were consistent with those obtained from simulations. The results obtained demostrated the effctivenetss of the protection algorithm. From the results presented, the proposed protection scheme satisfies the requirement of stability, sensitivity , speed of operation and reliabilty as per protection requirement for DC grid.

It should be noted that the capability of the proposed protection technique is largely dependent of the DC inductors placed at the cable ends. These inductors provides attenuation for the high frequency transient components resulting from an external fault which helps to provide discrimination between internal and external fault. These inductors are representative of the inductor incorporated with HVDC breakers.

Generally, HVDC grids bring new opportunities but the studies carried out revealed that a robust and intelligent fault detection algorithm is required to guarantee its full realisation. The results presented in this study revealed that the proposed algorithm can reliably protect the grid. Although the protection algorithms were formulated based on lossless cable parameters, the results presented based on validation on the frequency dependent full scale DC grid models shows the suitability. It is hopeful that the outcome of this research does not only contribute to the discussions involving the development of DC grids but serves as a basis for further research involving DC line protection algorithms. Some proposals for future work are enumerated hereunder.

9.4 Future work

There is no gainsaying the fact that this research has open new research areas involving HVDC grid protection. In the light of this, the following is proposed as future work.

- Full deployment of the protection algorithm onto a micro-processor based relay; and subsequently implementing it on a real time digital simulator (RTD)
- Further investigate the relationship between the travelling wave power and distance to the fault. This would ultimately pave the way for a distance protection strategy since the travelling wave power for a pre-set time duration following the arrival of the first incident wave at the relay terminal is directly proportional to the fault.
- Investigate the effect of the converter operation on the proposed protection technique. This will ensure that the protection scheme does not operate during normal converter operation
- The proposed protection technique utilising travelling wave power concavity can be further investigated and implemented. The main advantage of this technique is that it relies on the wave shape of the resulting travelling wave power curve, hence can accurately and reliably distinguish between long distance remote internal fault with large fault resistances and a forward external fault with very low resistance. Methods utilising pattern recognition can be a suitable research direction in this regard.
- Although it was assumed in this thesis that the effect of lightning would not have any appreciable effect on the protection algorithms since underground DC cables were used. The effect of lightning considering transmission lines can further be investigated.
- Further studies shall also be carried out to investigate the effect of noise on the proposed protection algorithm.

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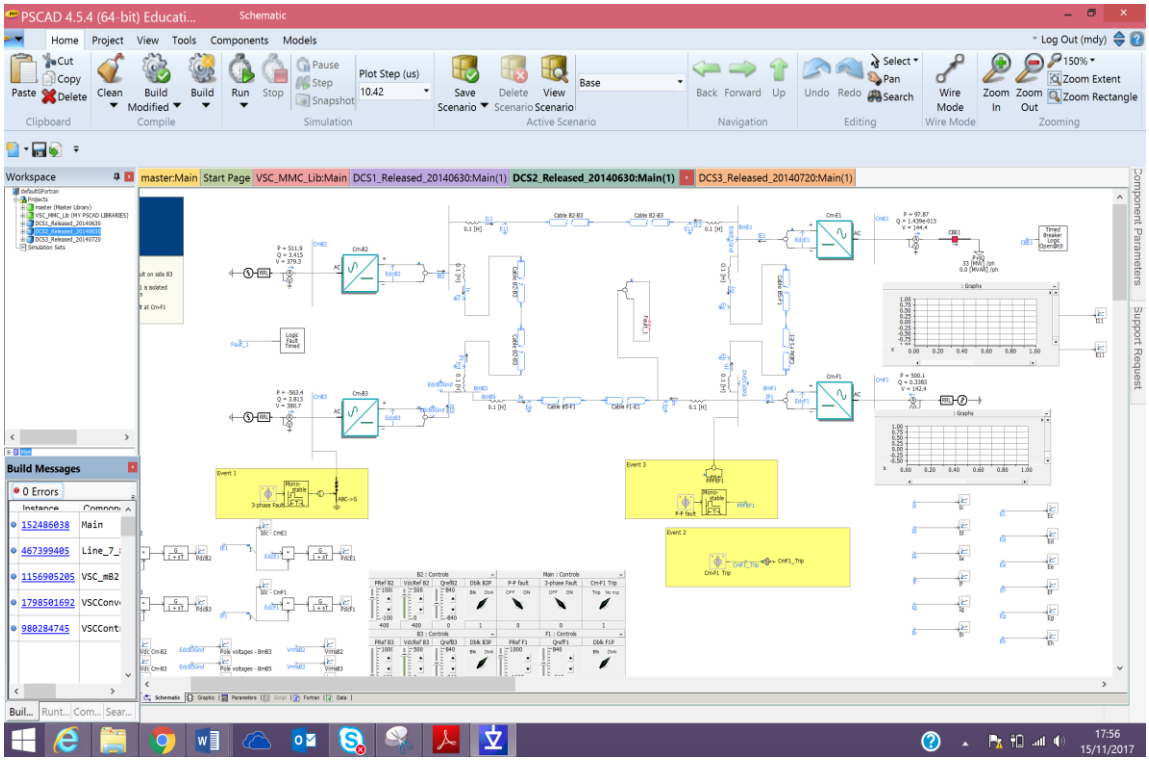
Appendix A5

A5.1 PSCAD Model of MMC-Based four terminal HVDC Grid



Appendix A7

A7.1 The Matlab Code for the Protection Algorithm

```
clc; clear;
Ts=0.1e-3;
data = xlsread('Sensitivity_R12');
t=data(:,26);

%RELAY INPUT PARAMETERS
Vdc_ss = 198.5;  %steady state DC voltage (or Reference voltage)
Idc_ss = -1.03; %steady state DC Current (or Reference Current)
Zc = 23;       %surge Impedance
Thr=1.5*(ones(10000,1));  %Threshold for Forward internal Fault


%THREE POINT MOVING AVERAGE FILTER
 for k=2:length(data)-1;
   Idc_tr(k)=(data(k-1,27)+data(k,27)+data(k+1,27))/3; % Obtain
Sampled current based on moving average filter
   Vdc_tr(k)=(data(k-1,28)+data(k,28)+data(k+1,28))/3; % Obtain
Sampled voltage based on moving average filter
   data_1=[Idc_tr' Vdc_tr'];% Create a Matrix for the filtered current
and voltage signal
 end

 %STARTING UNIT
 for w=2:length(data_1)-1
     derv_V(w)=(data_1(w+1,2)-data_1(w,2))/Ts;
     t2(w)=t(w);
 end

t2_t=t2';
dev_V=derv_V';
dv=abs(dev_V);
data_2=[t2_t dv];
[r,c]=size(data_2);
j=1;
for m=1:r
  if dv(m)>Thr  %Ensures the Relay remain Stable during starting
    delta_Vdc(j)=Vdc_tr(m)-Vdc_ss;   %Increamental change in Voltage
    delta_Idc(j)=Idc_tr(m)-Idc_ss;   %Increamental change in Current

Pf(j)=(1/(4*Zc))*((delta_Vdc(j)^2)+(2*delta_Idc(j)*Zc*delta_Vdc(j))+(d
elta_Idc(j)*Zc)^2); %Power Developed by Forward Travelling Wave
    Pr(j)=(-1/(4*Zc))*((delta_Vdc(j)^2)-
(2*delta_Idc(j)*Zc*delta_Vdc(j))+(delta_Idc(j)*Zc)^2); %Power
Developed by Reverse Travelling Wave
    P_ratio(j)=Pf(j)/Pr(j);
     t1(j)=t2_t(m);
    Thrr(j)=Thr(j);  %PROTECTION THRESHOLD
        if j==1000    %TAKE FEW SAMPLES AS PER TRAVELLING WAVE
PRINCIPLES (Transient may damped in 1ms following abrubt injection)
            break
        end
        j=j+1;
```

```
 else
     delta_Vdc(j)=0;
     delta_Idc(j)=0;
     Pf(j)=0;
     Pr(j)=0;
     t1(j)=0;
     Thrr(j)=0;
 end
end

%RELAY DECISION
P_f=Pf';
P_r=Pr';
Thrr_1=Thrr';
Table=[t1' P_f P_r Thrr_1];
[rr,cc]=size(Table);
for z=1:length(Pf);
    if  Pf(z)>=Thr2;
         disp('Fault is Forward Internal, Relay Operate')
%     else
%          disp('Healthy System, Relay is Stable')
     end
end
Table=[P_f P_r];
time=t1';
subplot(1,1,1)
plot(t1,P_f,'r',t1,P_r,'b',t1,Thrr_1,'c-
.','LineWidth',2);set(gca,'fontsize',10);  grid on; ylabel('Travelling
Wave Power (kW)','FontSize', 10);xlabel('Time(s)','FontSize', 10);
axis([2 2.01 -1E1 1E1]);legend('Forward Travelling wave power,
kW','Backward Travelling wave power,kW','Threshold for Forward
Internal
Fault','Location','northeast','Orientation','vertical');text(2.501,2e4
,'Relay R1','Color','k','FontSize',10)

%% Determine Energy Contents of the forward and reverse Travelling
Wave.
SS=size(Pf);
for z=1:SS;
    Ef_tra=0.0001*(0.5*(Pf(1)+Pf(end))+sum(Pf)-Pf(1)-
Pf(end));%Trapezoidal Algorithm
    A=sum(Pf(2:2:length(Pf)))*2;
    B=sum(Pf(1:2:length(Pf)))*4;
    C=1.04e-5/3;
    Ef_symp=C*(A+B-Pf(1))%Simpson's Algorithm

end
ST=size(Pr);
for z=1:ST;
    Er_tra=0.00001*(0.5*(Pr(1)+Pr(end))+sum(Pr)-Pr(1)-
Pr(end));%Trapezoidal Algorithm
    A=sum(Pr(2:2:length(Pr)))*2;
    B=sum(Pr(1:2:length(Pr)))*4;
    C=1.04e-5/3;
    Er_symp=C*(A+B-Pr(1))%Simpson's Algorithm
end
```

Appendix A8

A8.1 Specification of Arduino UNO Microcontroller

Technical specs

Microcontroller	ATmega328P
Operating Voltage	5V
Input Voltage (recommended)	7-12V
Input Voltage (limit)	6-20V
Digital I/O Pins	14 (of which 6 provide PWM output)
PWM Digital I/O Pins	6
Analog Input Pins	6
DC Current per I/O Pin	20 mA
DC Current for 3.3V Pin	50 mA
Flash Memory	32 KB (ATmega328P) of which 0.5 KB used by bootloader
SRAM	2 KB (ATmega328P)
EEPROM	1 KB (ATmega328P)
Clock Speed	16 MHz
LED_BUILTIN	13
Length	68.6 mm
Width	53.4 mm
Weight	25 g

The Arduino UNO board has five analogue input pins A0 through A5. These pins can read the signal from an analogue sensor like the humidity sensor or temperature sensor and convert it into a digital value that can be read by the microprocessor. It has 14 digital I/O pins (15) (of which 6 provide PWM (Pulse Width Modulation) output. These pins can also be configured as input digital pins reading logical values (0 or 1) or as digital output pins driving modules like LEDs, relays, etc. The pins labelled "~" can be also used to generate PWM.

A8.2 The Matlab code Implemented on Arduino UNO Micro controller

```
clc; clear;                 %clear the work space
a=arduino;                  %declare Arduino object
Ts=1/(96e3);                %Sampling period (Sampling frequency=96kHz
Vdc_ss = 198;               %steady state DC voltage (or Reference
voltage (kV))
Idc_ss =-0.95;              %steady state DC Current (or Reference
Current (kA))
Zc = 23;                    %surge Impedance of cable
Thr=100000*(ones(100,1)); %Generates threshold
data = xlsread('Scenarios_1');% Read voltages and current from a text
file

j=2;
for k=2:length(data)-1
    Idc_tr(k)=(data(k-1,2)+data(k,2)+data(k+1,2))/3; %Three Point
Moving Avarage Filter to eliminate spikes in current
    Vdc_tr(k)=(data(k-1,3)+data(k,3)+data(k+1,3))/3; %Three Point
Moving Average Filter to eliminate spikes in voltage
    delta_Vdc(k)=Vdc_tr(k)-Vdc_ss;   %Increamental change in Voltage
    delta_Idc(k)=Idc_tr(k)-Idc_ss;   %Increamental change in Current
    derv_V(k)=-1*(data(k+1,2)-data(k,2))/Ts;% Determine the voltage
derivative


Pf(k)=(1/(4*Zc))*((delta_Vdc(k)^2)+(2*delta_Idc(k)*Zc*delta_Vdc(k))+(d
elta_Idc(k)*Zc)^2); %Power Developed by Forward Travelling Wave
    Pr(k)=(-1/(4*Zc))*((delta_Vdc(k)^2)-
(2*delta_Idc(k)*Zc*delta_Vdc(k))+(delta_Idc(k)*Zc)^2);%Power Developed
by Reverse Travelling Wave
    Pf_Pr_Ratio(k)=Pf(k)/Pr(k); %Calcutae the travelling wave power
ratio

    if (derv_V(k)>2)&&(Pf_Pr_Ratio(k)<1); %Setting conditions
(derv_V=starting unit; then check for ratio.)
        Pf_tp(j)=Pf(k);
        Pr_tp(j)=Pr(k);
        if j==48    %TAKE FEW SAMPLES AS PER TRAVELLING WAVE
PRINCIPLES (Transient may damped in 1ms following abrubt injection)
            break
        end
         j=j+1;
          SAMPLE=[Pf_tp' Pr_tp'];
         for mm=1:length(Pf_tp);
             if Pf_tp(mm)>=1
                 writeDigitalPin(a, 'D12', 1) %send a trip signal to
pin 12 of the Arduino to light an LED
             else
           writeDigitalPin(a, 'D12', 0)

             end
         end
    end

end
```