Fault Detection in Multi-Terminal Modular Multilevel Converter (MMC) Based High Voltage DC (HVDC) Transmission System

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***Abstract*: A Multi-Terminal High Voltage Direct Current (MT-HVDC) network is being considered for utilising the full potential of offshore wind power whereas its realisation is currently being hampered by protection issues. In this paper, a protection strategy for future DC grids based on Modular Multilevel Converter (MMC) based HVDC system is presented. Firstly, a fault detection technique based on initial di/dt measurement is presented and thereafter protection strategies for future DC grids are presented. The fault detection technique presented is based on estimating the initial rate of rise of the current, $IRRC$ (di/dt) at fault inception using measured data and thereafter calculating the line inductance. The calculated line inductance is compared with a setting value to determine whether or not a fault has occurred, thus paving the way for a distance protection strategy. Simulations were carried out using Matlab/SIMULINK for varying fault distances. The results obtained show the validity of the technique in detecting and locating DC side short circuits. An advantage of this technique is that it relies only on information from the local end terminal and as such, no communication channel is required, hence satisfying the protection requirement of fast fault detection and location technique for MT-HVDC systems.**

***Index Terms*: Offshore Wind Power, Multi-terminal HVDC System, Modular Multilevel Converter, DC side short circuits, Fault detection and Location, DC Line Protection.**

I. INTRODUCTION

Protection issues remain a major challenge in realising Multi-terminal High Voltage DC (MT-HVDC) networks[1]–[5]. Protection algorithms for MT-HVDC system will have to operate faster than those used in the conventional HVAC system; typically less than $1ms$ from fault inception[5],[6]. Another issue is selectivity; as only the faulty section should be isolated in the event of a fault. This constitutes a major challenge considering the complex nature of the grid (Fig.1) as well as the anticipated length of the cables. Several attempts have been made in the recent past to develop a DC line protection technique for a MT-HVDC network[1], [5], [7]–[10] yet much work still needs to be done. This paper attempts to contribute to this discussion by developing a DC line protection technique that will be capable of protecting the network from faults and disturbances. The rest of the paper is structured as follows. Section 2 gives a brief overview of the protection issues that have hindered the development of suitable protection algorithms for MT-HVDC network while section 3 presents the topological structure and the operating principle of MMC. Section 4 presents the DC short circuit analysis of MMC- HVDC system and also the developed equivalent circuit for the calculation of the fault current. The concept of distance protection for HVDC system is introduced in section 5 while section 6 presents a protection strategy for future DC grids. The paper concludes with section 7 and with some guidelines for future studies.

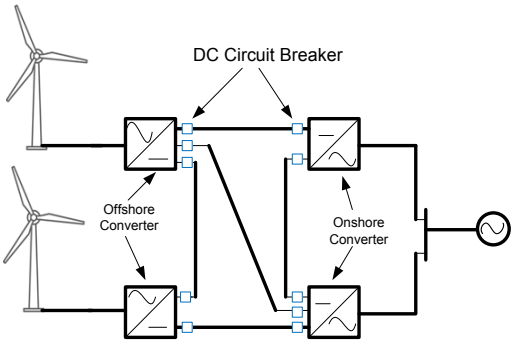


Fig. 1. Conceptual Four Terminal MT-HVDC Network

II. PROTECTION ISSUES

Existing protection techniques for two terminal HVDC systems utilising AC side circuit breakers is not suitable for MT- HVDC systems since it does not provide DC protection. MT-HVDC systems are based on Voltage Source Converters (VSC) due to their advantages over the conventional thyristor based HVDC systems such as black start capability and ability to independently control active and reactive power. Also, the power flow in VSCs HVDC system can be reversed without changing the voltage polarity. These features have made VSCs the best option for MT-HVDC. However, VSC based HVDC are susceptible to DC side faults due to the discharge of current from the DC side capacitance during fault conditions[11]. This discharge together with the low inductance of the DC network results in a sudden rise in the fault current which can reach damaging levels in less than a quarter of a cycle; hence the requirement of a fast fault detection and isolation technique.

Recent trends in VSC technology led to the development of the Modular Multilevel Converter (MMC). MMC can either be of half bridge or full bridge type. The half-bridge type is

not able to block fault current and is referred to as a *non-blocking* converter. It therefore requires DC side circuit breakers to be placed at both ends of the line or cable. The full-bridge type is able to block fault current by converter control and is referred to as *blocking* converter and as such does not require DC side breakers; but would still require new protection algorithms for fault location. Details are well documented in[1], [12]. The study presented here is based on a half bridge type MMC and as such DC circuit breakers will be required. Although early attempts made in the development of HVDC breakers suffers some setbacks due to some technical issues [13] [14], remarkable achievements have been made in its development.[15] [16].

III. MODULAR MULTILEVEL CONVERTER (MMC)

MMC consists of a large number of identical but individually controllable sub-modules (*SM*s), which forms its basic building block (Fig. 2). Some of the key features of the MMC includes modular design, low switching frequency resulting in reduced losses compared to 2 or 3 - level VSC converters, flexibility in control of voltage level, reduced harmonics and reduced dv/dt on the AC side [17]–[19]. A *SM* (Fig. 2b) consists of two IGBT switches S_1 and S_2 , and a capacitor C_{SM}. V_{SM} is the instantaneous voltage of the capacitor. The function of S_1 and S_2 is to either *"insert" or "by-pass"* the capacitor in the current path thus allowing the production of two voltage levels. When S_1 is *on* and S_2 is *off*, the *SM* is in the "ON" state and $V_{SM} = V_{CM}$; conversely, when S_1 is *off* and S_2 is *on*, the *SM* is in the "OFF" state and $V_{SM} = 0$. when both switches are "*off",* the *SM* is said to be "*blocked*". Details can be found in [20]–[22]. As shown in Fig. 2a, an MMC comprises two multi - valves in each phase, namely the upper and lower multi-valve. These multi-valves are collectively referred to as phase modules (or Legs). Each of the multi-valves has an equal number of *SMs;* and the *SM* capacitor is usually charged to a voltage V_{CM} . V_{DC} is the voltage across the converter terminal and N_{SM} is the number of *SMs* in a multi-valve (or arm). The net output voltage is the sum of the individual output voltages from each *SM* in a multi-valve. Under steady state conditions, the total DC voltage in each converter leg equals the nominal DC link voltage; and only half of the *SMs* in each arm are connected to their respective capacitor (or inserted) during normal operating conditions[23]. The arm reactor ($\boldsymbol{L_{arm}}$) is designed to eliminate the circulating current resulting from capacitor voltage imbalances and also limit the rate of rise of DC faults during DC side short circuits [24], [25]. Its value depends on V_{CM}, the modulation technique, the switching frequency or any other controller that may be present for suppressing the circulating current. Details are well documented in [24], [26]

IV. DC SHORT CIRCUIT ANALYSIS OF MMC HVDC SYSTEMS.

Different types of faults can occur in MMC based HVDC systems. They include *SM* faults, AC side faults and DC side faults. However, this study shall focus on the DC side faults. DC side faults can either be a pole to ground or pole to pole. In a pole to ground fault, the AC grounding point and the point of occurrence of the fault constitutes the fault path way. In the pole to pole fault, the converter terminals and the point of occurrence of the faults constitute the fault pathway [11].

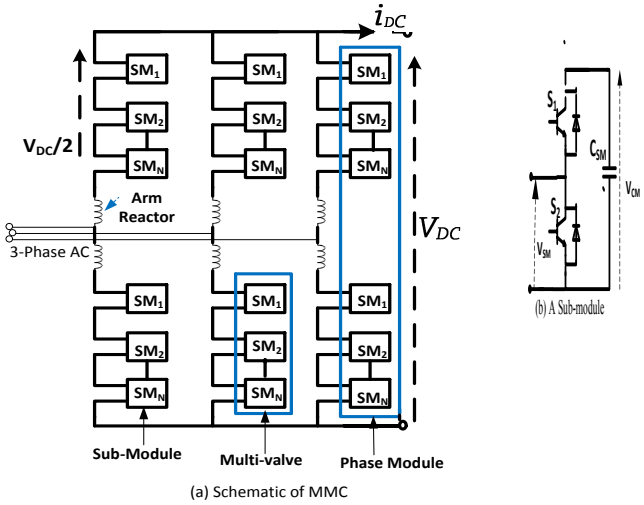


Fig. 2 Topological Structure of MMC[21]

$$\boldsymbol{V_{SM}} = \frac{\boldsymbol{V_{DC}}}{\boldsymbol{N_{SM}}} \quad (1)$$

Generally, two major factors influence the fault current profile. They are the earthing arrangements and the converter configurations together with its control system as documented in[1], [4]. Although a pole to pole fault would rarely occur, but the resulting effects can be detrimental to the operation of the system as it can result in total HVDC network voltage collapse and a high magnitude of fault current[1]**.** For this reason, it shall be the focus of this study.

The equivalent circuit of a MMC operating under a pole to pole fault is shown in Fig. 3. The short circuit process consists of two stages - the capacitor discharge stage and the AC (grid-side) feeding stage. The capacitor discharge stage represents the first few milliseconds following fault inception and the current discharged from the *SMs* capacitors and the cable capacitance is the main component of the short circuit current [22], [27]. During this stage, the MMC will remain operational until it is blocked following the detection of the fault. Once the IGBTs are blocked, the AC side current will continue to flow through the free wheel diode[28]. If the fault is not cleared, the current overshoot resulting from the discharge of current from the *SM* capacitance would be continually supported by the AC current flowing through the freewheeling diode even if the capacitor discharging current decays to zero.

In order to satisfy the protection requirement of MT-HVDC, the equivalent circuit of the MMC during the capacitor discharge stage shall be used in this study to determine whether or not a DC side short circuit has occurred.

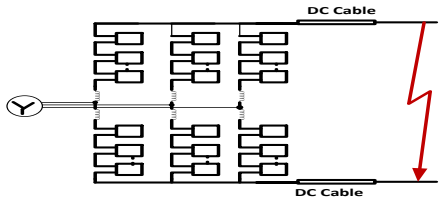


Fig. 3. Equivalent Circuit of MMC during Pole-to-Pole Fault

Equivalent Circuit of MMC during Capacitor Discharge Stage:
The parameters for the equivalent circuit of a MMC during the capacitor discharge have been derived as documented in [18] and the converter equivalent circuit is shown in Fig. 4. However, as the capacitive discharge period is short, the equivalent capacitive voltage can regarded as constant during this period [27].

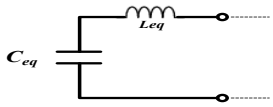


Fig. 4. *LC* Equivalent Circuit of a MMC

$$L_{eq} = {}^{2}/_{3}\,L_{arm} \quad and \quad C_{eq} = 6\,\frac{C_{SM}}{N_{SM}}$$

This was also reported in [29] where the fault current profile was the same for the first few milliseconds from fault inception irrespective of the values of the *SM* capacitances. A study was also carried out and is presented in Fig. 6.

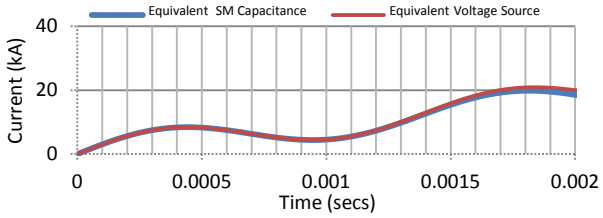


Fig.5. Predicted Fault current resulting from Equivalent Voltage source and Equivalent Capacitance during pole to pole fault

For this reason, the equivalent *SM* capacitances are replaced by their equivalent DC voltage (Fig. 6) during the capacitor discharge stage. The DC cable was modeled using the *Pi* - cable model. R_C, L_C and C_C are the cable resistance, inductance and capacitance respectively. The converter and cable parameters were obtained from [18] and are presented in Table 1. Simulations were carried using Matlab/Simulink for various fault distances and the result obtained is presented in Fig.7. As shown in Fig 7, there is an oscillation in the fault current profile especially for short distance fault. This oscillation is attributed to the cable capacitance and was found to reduce with increasing fault distance. A 100*mH* low resistance reactor which is typical of a HVDC breaker and as used in [10] was placed in series with the DC cable to damp this effect, thus making the total series inductance, $\boldsymbol{L_T}$ to be

$$\boldsymbol{L_{eq} + L_S + L_C}$$

L_{eq} = Converter Equivalent arm inductance
L_s = DC smoothing inductor (*100mH*)

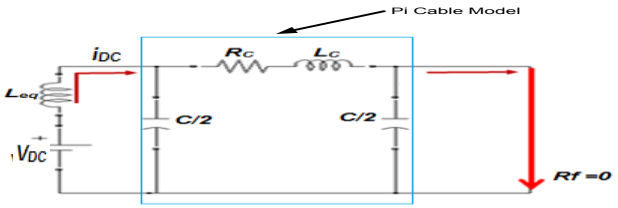


Fig. **6**. Proposed Model for MMC during Capacitor Discharge Stage

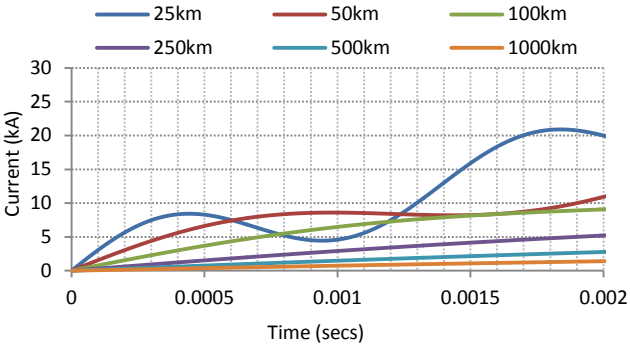


Fig. 7. Fault Current Profile for varying fault distance during Capacitor discharge

Simulations were also carried out for varying fault distance and the resulting plots shown is shown in Fig. 8.

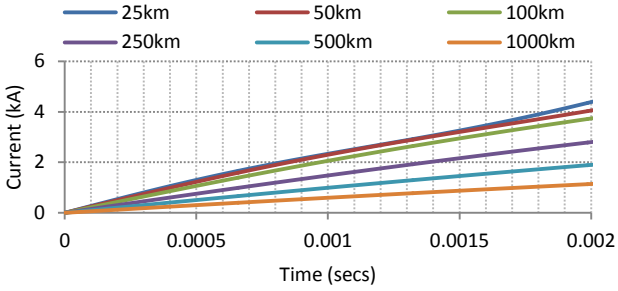


Fig. 8. Fault Current Profile for varying fault distances during Capacitor discharge with a DC Smoothing Reactor

From Fig. 8 and neglecting the effect of the cable resistance at the instant of fault inception, the initial rate of rise of the fault current from the time of fault inception up till time, *t = 0.5ms* was estimated and thereafter the system inductance calculated. Thus

$$\boldsymbol{|di_{DC}/dt|}_{\,t\to 0} = \frac{\boldsymbol{V_{DC}}}{\boldsymbol{L_T{}'}}$$

$|di_{DC}/dt|_{\,t\to 0}$ =initial rate of rise of the fault current, *IRRC*.

$$\boldsymbol{L_T{}'} = \frac{\boldsymbol{V_{DC}}}{\boldsymbol{IRRC}} \qquad (2)$$

$L_T{}'$ = Calculated system inductance.

The results obtained (Fig. 9 and Table 2) show the suitability of the technique in estimating the system inductance from the initial rate of rise of the fault current. However, in order to guarantee a high degree of accuracy, *IRRC* must be measured very close to a time, *t =0.*

TABLE 1.
CONVERTER AND CABLE PARAMETERS [18]

Rated capacity of converter transformer	$420\ MVA$
Nominal ratio of converter transformer	$220kV/150kV$
Leakage Reactance of Converter transformers	10.5%
AC side impedance	$5+5j\ \Omega$
Line-to-neutral Nominal AC voltage	$220kV$
DC Link voltage	$+/-150kV$
Converter nominal power	$300MW$
Number of Submodules per arm (N_{SM})	20
Submodule capacitor	$765\mu F$
Arm inductor	$33.42mH$
DC cable resistance, R_C	$2\times10^{-2}\Omega/km$
DC cable inductance, L_C	$1.91\times10^{-4}H/km$
DC cable capacitance, C_C	$2.95\times10^{-7}F/km$

The additional DC smoothing reactor added to the line was found to increase the accuracy of the technique. Generally, the larger the smoothing reactor, the smoother the fault current profile but at the expense of cost. This implies that a compromise will have to be reached, taken into consideration the accuracy and the additional cost posed by the smoothing inductor. The results presented in Figs.10 and 11 respectively also show that the *IRRC* is independent of the cable resistance; in anticipation that it can be measured within *0.5ms* from the fault inception. This was also reported in the work presented in [30]; and therefore implies that the technique also be applicable to high resistance or arc fault such as in the case of ground faults. An advantage of this technique is a non-unit system of distance protection and as such no information from remote end converter station is required. This eliminates the requirement of communication channel.

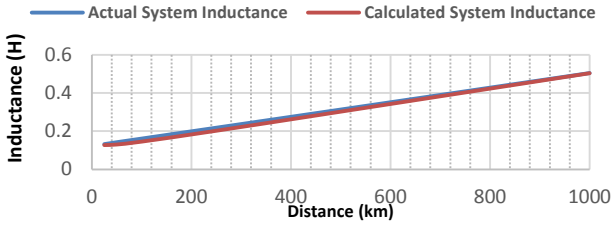


Fig. 9 Actual Versus Calculated System Inductance

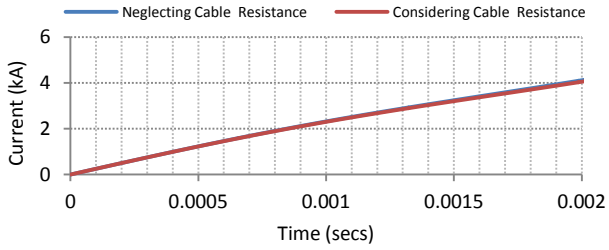


Fig. 10 Comparison of Fault Current Profile with and without cable resistance (50km)

Now, if it is assumed that the cable inductance is proportional to the distance and considering Fig.9 and Table 2, the traditional distance protection philosophy as applied to the conventional HVAC system can be adapted for HVDC system.

TABLE 2.
INDUCTANCE AND DISTANCE

Fault Distance (km)	L_T (H) *(Actual)*	$L_T' = \frac{V_{DC}}{IRRC}$ (H) (Estimated)	% Error
25	0.132	0.127	3.788
50	0.142	0.130	8.450
100	0.161	0.145	9.938
250	0.218	0.202	7.340
500	0.313	0.302	3.514
1000	0.504	0.503	0.198

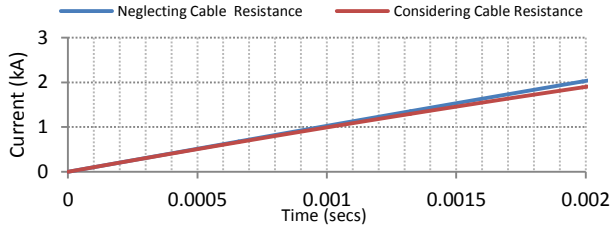


Fig. 11 Comparison of Fault Current Profile with and without cable resistance (500km)

V. DISTANCE PROTECTION

In the traditional distance protection philosophy applicable to AC systems, a fault is detected when the calculated impedance is less than the reach point impedance. Generally, the impedance of a transmission line is proportional to its length. Therefore, a relay capable of measuring the impedance of a line up to a predetermined point termed the reach point or the setting point will be needed. Such a relay is referred to as a distance relay and is designed to operate only for faults occurring between the relaying point and the selected reach or setting point. By so doing, it can provide discrimination for faults occurring in different sections. The principle involves the division of measured voltage at the relaying point by the measured current to calculate the impedance seen by the relay (Fig 12.).

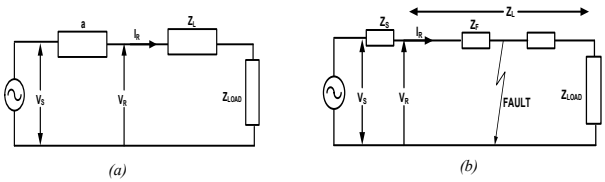


Fig. 12 Impedance Measured by a Distance Relay.

Z_S = source impedance behind the relaying point,
V_S = source voltage,
Z_L = line impedance of the total line length that is protected by the distance relay,
Z_{LOAD} = impedance of the connected load.

I_R = current measured by the relay's current transformer
V_R = voltage measured by the relay's voltage transformer

From Fig. 12a, $Z_R = \frac{V_R}{I_R} = Z_L + Z_{LOAD}$ (3)

From Fig. 1b, $Z_R = \frac{V_R}{I_R} = Z_f$ (4)

When $Z_f < Z$, the relay operates;

Z_f = Fault impedance.

Z = Reach or setting point impedance

If the measured impedance is less than the setting impedance, then the fault exists on the line in between the relay and the setting or reach point. In the case of DC systems as line inductance is proportional to the length of the line, a similar protection strategy can be developed based on the line inductance. A fault is detected when the calculated loop inductance is less than the reach point inductance. With the knowledge of inductance per unit length, a decrease in the calculated inductance will effectively shorten the fault distance. Thus,

$L_f < L_{set}$, detect Fault; else, restrain.

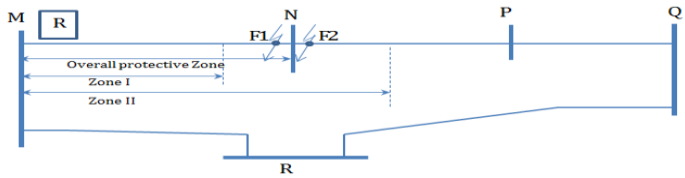
$$L_f = L_T{}' - (Ls + L_{arm}) \quad (5)$$

L_f = measured inductance to the fault
L_{set} = setting inductance

VI. PROTECTION STRATEGY FOR MT-HVDC NETWORK

In general, the protection principles for DC networks are likely to follow those applicable to AC networks. The main principles are selectivity, speed of operation, sensitivity and security. However, these four principles are in contradiction with each other and as such a compromise will have to be reached but without prejudice to security and reliability of power delivery.

Whether or not to use unit protection or non-unit protection should also be considered. The unit protection is based on information and measurement from both ends while the non-unit type is based on information and measurement from local end. The information refers to the current and voltage. In the conventional AC systems, the over-current and distance protection belong to the former while the current differential and phase comparison belong to the latter. Clearly, the unit protection will not meet the requirement for MT-HVDC protection since it will require communication between two ends incurring time delay as well as increasing cost. The non-unit protection is therefore a preferred option for MT-HVDC network but not without some limitations since it cannot guarantee absolute selectivity [6]. For example as shown in Fig 13, and as per the principle of zoning, the trip signal for a non-unit protection will be delayed when a fault occur outside zone 1, yet no significant difference in the measured impedance for faults F_1 and F_2. Faults occurring in zone 2 are cleared by the zone 2 protection, but with a time delay (typically 0.5s) to avoid nuisance trips for faults occurring in the overlapping zone between zone 1 and 2.



Zone 1: 80 – 85% of protected line; Zone 2: Remaining 15 – 20% up till 120% of protected line

Fig. 13 Typical AC Grid Protection Scheme [6]

Therefore in the context of future MT-HVDC grids, the non-unit protection may be the main protection and unit protection may serve as a backup.

Transient based versus steady state based protection:

Protection algorithms based on the characteristic difference of transient voltage and/or current signals are referred to as transient based protection while those based on the signature of steady state voltage and current signals are called steady state based protection. Considering that isolating the faulty section in MT-HVDC grids need to be very fast, the transient based algorithm should be adopted. However, the time window should contain sufficient samples for detecting/ characterising the fault. Also, the sampling rate for DC grid protection is 96 kHz, that is, 96 samples per millisecond. If the requirement of the total fault clearance time is less than $5ms$, then the window length should be less than $0.5ms$ as well. Using the above sampling rate, the decision of internal or external fault can be made by an algorithm less than 0.5ms, which can meet the requirement of DC fault clearance[6].

New Protection Scheme for DC grid

Based on the above, the following have been proposed.

For primary Protection:

Transient based directional overcurrent relay or Transient based distance Relay + Transient based high speed remote trip detection.
(*Without relying on communication between the ends*)

For back-up Protection:

Transient current differential or Transient based directional comparison unit protection or transient based distance unit +Aided scheme[1]
(With communication between the ends).

A typical three terminal MT-HVDC network, in which the above protection strategy can be implemented, is shown in Fig. 14. As shown, there are DC breakers located on both ends of the DC lines. Protection R_1 and R_2 are responsible for protecting the line MN, R_3 and R_4 for line MR, and R_5 and R_6 for line NR. For fault in overlapping zone of both R_1 and R_2,

[1] There are 2 types of distance protection scheme. They are (a) Basic scheme (b) Distance + aided scheme. Aided scheme means the local end distance relay operation is accelerated by the received information (via communication) from the remote end distance relay.

directional distance protection will trip to isolate the fault. For fault in zone 1 of R_1 and outside of R_2, directional distance R_1 will trip first, and thereafter R_2, having detecting the breaker tripping by transient remote trip detection. In a similar way, for fault in zone 1 of R_2 and outside of R_1, directional distance R_2 will trip first, and thereafter R_1, having detecting the breaker tripping by transient remote trip detection. The same principle holds for the remaining line sections.

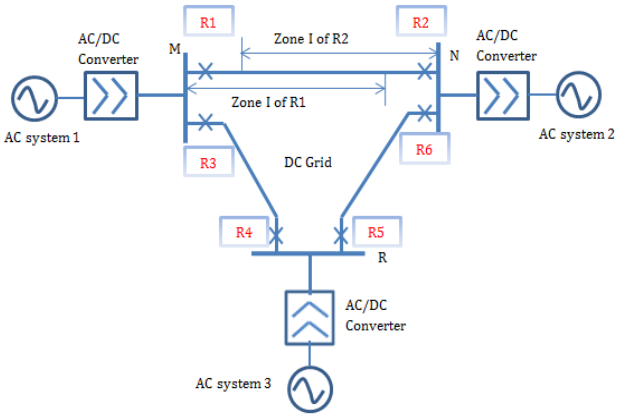


Fig. 14 Typical AC Grid Protection Scheme [6]

In general, the algorithms will follow the same philosophy applicable to the traditional HVAC system. In particular, they should be re-constructed from the algorithm based on fundamental frequency component to those based on transient components of the fault generated signal.

VII CONCLUSIONS

This paper has provided an insight into the protection strategies for DC grid with a view to developing a protection algorithms capable of meeting its protection requirement. In the first instance, a technique for detecting a DC side short circuit in a MMC based HVDC system was developed. Particular attention was given to the pole to pole fault since it is more severe. The technique is based on measuring the initial rate of rise of current (*IRRC)* at fault inception and thereafter estimating the line inductance. A fault is detected when the calculated line inductance is less than the estimated (setting) inductance. A protection strategy for DC grids was also proposed. In general and in order to meet the protection requirement of fast fault detection in MT-HVDC systems, new algorithms should be developed. It is hopeful that this paper will contribute to the discussions towards the development of DC grids.

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