AN INVESTIGATION OF AN ENERGY DIVERTING CONVERTER FOR HVDC APPLICATIONS

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To Paul, Clara, Marta and Stéphanie. You are the light that brightens my days and keeps me going.

Ama, aita, porque sin vuestro cariño y apoyo nunca habría llegado hasta aquí.

Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text.

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Abstract

Wind power generation in Europe has experienced an unprecedented expansion fuelled by a very favourable regulatory framework promoted to fight climate change. It is currently the second largest power generation source accounting for 17% of the total energy mix and in 2016 it covered an impressive 10.4% of the total energy demand. With faster wind speeds and better availability, offshore wind farm developments have also experienced a surge in recent years. There are 12.7 GW of cumulative installed capacity with the hot spot located in the North Sea.

The grid integration of offshore wind farms has evolved to meet the requirements of recent projects, much larger in power capacity and located farther offshore. High voltage direct current (HVDC) connections using state of the art multilevel voltage source converters are now the industry standard for distant wind farms, with transmission capacities of up to 1 GW. The scale of the projects and frequent grid weakness at the onshore locations challenge transmission system operators which need to ensure the entire grid stability. Grid codes have evolved to regulate such interconnections, with a set of well specified requirements which need to be fulfilled. One such requirement is the fault ride-through capability, which defines the need for the HVDC interconnector to remain connected during onshore grid faults.

A Dynamic Braking System (DBS) is a power electronics device that provides fault ride-through capability to the HVDC interconnector by absorbing the excess energy injected to the link for the duration of the fault. This energy is commonly dissipated in a resistive element. In this way the DC over-voltage is avoided and the operation of the connected wind farms is kept undisturbed. There is a lack of knowledge in the design and implementation of such devices. Therefore four concepts put forward by industry and other researchers are studied in this work. The rating of the different components in each circuit is investigated as the basis for the comparison.

Taking into account the modular structure of AC/DC converters in HVDC stations it makes commercial sense to reuse the same modules as building blocks for the DBS. With modular structures, a good balancing of the total energy stored in the converter and its distribution among the different modules is one of the key elements. Modular DBS circuits can synthesize multilevel voltage waveforms,

allowing for advanced power modulation strategies. Two novel strategies are developed in the thesis and an accurate mathematical modelling is performed to ensure that the energy balance conditions are met for all points of operation. An overall control strategy for each of the four circuits is also developed and presented in the thesis.

A good coordination of the protective actions of the DBS and the main HVDC converters is important to ensure that no negative interactions occur. An operation strategy based on over-voltage thresholds is developed in the thesis. Accurate simulation models of the HVDC link integrating the DBS and controls are also implemented to give the required degree of confidence in the overall system behaviour. These are finally validated by a laboratory scaled-down test platform, where the control actions and the different converters are implemented in real hardware, and the correct coordination of all the elements during a fault event is experimentally tested.

The main drawback of the DBS solution usually highlighted in literature is its cost. The option of adding some extra functionality to better justify the economic investment is explored in this thesis, resulting on a multifunctional circuit named *Energy Diverting Converter (EDC)*. Two proposals including active filtering and HVDC tapping are developed in this thesis, for which two patent applications have been filed.

Acknowledgements

First and foremost, I would like to express my gratitude to my supervisor, Professor Sarath Tennakoon. This PhD would not have been possible without his guidance, support and help to overcome all the difficulties I found on the way. Secondly, many thanks to Roger Critchley, who guided my first steps in industry as a fantastic manager and ultimately made it possible and encouraged me to undertake this great challenge. My recognition to Carl Barker for the time he dedicated to this work as an industrial advisor and his encouragement to file many patents. This work would not have been possible without the financial support from Alstom and the Engineering and Physical Sciences Research Council (EPSRC).

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Finally, to my wife Stéphanie who has suffered more than anybody the sometimes not so easy years but never gave up encouraging me, a big big thank you. Paul, Marta and Clara, our three little stars, you gave me the energy to cross the finish line. And to the rest of the family, thank you all for being there.

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List of acronyms and symbols

Acronyms

AC Alternating current

ADC Analogue to digital converter

CSC Current source converter

DBS Dynamic braking system

DC Direct current

EDC Energy diverting converter

PCB Printed circuit board

EMI Electro magnetic interference

FRT Fault ride-through

HDL Hardware description language

$HVAC$ High voltage alternating current

$HVDC$ High voltage direct current

$IGBT$ Insulated gate bipolar transistor

LCC Line commutated converter

$LOVL$ Lower over-voltage limit

MMC/M^2C Modular multilevel converter

$MTDC$ Multi-terminal direct current

$MVAC$ Medium voltage alternating current

$MVDC$ Medium voltage direct current

OWF Offshore wind farm

PCB Printed circuit board

PLL Phase-locked loop

PWM Pulse-width modulation

RES Renewable energy sources

$DFIG$ Doubly fed induction generator

SI International system of units

$STATCOM$ Static synchronous compensator

SVC Static VAR compensator

TSO Transmission system operator

$UOVL$ Upper over-voltage limit

VSC Voltage source converter

$VSC - HVDC$ Voltage source converter based high voltage direct current

WTG Wind turbine generator

$XLPE$ Cross-linked polyethylene

Chapter 1

Introduction

1.1 Context

In the 1880s Nikola Tesla and Thomas Edison fought their famous *War of Currents*. The result is well known, with the alternating current (AC) winning the final battle over the direct current (DC) and, with a few exceptions, imposing itself as the technology of choice for the widespread deployment of electrical grids around the world over the next century.

Nonetheless, during the 20th century the high-voltage power conversion industry thrived, firstly using mercury arc technology in the early 1950s and later with their solid state replacement, the thyristor valves, from the late 1960s onwards. These devices facilitated the implementation of line commutated converters (LCC) to perform a high voltage AC to DC conversion. Electrical power transmission using DC experienced a resurrection, with the revolutionary high-voltage DC (HVDC) transmission representing a more economical option for bulk, long distance power transmission.

A second revolution in the HVDC market has taken place more recently, with the proposition in the early 2000s of the modular multilevel converter (MMC) concept. The first project to be commissioned using this technology was the Trans Bay Cable in 2010, a submarine DC cable transmission in the San Francisco Bay. With the MMC station power losses getting closer to those of a conventional LCC (around 1% against 0.7%), a smaller station footprint and lower cost, MMC technology has rapidly found its own place in the HVDC market, in particular for the interconnection of offshore wind.

In parallel, the commitments to reduce CO_2 emissions and fight climate change, by reaching at least a 20% renewable energy share by 2020 in Europe, have encouraged investment in renewable energy sources (RES). This has fuelled an incredibly fast deployment of offshore wind generation in Europe with the North Sea being seen as the centre of this activity.

The interconnection of offshore wind farms using submarine cables has found

in HVDC transmission a more economical alternative to conventional HVAC as the distance from shore increases. MMC has found itself as an ideally suited conversion technology for the interconnection of clusters of increasingly larger and more distant offshore wind farms. At the time of writing, 6 such HVDC connections are operational in the North Sea and 3 more are in the commissioning or construction stage, and expected to enter operation in the coming three years.

With power ratings ranging from 400 MW to 916 MW, these HVDC connectors are comparable to conventional power plants. Their integration in the national grids starts posing some basic network security and stability issues, and grid codes have evolved to regulate it. Fault ride-through is one of the principal and most challenging requirements to be observed. A dynamic braking system (DBS), which takes its name from traditional braking choppers in motor drives, is currently included within the onshore MMC station to prevent a transient over-voltage in the HVDC link during a low voltage dip in the onshore AC grid. The term energy diverting converter (EDC) was coined during this research project as a generalization of the DBS concept. An EDC can extract the totality or a fraction of the power flowing through the DC link, and provides the same over-voltage protection with some additional functionality of interest for the operation of the HVDC system.

Since 2007, GE grid solutions (former Areva T&D and Alstom Grid) has been actively engaged in the development of modular multilevel converter (MMC) solutions for the HVDC market. In February 2013 the reward to the R&D efforts arrived in the form of a contract to supply a complete MMC conversion scheme for the Dolwin 3 offshore interconnector in Germany. As part of the deliverables, a dynamic braking solution was to be included within the onshore conversion station to provide the required fault-ride through capability for the interconnector.

1.2 Aims and objectives

Therefore, this research work kicked-off with the aim to investigate the design and technical and economic application of Energy Diverting Converters with added functionality. In doing so, the following research objectives were set:

1. To compare the technical performance of different electrical circuits suitable for the implementation of a dynamic braking system.

2. To develop control and modulation techniques to regulate the power diverted from the HVDC line by each circuit.

3. To design and build a low power DC grid in order to experimentally validate the developed control system and modulation techniques.

4. To investigate the DBS performance experimentally.

5. To explore the potential to implement energy diverting converters, which include extra functionality, in order to increase the DBS attractiveness from a commercial perspective.

1.3 Organisation of the thesis

In particular, the outcomes of this work are presented in the different chapters of the thesis as follows:

Chapter 2

The chapter reviews the current technical solutions for the connection of offshore wind generation to onshore AC grids. The requirements for the integration into national AC grids of the generated power using HVDC transmission are presented, as well as a review of the existing literature on fault-ride through capability provision for such connections.

Chapter 3

The principle and operation of a DBS as well as some general concepts common to all DBS circuits are described. Four implementations of a DBS using different circuits are investigated: the HVDC chopper, the multilevel chopper, the half-bridge multilevel and the full-bridge multilevel circuits. The controlled dissipation of power in the resistive elements requires a different approach in each circuit. A suitable control methodology for each circuit is derived and explained. For the complicated stored energy balancing in the half-bridge and full-bridge circuits the use of trapezoidal modulations is explored in great detail. A comparison of the circuits in terms of device ratings, as well as a trade-off analysis are performed at the end of the chapter.

Chapter 4

In order to evaluate the performance of the four DBS circuits and proposed control strategies during a fault ride-through event, simulation models are implemented. This chapter presents the results of these simulations and comments on the technical performance of each circuit and relative merits of the different control strategies.

Chapter 5

For a more realistic experimental validation of the control strategies running in digital control hardware, a low-power test platform was built. This chapter describes its physical implementation, with the scaled-down model of an HVDC system as well as the fault triggering mechanism to physically emulate a fault ride-through event. The flexible power cell, distributed control hardware, fibre optics communication, user interface and data logging and display interfaces, all of which was specifically designed by the author for this research project, are also described.

Chapter 6

The experimental results obtained with the test platform are presented in the chapter. For each circuit, the platform settings during each test are detailed. The different waveforms, logged during a successful fault ride-through event, are displayed and discussed to validate the performance of each control strategy.

Chapter 7

This chapter explores the Energy Diverting Circuits, which integrate some extra functionality that complements the DC over-voltage mitigation. Here the HVDC tapping function has been investigated. The novel circuit topologies developed and required control techniques are also derived and explained.

Chapter 8

The last chapter concludes on the findings and contributions made by this research work. A recommendation is also made on further research opportunities arising from the work here presented.

1.4 List of publications based on this work

Based on Chapters 3 to 6

1. J. Maneiro, S. Tennakoon, C. Barker, and F. Hassan, "Energy diverting converter topologies for HVDC transmission systems," *Power Electronics and Applications (EPE), 15th European Conference on*, pp. 1–10, Sept 2013.

Based on Chapter 7

1. J. Maneiro, S. Tennakoon, and C. Barker, "Scalable shunt connected HVDC tap using the DC transformer concept," *Power Electronics and Applications*

(EPE'14-ECCE Europe), 16th European Conference on, pp. 1–10, Aug 2014. ***Received the *Outstanding young EPE member award***

2. C. Davidson, K. Dyke, J. Maneiro, D. Trainer, and N. Okaeme, "Converter circuit," Patent EP 2 834 896 (B1), May 25, 2016.

3. J. Maneiro and C. Barker, "DC/DC converter," Patent EP 2 905 885 (B1), Aug 12, 2015

1.5 Thesis contributions

The work presented in this thesis has made a number of contributions which can be summarised as follows:

Analysis of DBS circuits: The use of DBS for DC over-voltage protection had previously been presented in literature but always from a simplified perspective considering an ideal switch with a series resistor. The author provides in this work a thorough investigation on the working mechanism of four different implementations of a DBS circuit, three of them using modular multilevel structures, in sections 3.2, 3.3, 3.4 and 3.5. Control strategies, not previously disclosed in literature, have been developed in sections 3.2.1, 3.3.1, 3.4.3 and 3.5.3.

Energy balancing of modular DBS: The key aspect for operating multilevel circuits is the energy balancing. The author has developed a novel modulation strategy based on trapezoidal waveforms to operate DBS circuits using half-bridge and full-bridge cells. These are described in sections 3.4.2 and 3.5.2, where a detailed analysis of the naturally achieved energy balance is also investigated. The full derivation of the presented expressions is included in Appendix A.

Circuit dimensioning and trade-offs: The sizing of the main DBS circuit elements: number and rating of semiconductors, resistors and capacitors, which impacts the required capital expenditure, is analysed in Chapter 3. Design trade-offs, crucial to tailoring the converter design, are identified in section 3.6 for the half-bridge and full-bridge multilevel circuits. These affect the converter's performance in terms of required number of cells, capacitor size, switching frequency, EMI performance and the choice of semiconductor devices. Economical aspects are briefly discussed in section 3.7

Laboratory test platform: In order to test the designed DBS circuits under FRT conditions, a test set-up was constructed by the author as described in Chapter 5. This allowed for the testing of the DBS circuits with their control strategies implemented in real hardware. Experimental data is obtained and the proposed converter design and control strategies are validated, with all

the results presented in Chapter 6. The entire test platform was fully designed and built by the author for this research project, including PCB design and development of all the communication protocols, PC software to implement the human-machine interface and the firmware for all the control cards.

Energy Diverting Converters: The addition of extra functionalities in DBS circuits to implement EDCs had great innovation potential. The result of this work gave place to two patents [1, 2].

Based on the Marx converter principle the author develops the *Cascaded resonant DC transformer* circuit in section 7.1.1. A thorough analysis of the operation principle and component sizing for the circuit is performed in the thesis. This work resulted in a publication [3] which received the *Outstanding young EPE member award* by the European Power Electronics and Drives Association and the patent *"DC/DC converter"* [2].

Chapter 2

Review of grid integration of offshore wind farms

Global warming due to human greenhouse gas emissions is the most plausible cause behind the accelerated earth surface temperature increase and climate change experienced since the mid 20$^{\text{th}}$ century [4]. International initiatives such as the *United Nations Framework Convention on Climate Change*, the *Kyoto Protocol* and more recently the *Paris Agreements* set targets for a reduction of greenhouse gas emission and mitigation of climate change effects.

Renewable Energy Sources (RES) play a vital role to reach the goals concerning CO_2 emissions reduction. At a European level, the European Union (EU) Renewable Energy Directive, published in 2009, targets 20% of the energy needs to be supplied by RES by 2020. This figure increases to 27% under the new 2030 Framework for climate and energy [5]. These regulations have provided the perfect breeding ground for an exceptional expansion of wind and solar energy in Europe over the last decade. In 2016 for example 86% of all the EU's new installed capacity was from renewables, with a total 21.1 GW of power installed (59.2% wind and 31.8% solar). By the end of 2016, wind and solar power already accounted for 17% and 11% of the EU's total installed power mix respectively, and wind power overtook coal as the second largest form of installed generation capacity. Wind power also covered an impressive 10.4% of the total energy demand in Europe [6][1].

Even if onshore plants remain as the main type of installed wind generation capacity, offshore wind is catching up fast. In 2015 for example, offshore

[1]Wind Europe, previously known as European Wind Energy Association (EWEA), is a non-profit association gathering together manufacturers, electricity providers, research institutions and universities among others, with the goal of promoting wind power in Europe. References from this organization are used throughout the chapter to provide figures for renewable energy installation and production in Europe. The key figures have been validated with the data available at the European Statistical Office (EUROSTAT) portal: https://ec.europa.eu/eurostat

wind installations more than doubled with respect to 2014, whereas onshore installations decreased by 7.8% [7]. Allowing the use of larger turbine sizes and with stronger and steadier winds, large offshore wind farm (OWF) projects are being commissioned in Europe, with the main focus in the North Sea. This new type of installations require a complete new approach for grid interconnection. Large distances from the shore and the use of submarine cables made the industry turn towards DC transmission. HVDC interconnectors using VSC converters are now the state of the art solution for grid integration of several offshore farms with power ratings approaching now 1 GW.

However the large size of these new interconnections starts posing some basic grid security issues, and grid codes have started to be more strict concerning the operation of such large offshore wind installations. One such aspect covered by grid codes is the fault ride-through (FRT) requirement. A new range of solutions are proposed to provide such capability in HVDC interconnectors, with the dynamic braking systems (DBS) being the preferred solution in current offshore projects. The rest of the chapter gives a critical review of the current state of the technology in this area.

2.1 Offshore wind generation

The interest in offshore wind resources is steadily gaining momentum around the globe. The stronger and steadier winds available offshore translate into a higher power production: a 10% in the wind speed theoretically leads to a 33% increase in the wind power reaching the turbine blades according to relation 2.1:

$$P = \frac{1}{2}\rho A V^3 \tag{2.1}$$

Where,

- ρ: air density (kg/m^3)
- A: area covered by the turbine blades (m^2)
- V: wind speed (m/s)

Offshore wind located far from the coast does not generate any noticeable visual or noise pollution, and therefore encounters less opposition from the population. Offshore wind also presents a reduced impact to local fauna, specially concerning birds' habitat disturbance and injury. In addition, some European countries such as Germany, are running out of suitable onshore locations.

In Europe offshore wind installations have been steadily growing since the installation of the first OWF in Denmark in 1991 [8]. Fig. 2.1 shows the evolution of the installed capacity in Europe over the last two decades. By the end of 2016, 12.6 GW of offshore wind were connected to the grid in Europe, 72% located in the North sea [9]. The UK and Germany are the two leading countries in terms of installed offshore capacity with 41% and 32.5% share respectively [9]. Fig. 2.2 presents a map of all the current OWF projects in operation and under construction, where the concentration around these two countries is clearly observed.

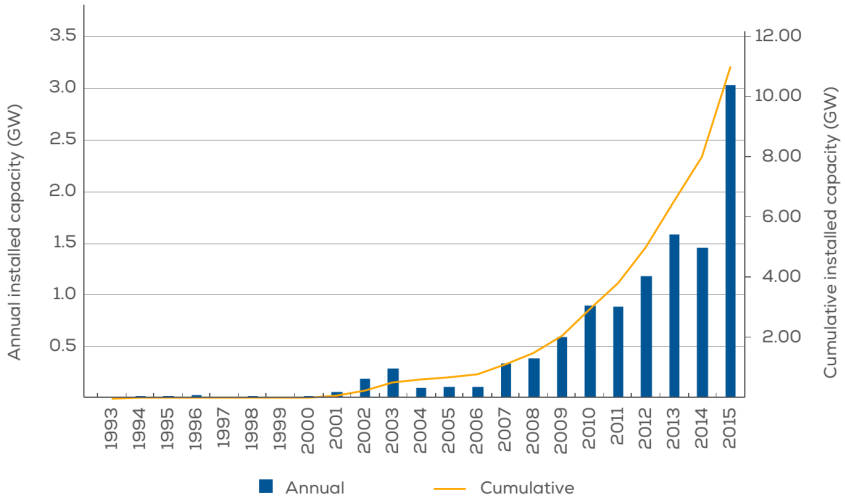


Fig. 2.1 Evolution of offshore wind power installed capacity in Europe, (Source: The European wind energy association, [7], 2016)

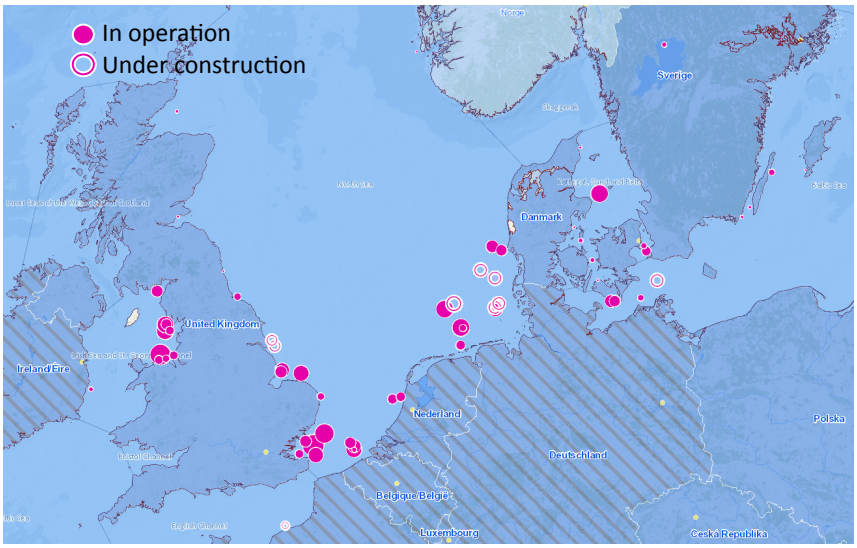


Fig. 2.2 Offshore wind farms in Europe (Source: European commission, [10], 2016).

2.2 Grid integration of offshore wind farms

The offshore industry has rapidly evolved towards larger projects in terms of rated power, size of the wind turbine generators (WTG) and distance from the shore in recent years. This evolution has also been accompanied by an adaptation of the electrical interconnection schemes with the onshore AC grids. While in the case of wind locations close to shore, AC submarine cables are still the cheaper option, for projects farther offshore DC has imposed itself as the best suited transmission technology. Fig. 2.3 presents the well known graph where the break-even distance for which DC becomes a more cost effective solution for both overhead line and cable power transmission is presented. However, the exact break-even distance for a particular project depends on a number of factors such as wind conditions, size of the wind farms, cost of energy and others.

In Fig. 2.2 it is observed that most offshore wind projects in Germany are located far away from the coastline. This is the reason why several wind farm interconnections using the HVDC technology have been commissioned and are already in operation. A map of offshore wind interconnection projects in Germany is displayed in Fig. 2.4.

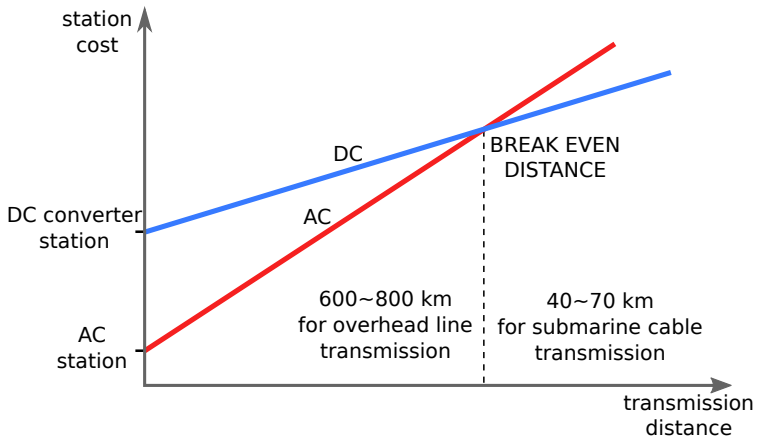


Fig. 2.3 Break-even distance AC against DC.

2.2.1 AC interconnection of offshore wind farms

Power transmission using AC is the most common method in electrical grids, and it was the natural choice as well as a relatively simple and economic way for connecting the first offshore wind projects. The first generation of wind farms commissioned in the 90's were located very close to shore in Denmark and the Netherlands. They also generated relatively low power levels. These first projects relied on medium voltage AC (MVAC) as the transmission technology. As displayed in Fig. 2.5, the generator output voltage is stepped up by a transformer within the turbine to a voltage level in the range of 10-36 kV. This voltage is used

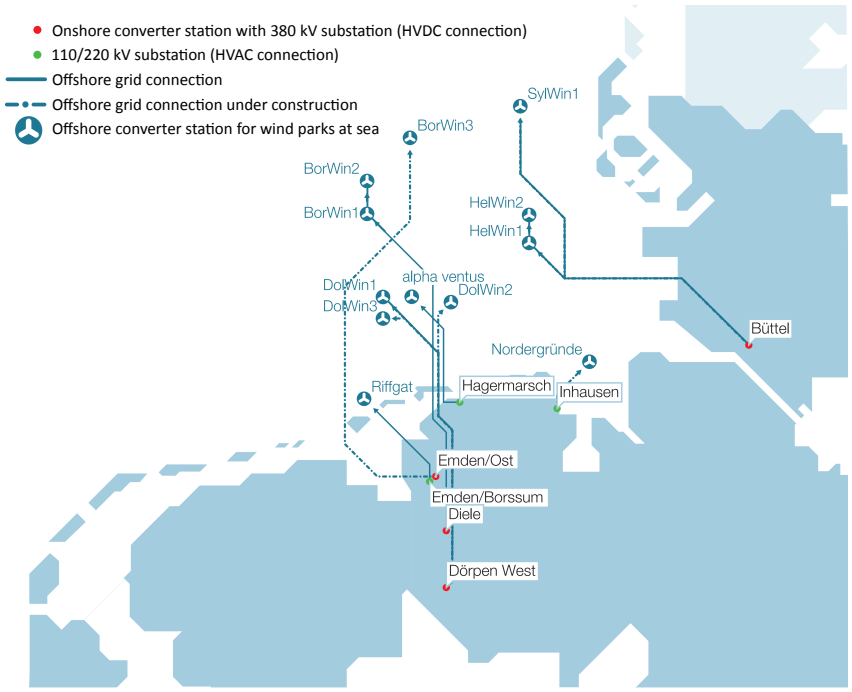


Fig. 2.4 German offshore interconnection projects by Tennet (Source: Tennet, [11], 2014).

for both the interconnection of the turbines in the arrays and also to export the power to shore. In this way the need for an offshore AC substation on a platform is avoided. One of the largest projects using this technology is the Egmond aan Zee wind farm in the Netherlands, commissioned in 2006 with a power rating of 108 MW and 14 km away from shore.

In order to avoid the large cable transmission losses when transferring larger amounts of power, the inter-array MVAC voltage can be stepped up to high-voltage levels which is then used in the export cables that go to shore. This results in a high voltage AC (HVAC) interconnection scheme as displayed in Fig. 2.6. As observed, in this configuration, one or several offshore AC substations will be required. The largest wind farm in operation at the time of writing, the London Array in the UK (630 MW and 20 km away from shore), uses this technology with 33 kV / 150 kV inter-array and export voltages respectively, and two offshore AC substations with a power rating of 360 MVA each. In an effort to reduce the losses in the offshore MVAC grid, the industry is also working towards the adoption of 66 kV as the standard voltage [12].

Modern WTGs with full-scale power electronics converters overcome some of the older WTG problems such as reactive power and voltage control, FRT capability and short circuit current contribution [13]. Nonetheless the main limitation for AC transmission is the large amount of reactive current flowing through the cables due to their capacitance, which increases the losses and limits the maximum transmission distance. Additional power electronics based

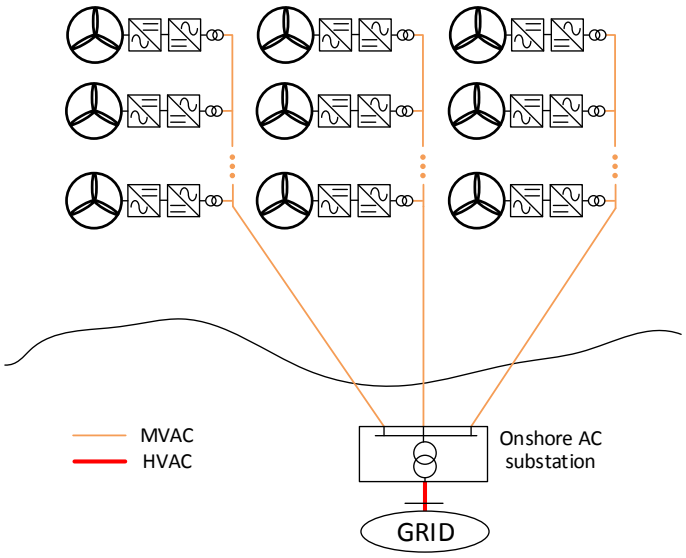


Fig. 2.5 MVAC interconnection of an OWF.

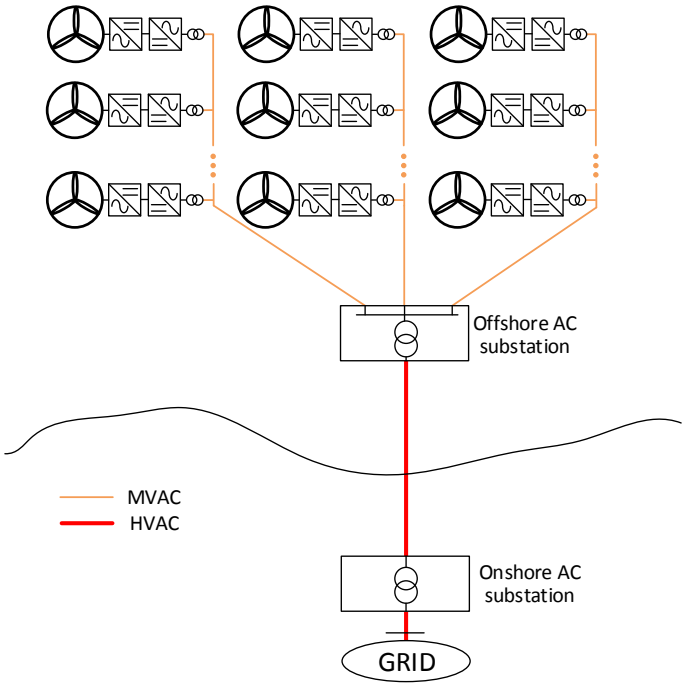


Fig. 2.6 HVAC interconnection of an OWF.

compensation in the form of SVCs or STATCOMs is therefore required to stabilize the voltage and ensure compliance with grid codes. Recent studies by Elliot et al. [14] suggest that AC might still be a competitive option for even longer distances than generally assumed, specially if reactive power compensation at the midpoint of the transmission cable is used. An additional problem is the propagation of the onshore grid faults offshore, which affects the operation of the wind turbines [15].

2.2.2 DC interconnection of offshore wind farms

DC transmission does not produce any reactive power flow on the cables, overcoming the main limitation in distance from which AC transmission suffers. In this case, as displayed in Fig. 2.7 an additional offshore HVDC conversion station is required, which receives the power generated by one or several wind farms through HVAC cables. Two main technologies are used for the HVDC transmission in conventional onshore projects, where onshore refers to HVDC power transmission on land and not to onshore wind. Current source converters (CSC), also know as line commutated converters (LCC) or classic HVDC, are the standard option for bulk power transmission. A more recent alternative, the voltage source converter (VSC) technology [13, 16], was first used in 1997.

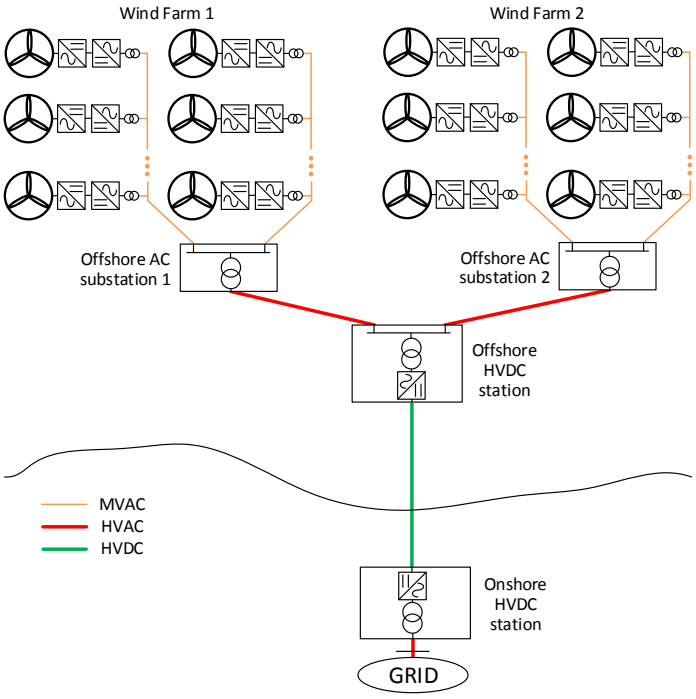


Fig. 2.7 HVDC interconnection of an OWF.

Line Commutated Converters

First introduced in 1954, it is a well known mature technology. The following characteristics limit the applicability of the LCC technology in offshore wind interconnection projects [13, 17]:

- The converter stations always absorb reactive power. Compensation is needed both onshore and offshore using SVCs or STATCOMs to comply with grid codes and ensure correct commutation of the thyristor valves.
- Subject to commutation failure in thyristors.
- Need of large and bulky harmonic filters on AC side: large size and weight of converter station.
- Lack of black start capability: diesel generators are needed offshore.
- LCCs need to operate at a minimum of 5-10 % of its rated power.
- Power flow reversal, needed for the wind farm start-up, requires to invert voltage polarity. This limits the use of cheaper XLPE cable technology due to space charge problems and makes it unsuitable for building large DC grids.

LLC was initially considered at the early stage for OWF interconnections [13, 18]. One of its main advantages is its good efficiency with power loss levels per substation below 1% [19–21]. The cost of the offshore platforms on which the AC/DC converter is mounted increases with the size and weight of the conversion equipment, and represents a large portion of the total wind farm cost. The above mentioned drawbacks of the need for reactive power compensation and harmonic filtering result in heavier and bulkier converters than the VSC alternative presented next. This is the reason why an offshore wind farm interconnection project has never been commissioned using LCC technology [13, 22, 23].

Voltage Source Converters

On the other hand, VSC technology presents the following characteristics which make it well suited for OWF interconnection projects [13, 24]:

- Independent control of active and reactive power: grid support during faults and compliance with grid code requirements.
- Also no reactive power compensation needed; neither offshore nor onshore.
- Can operate down to 0% of its rated power.

- Black start capability and possibility to supply passive networks.
- Low harmonic generation: minimal filtering, if any, is needed at the AC terminals.
- Power reversal achieved by inverting current direction: limits problem of space charge with XLPE cable technology.
- Flexibility to form DC grids.

For all these reasons, VSC technology has become the state of the art solution to interconnect distant OWFs. The original two-level VSC technology [25, 26] presents the drawback of needing series connected devices to reach HVDC blocking voltage levels in the IGBT valves, which is challenging and requires complex gate driving, snubbers and special semiconductor packaging [25, 27]. Furthermore, the use of pulse-width modulation (PWM) generates high losses (between 1.5-2%) compared to LCC converters. [19, 21, 28]. The first OWF interconnection using HVDC was commissioned in 2009 using 2-level VSC technology [29]. However, as the modular multilevel VSC technology [30] has become more mature, it has been the technology of choice for all the HVDC interconnection of offshore wind farms since the first projects were commissioned in 2014 [24, 29]. The basic structure of the modular multilevel converter (MMC) VSC is displayed in Fig. 2.8. Thanks to its modular structure, no series connection of IGBTs is needed and a low switching frequency of each individual IGBT is obtained, greatly reducing the converter losses which can go down to around 1% [20]. Also, thanks to the stepped nature of the generated AC voltage [31] less AC harmonics are produced and the filtering requirements are almost eliminated.

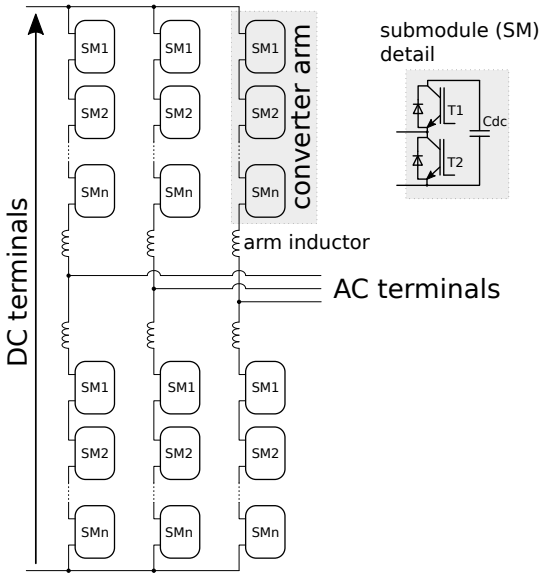


Fig. 2.8 Detail of the state of the art voltage source converter of the type modular multilevel converter (MMC).

2.2.3 Future developments

Recent efforts to reduced the capital investment required for OWFs and their grid integration have resulted in some alternative proposals which are still at a research stage.

The first one consists on replacing the offshore MVAC collection grid by a DC equivalent [32, 33] as shown in Fig. 2.9. This configuration presents the advantage of only needing 2-core DC cables for the offshore collector grid with the resulting cost saving in copper. The DC/AC conversion stage and output transformer in each wind turbine is replaced by a DC/DC converter to step-up the voltage to MVDC levels. The offshore AC substations and associated platforms are also eliminated with the subsequent cost saving. Finally, in the offshore HVDC station the AC/DC converter is replaced by a DC/DC converter which steps-up the voltage from MVDC to HVDC levels. This last converter is precisely the main challenge for the implementation of such solution. The very large step-up ration and high power rating [34] require of innovative circuits with power losses comparable to those of the conventional AC/DC converters while remaining cost effective. Such technical solution does not exist yet even if some research efforts are being consecrated to its development and a commercial solution is expected to be available by 2030 [35].

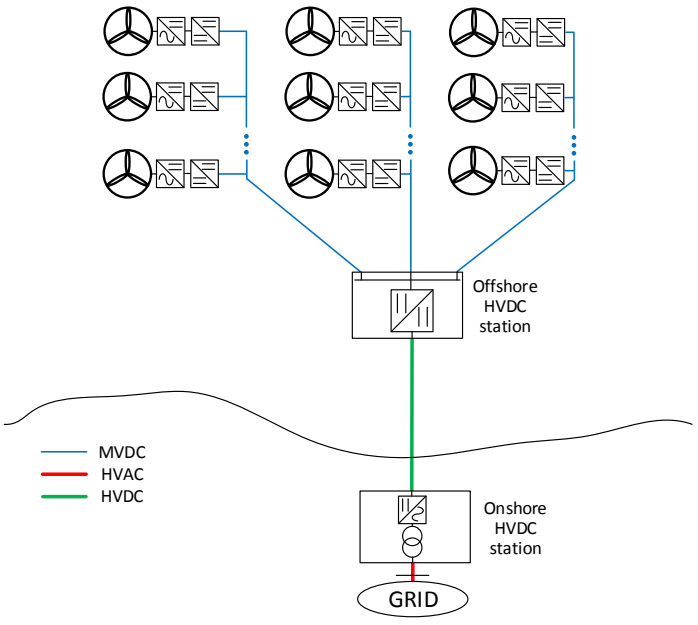


Fig. 2.9 HVDC interconnector using an offshore DC collector grid.

An alternative proposal that keeps an AC cable transmission to send the power onshore has also been made, operating at a frequency lower than the standard 50-60 Hz for conventional electrical systems. In [36] and [37] for example, the authors propose both an offshore collector grid and transmission onshore using

low frequency AC whereas in [38] a DC collector grid is proposed instead. The proposed frequencies of operation are in the region of 16.7 Hz as used for railway networks in some countries. An AC/AC conversion stage, commonly known as cycloconverter, is then needed offshore to adapt the frequency to that of the main AC grid. The advantage of this solution is the increase in transmission capacity and distance thanks to the reduction on capacitive charging currents flowing through the submarine cables when compared to a 50-60 Hz HVAC interconnection. As an example in [36] the authors investigate a 600 MW transmission for distances of up to 500 km when using 245 kV cables. An additional advantage is the use of standard AC breakers for protection which allows to add redundant paths to extract the power [38] and isolate portions of the circuit in case of a fault. An equivalent function in DC is more challenging due to the lack of a commercial solution for the implementation of DC breakers with the required voltage and power ratings.

A third alternative which has recently attracted a lot of attention was originally proposed in [39] and more recently recovered in [40], is represented in Fig. 2.10. The solution replaces the VSC converter in the offshore HVDC station, which is one of the most expensive pieces of equipment [41], by a diode rectifier unit. The company behind this idea [42] claims that this would result in a more efficient and reliable converter and a more compact, lighter and easy to install offshore platform, reducing the overall project cost and increasing the transmission efficiency.

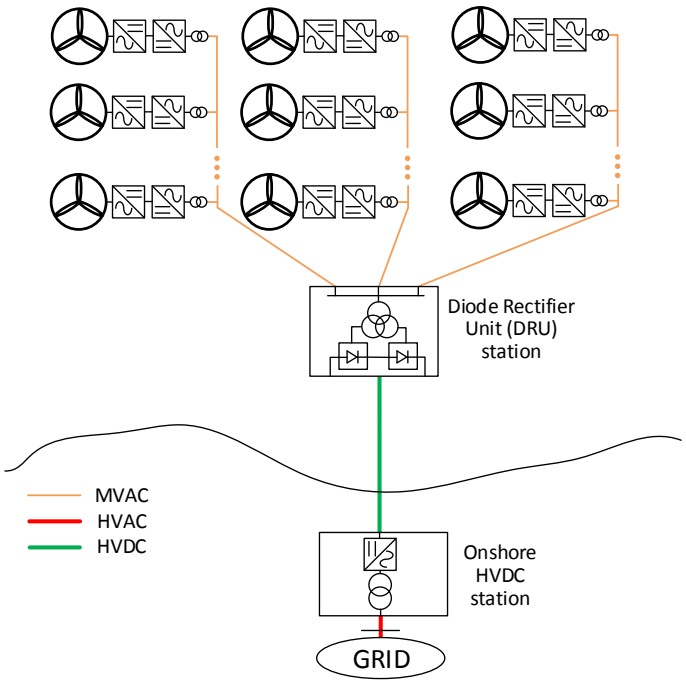


Fig. 2.10 HVDC interconnection using a diode rectifier station offshore.

The main drawback with this solution is a complex control of the offshore AC collector grid due to the lack of the VSC station which normally creates the AC voltage which serves as a reference to all the wind turbines, regulates the frequency and supplies reactive power to stabilize the collector grid. When using diode rectifiers as the HVDC converter, the control of the offshore AC grid increases in complexity since it is the duty of the wind turbine converters to create and regulate this grid. This problem of distributed control has been investigated in literature and some proposals have been made such as presented in [39] and more recently in [43] or [44], where each wind turbine converter contributes to the frequency regulation and provides reactive power for the voltage regulation of the collector grid. In this way a stable AC grid can be established offshore.

Even if some of these alternatives are starting to be considered for long term developments, the risk associated with the introduction of any new technology makes that currently two options remain as the only realistic alternatives for projects at the planning stage. These are conventional HVAC for wind farms relatively close to shore or HVDC using the VSC-MMC technology for more distant projects. This research work focuses on the latter. In the following sections the protection mechanisms implemented in these type of links are reviewed in detail.

2.3 Protection of the HVDC interconnector and the grid code

Grid codes are the technical rules that ensure a correct combined operation at the interface point between two interconnected electrical systems. Any generator connected to a transmission or distribution network must comply with the requirements specified in the grid code to ensure a safe and secure operation of the system. HVDC connected OWFs are a very particular type of generation which differs in some aspects from traditional onshore synchronous generation for which grid codes were developed [13]. A lower generator inertia compared to traditional generators, which is decoupled by the power electronics from the system frequency, or the limitation in active power generation controllability are examples of such differences that have a limiting effect on the grid stabilizing functions that wind generators can offer. These specificities often lead to deviations and amendments exclusively for OWFs with respect to the existing code.

In a HVDC connected OWF there exist two different AC systems, the onshore grid and the offshore collector grid. While at the onshore location the relevant national grid code applies, no particular code regulates the offshore collector grid whose operation is fully decoupled by the HVDC system. Nonetheless the

TSOs usually decide that onshore requirements are passed offshore, and therefore remain often valid [45]. The two different interface points where the imposed regulations have to be met are [24]:

- **Onshore interconnection:** Primary or secondary winding of the grid entry transformer.
- **Offshore interconnection:** Either at the offshore AC substation or in the primary ot secondary winding of the HVDC station transformer.

A variety of requirements are specified in the grid code which apply to the VSC station onshore and, as explained, passed to WTGs and the VSC station offshore, at the respective interface points. The following are usually listed in most grid codes [24]:

1. Voltage and frequency ranges of operation.
2. Voltage regulation through reactive power exchange.
3. Frequency regulation through active power control.
4. Behaviour during and after faults, including FRT requirements and post-fault recovery.
5. Grid connection capacity.
6. Short circuit current contribution.
7. System earthing.
8. Insulation coordination.
9. Power quality including harmonics and flicker.
10. Power system restoration.

In an effort to harmonise the disparities in the different country regulations, the *European Network of Transmission System Operators for Electricity* (entso-e) is working to develop a set of grid codes which will be enforced at a European level [24]. In particular DC connected OWFs fall within the scope of the*Network Code on HVDC connections* which was published on the 6$^{\text{th}}$ of August 2016 in the Official Journal of the EU [46].

A detailed description of all the requirements listed above is given in published literature [13, 18, 24, 45]. The focus of this work is on the fourth point which regulates the system behaviour during network faults and the subsequent recovery. An critical appraisal of this subject, paying special attention to the FRT requirement is presented next.

2.3.1 Behaviour during network faults

In HVDC interconnected OWFs three main types of faults are identified according to their location (Fig. 2.11). A set of control actions and protective circuits are usually in place, and activated during the fault to ensure the stability and compliance with the grid code. The Common protective actions used during each type of fault include [18, 45]:

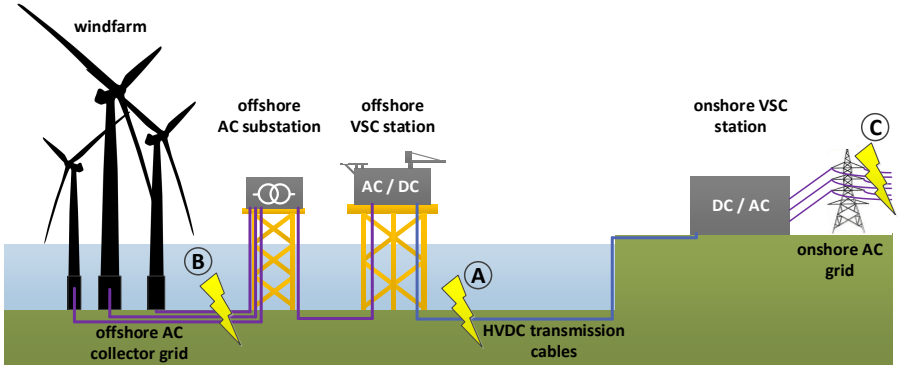


Fig. 2.11 Possible fault locations in the wind farm HVDC connector.

DC cable fault (A)

During a fault on the DC link the DC voltage collapses. In the standard VSC converters (2-level or half-bridge MMC) the anti-parallel diodes offer a path for a fault current to flow from the AC networks into the fault, and therefore the AC switchgear is used to disconnect. Offshore, the VSC converter brings the collector voltage down to zero and the current is extinguished by the trip of the WTGs and AC breakers [45]. Onshore, the AC breakers will also trip isolating the AC grid from the fault [18].

An alternative to be able to ride-through the DC fault is to use VSC converters based on full-bridge cells or the so call hybrid topologies, which use a mix of different cells in each converter arm [47–49]. This new generation of converters is capable of blocking the fault current by operating in a STATCOM mode at the cost of increasing the number of semiconductors and therefore the power losses.

Offshore collector fault (B)

During a fault in the AC collector grid the AC voltage collapses and the ability to extract the power from the WTGs is reduced. The offshore VSC quickly reduces the voltage amplitude at its terminals in order to control the reactive current flow within its maximum possible value. Only a reduced fraction of the generated power can then be transferred to the DC link and onshore. In the case of variable speed generators with fully rated converters including a DC chopper,

the surplus power is dissipated in a braking resistor for the duration of the fault [45]. Alternatively the generator torque can be reduced and the turbine blades pitch controlled to reduce the generator output power, however this generates mechanical stress [24, 45]. When the fault duration exceeds a predetermined value, the generators are allowed to trip and the wind farm will be disconnected.

Onshore network fault (C)

During a fault in the onshore AC grid, the AC voltage collapses. The onshore VSC station capability to inject power into the faulted network reduces as a result and in the absence of any action offshore, the excess energy is stored in the DC bus capacitance producing an over-voltage. To comply with the grid code, the onshore VSC needs to remain connected providing reactive power support for a predefined amount of time. A mechanism to avoid this energy accumulation while riding through the fault is therefore needed, and several alternatives have been proposed. This is the fault case this thesis work focusses on. The particularities of the FRT requirement and the over-voltage mitigation methods are described next.

2.3.2 The low voltage fault ride-through (FRT) requirement

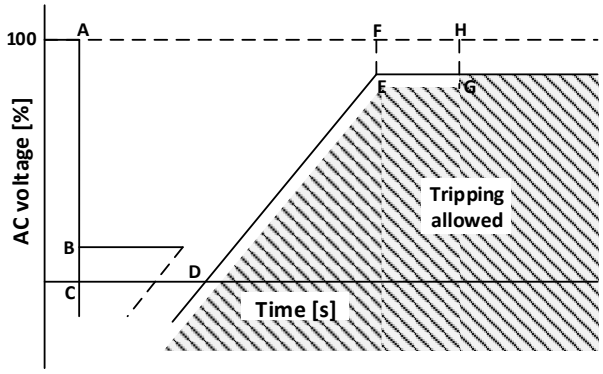
When the fault event takes place onshore, the reduction in the capacity of the VSC station to inject power into the faulted grid is proportional to the level of reduction in the grid voltage, according to expression (2.2):

$$P = \frac{V_{vsc}\, V_{grid}}{X} sin\delta \tag{2.2}$$

Where,

- V_{vsc}: AC voltage at the VSC terminals (V)
- V_{grid}: AC grid voltage (V)
- X: AC reactance (Ω)
- δ: phase difference between voltages

Grid codes establish a voltage-time profile, the FRT capability curve, above which a generation unit is not allowed to trip. Fig. 2.12 shows the plot with the FRT curve, including the variations in time an voltage levels for the grid codes of European countries with large wind energy penetration.



Grid Code	BC	BD	AF	FE	AH	HG
Denmark	25%	0.1 s	0.75 s	25%	10 s	NA
Germany (EON)[1]	0%	0.15 s	0.15 s	30%	0.7 s	10%
Germany (EON)[2]	15%	0.625 s	3 s	10%	NA	NA
Ireland (EirGrid)	15%	0.625 s	3 s	10%	NA	NA
Spain	20%	0.5 s	1 s	20%	15 s	5%
UK (NG)	0%	0.14 s	1.2 s	20%	2.5 s	15%

[1] For generating unit with large symmetrical short-circuit current component.
[2] For generating unit with low symmetrical short-circuit current component.

Fig. 2.12 Fault ride through requirement in different grid codes.

While in Denmark a voltage drop below 0.25 per unit (p.u.) of the nominal value allows the converter stations to trip, in countries like Germany and the UK, tripping is not allowed even with a voltage collapse to 0 p.u. for up to 150 ms. As part of the ongoing work by entso-e on European grid codes, the *Requirements for grid connection of generators* was published in April 2016 and become a binding EU regulation in May 2016 [50]. The code specifies a harmonised FRT profile (Fig. 2.13) which represents a lower limit for the phase-to-phase voltage at the connection point. Each transmission system operator (TSO) can establish its own voltage-time profile in line with the values specified in Fig. 2.13 which are specific for offshore wind farms.

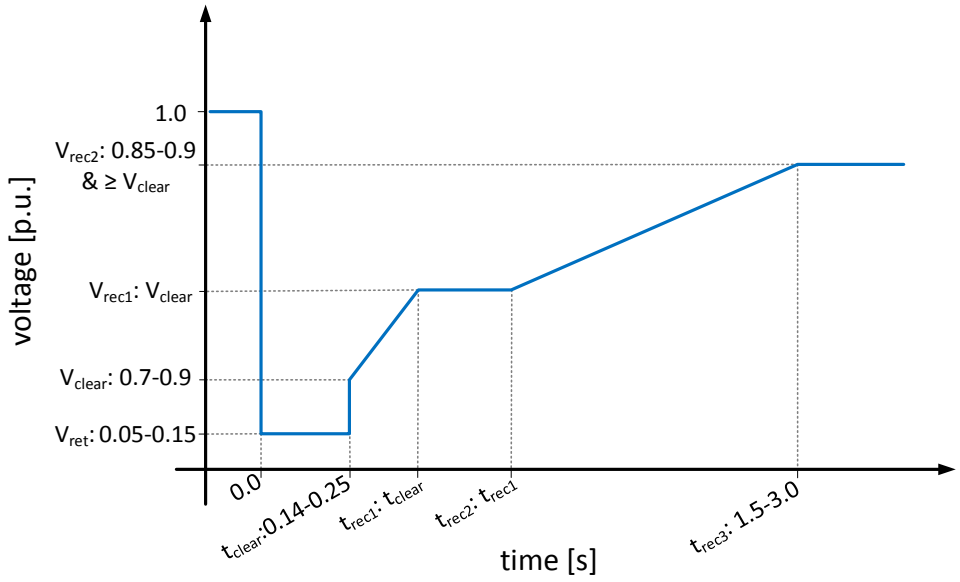
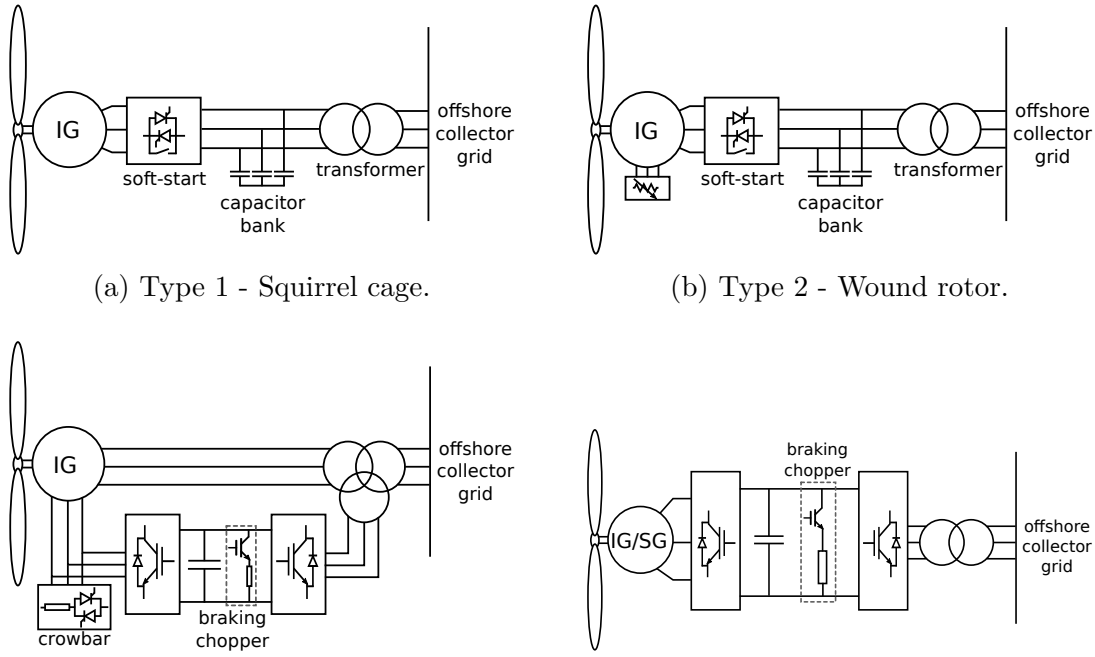


Fig. 2.13 Fault ride through profile proposal by entso-e.

While the OWF interconnector operates within the *no trip* area of the FRT requirement, the power unbalance between offshore generation and onshore injection capability into the faulted network can lead to an over-voltage situation both in the DC link or the AC collector grid. To avoid a system trip due to exceeding the voltage operation range, some control actions and protection circuits can be used. A detailed review of these methods is presented in section 2.4.

2.4 Review of over-voltage mitigation methods

To comply with the low-voltage FRT requirement and mitigate the over-voltage in the HVDC link a number of solutions have been proposed in literature. A first group of solutions rely on a rapid reduction of the wind farm power output to limit the over-voltage below the maximum safe values. An alternative consists on the use of protection circuits, known as Dynamic Braking Systems, which dissipate the excess power in a braking resistor, keeping the operation of the wind farm undisturbed. A third possibility is to use a hybrid approach, where a combination of both methods is used to theoretically achieve an overall system cost reduction. All are reviewed in this section. The convention used in the text for the different types of WTGs is explained in [51] and graphically presented in Fig. 2.14. This figure is used to describe the different types of WT hardware and their influence on the FRT that are described in the sections that follow, e.g. power/non-power control. Fig. 2.15 summarizes of the different DC over-voltage mitigation methods described in the remainder of the chapter.



(a) Type 1 - Squirrel cage.

(b) Type 2 - Wound rotor.

(c) Type 3 - DFIG.

(d) Type 4 - Full size converter.

Fig. 2.14 Different types of wind turbine generators.

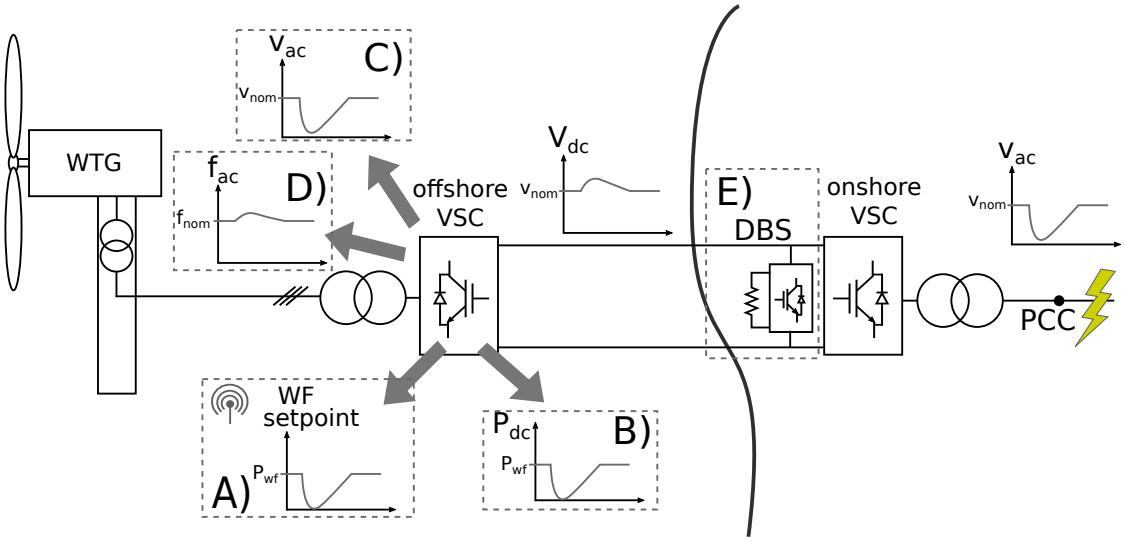


Fig. 2.15 Summary of DC over-voltage mitigation methods during FRT event: A) Wind farm set-point change via telecommunications, B) Active power reduction in offshore VSC station, C) Offshore voltage reduction, D) Offshore frequency increase, E) Dynamic Braking System.

2.4.1 Wind farm output power reduction techniques

This set of techniques rely on the coordinated or uncoordinated actions of the offshore VSC station and WTGs to rapidly reduce the wind farm output power.

The topic has been extensively researched in literature and a summary of the different methods identified is presented here:

Methods requiring telecommunications (A)

The implementation of this solution relies on the fibre optics communications, usually available between the wind farm controller and the WTGs, to dispatch individual power reference values to each turbine. Optionally, the communication link between the onshore and offshore VSC stations is also used.

In [52] this method is described. The onshore VSC station calculates the maximum transferable power from the wind farm according to the fault severity and sends the information to the offshore VSC. The information is combined with the current wind farm output power and a reduction factor is calculated. This is then sent to each WTG which reduces its active power output accordingly. The communications between the VSC stations can be eliminated and replaced by a DC over-voltage control action implemented in the offshore VSC. In [53] the same method is proposed for a wind farm using type 4 WTGs without braking chopper (Fig. 2.14). The WTG output power is lowered by the generator torque reduction, which leads to an acceleration of the turbine rotor storing kinetic energy and, if necessary, complemented by a change in the blades pitch angle.

The main problem with this approach is the delay introduced by the communications and the reliability issues if communications are lost. In [52] it is explained how the communication delay limits the speed of power reduction. In [53] when ideal communications are used the system works well, however for a 10 ms delay in the communications the DC over-voltage limit is exceeded. As explained in [54], the wind farm controllers generally rely on slow SCADA protocols (10-100 Hz), so the delay in updating the WTGs power set-points could go up to 100 ms.

Uncoordinated actions by offshore VSC (B, C and D)

In this case, on detection of a DC voltage increase the offshore VSC station reacts, without coordination with the WTGs, to rapidly reduce the power injection in the HVDC link.

A first approach consists on the offshore VSC to rapidly reduce the active current absorbed while keeping AC frequency constant [52]. The energy generated by the WTGs is then stored in the offshore grid capacitance, leading to a rapid increase of the AC voltage [55]. The method works in combination with type 3 and 4 WTGs, which are power controlled, if additional loops are added to the turbine controller to reduce its output power on detection of an AC over-voltage, however this will have a slow response. The method does not work with type

1-2 WTGs, where a voltage increase does not lead to a reduction of the turbine power output.

A second approach is based on a rapid reduction of the offshore collector grid voltage emulating a short circuit condition, which reduces the power flow into the HVDC link [54]. The method relies only on the FRT capability already implemented in the wind turbines and not on special modifications of the turbine controllers [53]. With WTGs of types 1, 2 and 3 the method works by de-magnetizing the generator and an increase of angular speed [56]. This triggers the modification of the blade pitch angle controller to reduce the mechanical torque and mitigate the effects of the rotor acceleration. In type 4 WTGs, the voltage drop crelates an over-current on the inverter side and a DC bus voltage increase which is reduced by triggering the braking chopper [56] or by using the rectifier converter to reduce the electric torque in the generator. However the method presents several problems which might limit its applications. The voltage sag, which can go all the way down to 0 p.u., can lead to dummy faults and cause disconnection of generators, specially for types 1, 2 and 3 [57]. As explained in [53], large short-circuit currents will flow through the WTGs and offshore VSC station at the beginning and at the end of the fault, producing mechanical stress in the turbine and electrically stressing the semiconductors. In type 1-2 machines the pitch control needs to act fast otherwise the acceleration of the rotor produces a high slip with very large amounts of reactive power being absorbed [54]. This will also call for an increase of the offshore VSC station current rating. In type 4 WTGs the back-to-back converter can effectively limit the over-currents and therefore this problem does not apply. In [56] the authors point out that short-circuit currents can contain significant DC component, resulting in high mechanical stress in WTGs and converter semiconductors. Therefore they propose to complement the voltage reduction by the injection by the offshore VSC of a DC voltage pulse in the 3-phases of the offshore grid which, they demonstrate, helps reducing the surge currents. As noted in [54] an additional problem is that the voltage sag might trigger the voltage support mechanisms of the WTGs by reactive current injection, which should ideally be disabled. In [55] the main drawbacks identified are the very fast change in electrical torque producing high mechanical stress, the potential crowbar triggering in type 3 generators and the fact that very fast voltage sags might be limited by the AC inductance because VSC will reach its current limit. In [58] potential instability caused by the rotor acceleration is seen as a drawback when using type 1 generators.

A third approach consists on a controlled increase of the offshore grid frequency. This works with fixed-speed turbines (types 1-2) and is used to absorb some of the wind farm produced power by increasing the system apparent inertia as explained in [57]: the turbine rotors accelerate storing kinetic energy.

However, as explained in the paper, the energy absorption using this method is relatively low compared to the amount of energy produced by the farm and might be impractical. With types 3 and 4 of WTGs, being variable speed and power controlled, this method does not produce a reduction of the output power unless the turbine controller is modified. In [55] this method is also described, and it is mentioned that to achieve a power reduction from the nominal value down to zero, 1 or 2 Hz increase in frequency might be needed. It is pointed out that grid codes might limit such a large frequency increase offshore.

Voltage/frequency signalling to WTGs (C and D)

In this case the offshore VSC, upon detection of a DC voltage increase, modulates the offshore grid voltage amplitude or frequency. As opposed to the uncoordinated approach presented before, in this case the goal is not to directly reduce the power injection in the HVDC link by the VSC, but rather to indicate the onshore fault event to the wind generators to trigger a controlled regulation of their output power. Additional high level control loops are needed both in the VSC station and WTGs to implement these two methods [59]. With types 1-2 turbines only mechanical actions (blade pitch control) are possible, which are slow and stress the drive train. With type 3 and 4 turbines suitable control of the converters provides a faster power reduction [57]. In type 3 turbines, the voltage reduction method also contributes to the generator de-magnetization, increasing its angular speed and reducing the output power [59]. With type 4 generators, if available, the braking chopper can absorb the produced power [60], decoupling the generator from associated grid disturbances. The DC voltage rise is used by the offshore VSC to proportionally reduce the AC voltage amplitude or to increase offshore grid frequency according to a pre-defined scaling factor [59]. In paper [61] the voltage drop method performance is assessed with type 3 and 4 WTGs. The paper additionally analyses the influence of this FRT method on the onshore AC systems stability after the fault by observing the rotor-angle excursions and speed deviations of the generators in the onshore AC grid.

The main drawback usually identified for both methods is the required modification on the WTG controllers [54]. With the voltage regulation method, the need to disable the WTG reactive power support for this strategy to work is an additional drawback [57] although according to [62] the decrease in performance is not expected to be dramatic even if the reactive support is kept active. In [59] the mechanical stress in terms of speed variations is also seen as a drawback with type 3 WTGs, as well as the inrush currents resulting from the generator demagnetization and small over-currents in WTGs and offshore VSC after the fault clearance. Type 4 generators do not experience these problems when the local braking chopper is used. In [52] the main drawbacks cited are over-currents

in type 3 generators requiring dedicated protection devices (crowbar, chopper) and associated mechanical stress to the drive train when using the voltage modulation approach. A potential crowbar ignition also produces mechanical stress and loss of controllability of the generator.

One drawback commonly cited with the frequency modulation method is the need for fast frequency deviation measurements by the WTG controller. Detecting small variations in a fraction of a period is difficult to implement [55]. Typical PLLs are slow, producing delays of 10-100 ms. Faster PLLs are possible but will be very sensitive to noise [54]. As a consequence of the slow response the performance of this method might be limited. In [52] the authors present some simulation results comparing both frequency and voltage modulation methods. They conclude that the frequency modulation method is not fast enough to limit the DC over-voltage.

Once the fault is cleared, the offshore VSC restores the voltage or the frequency in the collector grid in order to re-establish active power transmission.

2.4.2 Dedicated energy dissipation circuits onshore (E)

Commonly known in literature as *DC choppers*, *braking choppers* or *dynamic braking systems (DBS)*, they all refer to a solution including a power electronics converter which modulates the power dissipation across a resistor. The term *braking* has its origin in the dissipative braking choppers historically used in motor drives. Throughout this thesis, the term DBS has been adopted when referring to these circuits. For wind farm interconnectors, the power electronics and braking resistor need to be dimensioned to absorb the wind farm rated power for the duration of the fault. The DBS is placed inside the onshore VSC station, connected across the DC terminals (Fig. 2.15), due to the much higher cost of increasing the weight and volume supported by the offshore VSC station platform. The DBS controller monitors permanently the DC voltage, and if the predefined thresholds are exceeded during a FRT event, the DBS modulates the power dissipation in the braking resistor to match the excess power being injected into the DC link from the OWF. In this way the power balance is restored and the DC over-voltage is controlled.

Most literature references use this solution as the benchmark case to assess the performance of the offshore power reduction techniques described in previous subsections. There is a general consensus concerning the obvious advantage of this method with respect to power reduction techniques for HVDC over-voltage mitigation. With the DBS, the wind farm and offshore grid operation stays completely decoupled from disturbances in the onshore grid [52]. The WTGs output power remains unchanged during the fault, hence no acceleration of the rotors with the associated mechanical stress, instability, or short-circuit currents

when using type 1, 2 or 3 generators occur. In [63] the authors conclude that with a DBS the system recovers to the pre-fault state quicker and experiences less voltage and power fluctuations. The faster restoration of the active power injection on the fault clearance is also an advantage of this method [61]. A DBS is very robust [55] and in [64] it is chosen as the FRT solution since power reduction techniques either need telecommunications, are not suitable for all types of WTGs or require modifying the controls of offshore VSC and WTGs.

Furthermore, the use of a DBS is the only solution which has been practically demonstrated in real projects. In [65] it is presented as the most robust and practical solution for the Dolwin 1 offshore wind farm interconnection: it operates with any type of WTG, keeps the wind farm operation undisturbed and acts as a firewall, buffering disturbances in the onshore grid from entering the offshore grid. In [66] it is explained how the small equivalent capacitance of the HVDC link leads to the over-voltage limits, typically set at around 1.3 p.u., being reached very quickly (5-10 ms). The DBS, with its very fast reaction time of some hundreds of microseconds compared to the tens to hundreds of milliseconds reaction time of power reduction methods, is a more robust solution than power reduction methods. In [67], the technical approach used in Dolwin 2 and Helwin 1 offshore wind farm interconnectors is presented, and also consists on the use of a DBS.

Most references found in literature, which focus on the system level study of the FRT problematic, consider the DBS from the simplified perspective of an ideal switch in series with a resistor. Few references address the detailed implementation of the DBS circuit. In [65] some details are given about the use of series connection of IGBTs to implement a DBS valve. In [68] and [67] some detail is given regarding the implementation of modular DBS topologies that are built following the same principle from the MMC-VSC (Fig. 2.8).

The use of a DBS has also been proposed to mitigate DC over-voltages and provide with FRT capability to the novel method of wind farm connection using offshore diode rectifiers which was described in section 2.2.3 [69].

A high cost and the space requirements when compared to the power reduction techniques are recurrently highlighted as the main drawback of the DBS solution [53].

2.4.3 Hybrid solutions

The possibility of combining the use of energy dissipation circuits (DBS) with the wind farm power reduction techniques has also been proposed in literature as a cost-effective way to address the FRT requirement while keeping a good system reliability [54].

In [55] a combination of voltage reduction, frequency increase or rapid active current reduction by the offshore VSC with a reduced size DBS is proposed.

In general, the combined use of a DBS with any of the three power reduction methods allows for a slowed down torque reduction in the generators, which in turn helps reducing the mechanical stress and the other associated problems. In [52] and [57] the combined use of the voltage modulation technique and DBS is proposed. In this way, a secure operation of the system can be achieved without the need for a full-rated DBS.

With multi-terminal DC (MTDC) offshore grids a combination of several methods are possible. Initially, when a fault occurs, the excess power is re-dispatched from the faulted station to other inverter stations without exceeding their maximum power rating using voltage droop [70], or in [71], using a novel coordinated DC voltage control strategy. If the DC voltage still increases, wind farm power reduction techniques, such as voltage or frequency modulation, are applied. As a back-up resource to avoid an over-voltage if the previous methods fail, a DBS is triggered to absorb the excess power. In this way, power reduction methods and DBS circuits are only used in case of severe faults and the rating of the chopper can be reduced, decreasing the overall system cost.

In [61] a combination of the voltage reduction and DBS circuit is analysed with type 3 WTGs. The performance is better than when the voltage reduction is used alone in terms of DC over-voltage limitation but also regarding the electromechanical dynamics from the WTGs which propagated through the DC link during the FRT event. This leads to less disturbances to the onshore AC grid once the fault has been cleared.

2.4.4 Conclusions concerning the different methods

Most research publications use the DBS solution as a reference case to evaluate the performance of the power reduction and hybrid methods. In [52] the frequency and voltage modulation methods are compared in simulation. Despite showing that the frequency modulation method does not actuate fast enough to limit the DC over-voltage, the work concludes that a fast power reduction strategy would be enough to completely eliminate the need for a DBS integration. In [53] a simple DBS function is simulated and compared with communication based and voltage modulation methods for wind farm rapid power reduction. The advantage of decoupling the wind farm operation from onshore faults when using a DBS is acknowledged, but it is still regarded as a costly solution. The work concludes that the power reduction method can meet the fault ride-through requirement at a lower cost. In [63] the authors study the FRT of an offshore wind farm based on type 4 WTGs, with an onshore DBS to limit the DC over-voltage. The comparison with a HVAC transmission, where the turbine's local braking chopper provides the FRT capability, concludes that with the DBS and a HVDC transmission, an enhanced voltage recovery is obtained in the onshore AC grid

and the system recovers to the pre-fault steady state quicker while experiencing less voltage and power fluctuations. In [55] the comparison of 3 power reduction methods , their combination with a reduced size DBS and a full size DBS are briefly commented without any simulation or experimental results. Although the lowest ride-though failure risk and mechanical stress in WTGs is identified with the full size DBS, its cost and size are seen as a major drawback. The best alternative method proposed is the voltage modulation combined with a reduced size DBS. In [70] it is shown that for some severe faults in MTDC grids, the power reduction techniques might fail to completely restore the power balance in the HVDC link and the use of a DBS as a back-up protection is needed.

As observed, most references conclude that power reduction techniques are a better alternative merely based on the higher cost of a DBS solution. However aspects such as the impact on the AC system stability, post-fault recovery and the active power injection recovery speed are usually neglected. Recently published [61] addresses all these points. The impact of different over-voltage mitigation methods is studied considering the onshore AC grid stability by observing speed excursions in onshore generators. The results of these comparisons show that a combination of the voltage drop method for wind farm power reduction with an onshore DBS solution improves the performance of the offshore action or the full-size DBS alone with respect to the DC voltage variation. The paper also shows that a fast active power recovery after the fault is beneficial to minimize the disturbance to the onshore AC system. The use of DBS allows for a very fast power injection restoration after the fault is cleared, making it the best solution regarding this particular aspect. The DBS also shows the best performance concerning onshore AC grid stability perturbation, with hardly any electromechanical dynamics from the wind farm propagated through the DC link.

The long term impact of mechanical stress and short-circuit currents on the reliability of wind turbines is difficult to evaluate. Nonetheless the prevention of these negative effects by using FRT methods which help mitigating them seems judicious. Currently, only the use of the onshore DBS or the local braking chopper in case of type 4 WTGs achieve this, completely decoupling the wind turbine operation from disturbances in the AC grid [45].

At the time of writing, the fully rated onshore DBS is the well established standard solution to provide with FRT capability to the HVDC connected wind farms [24]. It is also the only method which has been commissioned and demonstrated in real projects, for example Dolwin 1 [65] and BorWin 2 [67]. Furthermore, it is in fact a requirement from the grid operators to install a DBS in all the HVDC interconnectors being built today [72]. The turbine based braking chopper might be regarded as a potential future alternative to the full-size DBS, since most offshore projects start including type 4 WTGs. However, as explained

in [45], the split in ownership between the wind farm and the HVDC transmission system applied in some countries, hinders the implementation of optimized control strategies that require the coordination of elements in both the transmission and the generation chain. Even in a future scenario where these regulatory difficulties may not exist, the inclusion of the voltage-clamping function provided by the onshore DBS would still be prudent to act as part of a protective shut-down [45].

There is however a lack of published research dealing with the practical implementation of DBS circuits, covering the circuit dimensioning and the required control strategy. Most of the previously cited publications consider the DBS circuits from a system perspective: an available function which absorbs power as required to mitigate the DC over-voltage, but without dealing with the details of its low-level implementation. Two different manufacturers have disclosed some vague information regarding their DBS implementation ([65] for ABB or [67] for Siemens) but without providing any details on the sizing of the different elements or the required control strategies. This thesis work fills this gap with a thorough investigation of the low-level implementation of different DBS circuits. The re-use of the same sub-module technology used in the VSC stations (Fig. 2.8) for the DBS implementation can help reducing the cost and facilitates its commissioning. A special effort is therefore dedicated to the understanding of the energy balance in DBS circuits implemented with half-bridge and full-bridge sub-modules, which was left uncovered by the few publications in which such implementations are proposed, such as in [68] and [73]. The resulting contribution to the field is a novel power modulation technique which naturally achieves the energy balance in the DBS valve and is presented in Chapter 3.

2.4.5 DBS concept generalization: The Energy Diverting Converter

In order to address the drawback of a high cost, which as presented in this chapter, is commonly associated with the DBS solutions, this thesis also develops a novel concept: the *Energy Diverting Converter* (EDC). This new family of circuits results from a modification of the DBS circuit, which provides the same over-voltage protection in the HVDC link but with the addition of some extra functionality of interest for the operation of the DC transmission system. In this way the cost of the converter is not reduced but thanks to the added functionality, the economical investment is better justified. The term *energy diverting* highlights the fact that the excess power absorbed by the circuit is not necessarily dissipated but can be diverted into a secondary circuit, as is the case with the HVDC tap concept that will be presented in Chapter 7.

2.5 Summary

Wind energy penetration is growing fast in Europe and offshore wind, with the North sea as concentrating a lot of new developments, is becoming increasingly important. A variety of connection technologies to the onshore grid are presented in the chapter. Recent distant offshore wind farms rely on HVDC transmission technology using the latest generation of modular multilevel voltage source converters and submarine cables to bring the power to shore. The interconnection of such generation power parks is regulated by grid codes which impose performance requirements to be met by the interconnected park. One such requirement is the low voltage fault ride-through (FRT) capability of the HVDC transmission and OWF generators. During a fault in the onshore AC grid, power converters and wind turbine generators are not allowed to trip according to a FRT voltage-time profile. Meanwhile, the transmission system loses its capability to extract the power generated offshore leading to a DC over-voltage if no protective actions are taken. Several alternative over-voltage mitigation mechanisms are presented in the chapter. The addition of dynamic braking systems (DBS), a physical protection device connected to the HVDC bus onshore where the energy is dissipated in a braking resistor, is currently the preferred solution by transmission system operators. The main advantage of the DBS is a complete isolation of the offshore grid and WTGs from disturbances onshore and instantaneous power injection restoration once the fault is cleared. The goal of this thesis work, presented through the remaining chapters, is to investigate the low-level implementation, control methodologies and evaluation of the performance of different DBS circuits, which has not been previously dealt with in existing literature. While the main drawback of this solution is its cost, this work also investigates the addition of extra functionalities to the DBS circuit, in order to better justify such economical investment. The result is the Energy Diverting Converter (EDC) concept.

Chapter 3

The Dynamic Braking System

Recently published Standard IEC 62747:2014 [74] recommends the use of the term dynamic braking system (DBS) in a VSC-HVDC transmission context, when referring to a power electronics assembly made of a dynamic braking valve plus a braking resistor. This assembly forms a DBS arm, which is connected across the HVDC terminals in a VSC substation. The dynamic braking valve is subsequently defined as a group of controlled semiconductor switches which regulate the energy absorption in the braking resistor, in order to limit the transient over-voltage in the HVDC system caused by a fault in the high-voltage AC grid. This action helps the HVDC system to ride-through the fault, complying with the relevant grid codes.

There is currently three European manufacturers offering solutions for connecting offshore wind farms to onshore AC grids by means of VSC-HVDC schemes. These are ABB with the *HVDC light*, GE Grid Solutions with the *HVDC MaxSine* and Siemens with the *HVDC Plus* solution. All projects currently being commissioned or already in operation in Germany include a DBS as part of the VSC-HVDC transmission system. Very little information is available in published work concerning the different solutions from each manufacturer, and the main source of information can be found in patent applications and presentations at various conferences and events. As pointed out in IEC's technical report [75], there are different options for the implementation of the braking valve for a DBS, but the generic approach taken by the manufacturers is to keep the design of the braking valve similar to the converter valves in the VSC stations.

In this chapter four different circuits for the implementation of a dynamic braking system are studied. The operation principle of each circuit is explained and a suitable control strategy is proposed.

3.1 General concepts

A number of concepts which apply to all the four DBS topologies under study are presented in the following subsections.

3.1.1 Base quantities for variables expressed in per unit

Throughout the chapter some variables are expressed as per unit values. The following base quantities are defined and used throughout the thesis:

$$V_{base} = V_{DCn} \tag{3.1}$$

$$P_{base} = P_{DCn} \tag{3.2}$$

$$I_{base} = \frac{P_{DCn}}{V_{DCn}} \tag{3.3}$$

$$V_{C_{base}} = \frac{V_{DCn}}{N} \tag{3.4}$$

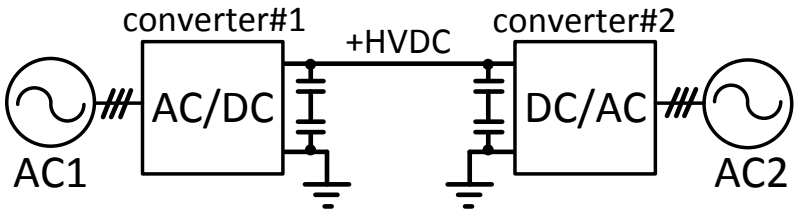
Where,

- V_{DCn}: DC system nominal voltage (V)
- P_{DCn}: DC system nominal power (W)
- N: Number of cells in a DBS converter valve (-)
- V_{Cbase}: base voltage used with the DBS cell capacitor voltage (V)

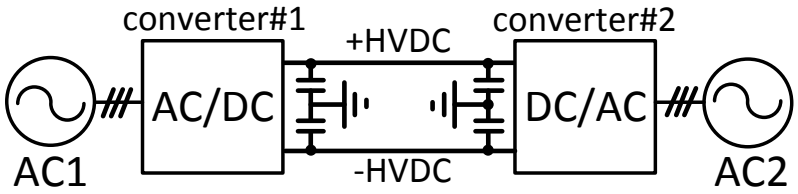
3.1.2 DBS circuit structure for different HVDC system configurations

There is two possible DC system configurations for the implementation of HVDC transmission systems: monopolar (Fig. 3.1a and 3.1b) or bipolar (Fig. 3.1c). For monopolar configurations, a system can be configured as an asymmetric monopole (Fig. 3.1a), with or without metallic return [75], or as a symmetric monopole (Fig. 3.1b).

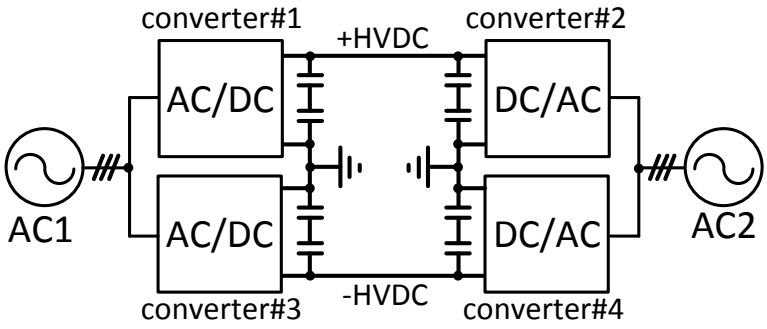
The HVDC system configuration influences the DBS circuit structure. For an asymmetric monopole, the DBS is composed of a single arm connected between the HVDC link positive pole and ground as shown in Fig. 3.2a. In the case of a symmetric monopole or a bipole, two arms, connected between the each pole and ground (Fig. 3.2b), would normally be used, although the use of a single arm between both poles, as for the monopolar case is also an option. The use of two



(a) Monopole configuration.



(b) Symmetrical monopole configuration.



(c) Bipole configuration.

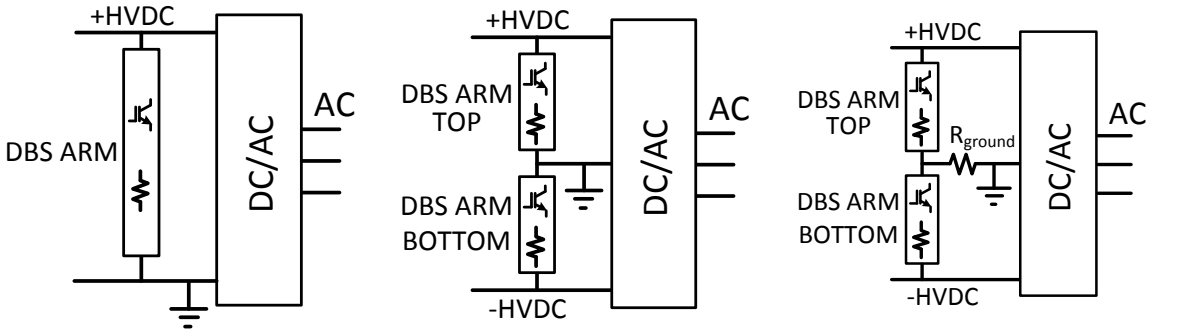
Fig. 3.1 Different HVDC system configurations.

independent arms can be beneficial for protection of the HVDC system during DC side faults. With this configuration, as proposed in [76], the use of a ground resistor (Fig. 3.2c) protects the DBS arms from an over-voltage situation during a pole to ground fault in the HVDC system.

For simplicity, the structure and operation of one DBS arm is presented in the next sections, acknowledging that both arms, in the case of a bipole configuration, are identical and so is their operation.

3.1.3 Braking resistor arrangement

The braking resistor R_{dbs} is the component where power is dissipated in a controlled manner by the operation of the dynamic braking valve (DBS valve). This resistive element however, can have two different configurations. A first option, as displayed in Fig. 3.3a, is to have a lumped resistive element in series



(a) Monopole. (b) Bipole. (c) Bipole with R to ground.

Fig. 3.2 DBS arrangement for different HVDC system configurations.

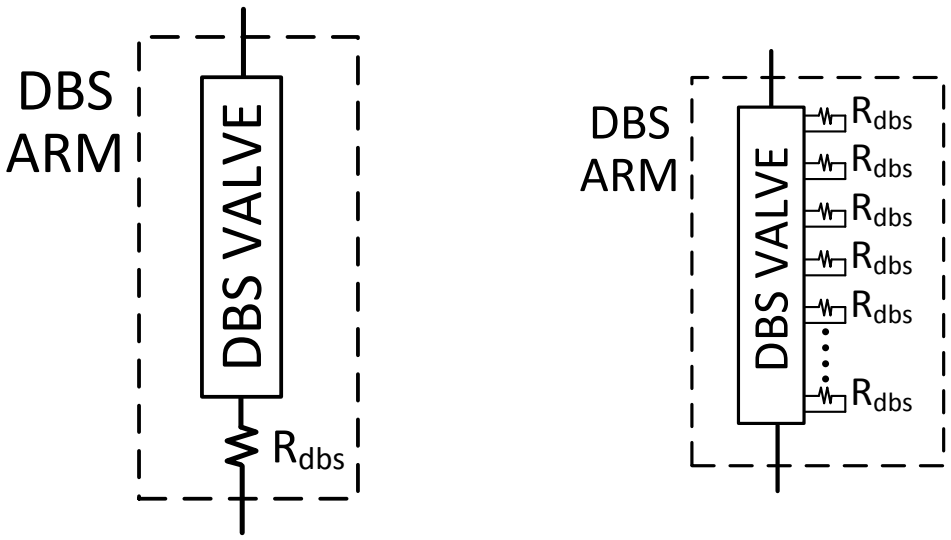
with the DBS valve. This means that the resistor needs to be rated for the full energy required to ride-through the fault, which is determined by the nominal power rating of the HVDC link and the fault ride-through characteristic imposed by the grid code or the TSO. The second option displayed in Fig. 3.3b consists on dividing the resistive element into a number of lower energy rated elements and distributing them along the DBS valve. This allows for a finer control of the dissipated power but requires an increase in the total number of components and electrical connections.

3.1.4 Operation regions for the DBS

HVDC transmission systems are equipped with some standard mechanisms for protection against DC side over-voltages. The main protective devices are surge arresters and protection actions implemented in the VSC controller. The surge arresters protect the different parts of the system against transient over-voltages caused by lightning or switching surges. A typical arrangement of surge arresters for a VSC-HVDC system is shown in Fig. 3.4 [77, 78]. The VSC controller over-voltage limitation [79] protects the HVDC system from a permanent over-voltage situation. It stops the operation of the transmission system, following a standard converter disconnection sequence, by blocking the converter and opening the AC breakers. In [80] a 1.3 pu over-voltage level is used as the level for this protection mechanism.

The operation regions of a DBS system have to be defined to avoid an overlap with the standard protection mechanisms for the case of a permanent over-voltage situation in the DC line, being the DBS the first level of protection. Only in an eventual failure of the DBS, should the alternative protection mechanisms be triggered.

Two limits are proposed in this work for the operation regions of the DBS, the upper over-voltage limit (UOVL) and the lower over-voltage limit (LOVL).



(a) Lumped resistor.

(b) Distributed resistors.

Fig. 3.3 Different braking resistor arrangements.

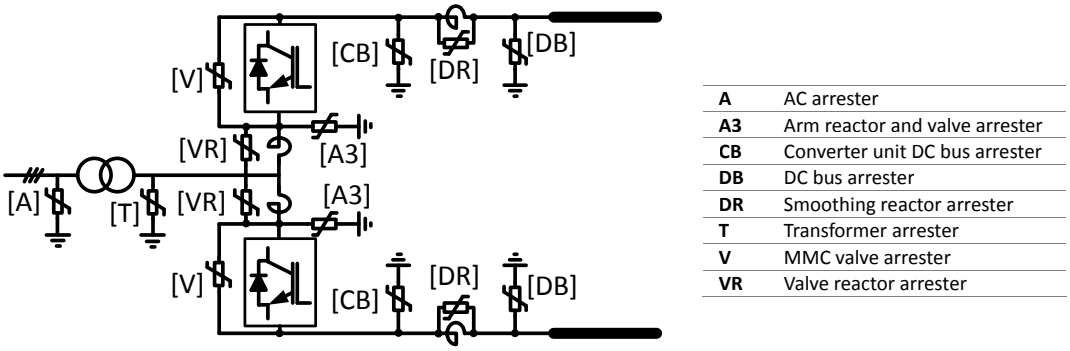


Fig. 3.4 Typical VSC-HVDC converter station arrester locations.

The operation of the DBS is controlled as follows according to the evolution of the DC link voltage during a fault event:

- When $V_{DC} < LOVL$: the DBS does not operate.
- When $LOVL \leq V_{DC} < UOVL$: The DBS power dissipation is proportional to the over-voltage level.
- When $V_{DC} \geq UOVL$: The DBS dissipates maximum power ($\frac{V_{DC}^2}{R_{dbs}}$).

The LOVL value is set to be higher than the maximum DC voltage expected during normal operation of the DC transmission system. In [81] a 1.05 pu limit is chosen to have enough margin to avoid the activation of the DBS due to the transient events and voltage ripple in the DC link. The same value has been chosen in this work. The UOVL sets the maximum expected DC voltage in the HVDC cable during a fault event. Therefore its value should be set below the

voltage limit that triggers the operation of the surge arrestors and the VSC station over-voltage protection. A value of 1.1 pu has been chosen in this work, well below the 1.3 pu level for the activation of the VSC converter protections. These values are used throughout the thesis for the simulations and the experimental work with the DBS circuits and are displayed in Table 3.1.

Table 3.1 Limits of the DBS operation for this research project.

OPERATION LIMITS FOR THE DBS CONTROLLER	
Upper over-voltage limit (UOVL)	1.1 pu
Lower over-voltage limit (LOVL)	1.05 pu

3.1.5 Periods and frequencies used to describe the operation of the DBS circuits

In order to clarify the nomenclature used throughout the thesis to define the operation of DBS circuits and resulting waveforms, the following periods/frequencies are described here:

- $T_{carrier}(s)$: the period of the triangular carrier signal used in classic pulse width modulation (PWM) for driving a chopper circuit.
- $T_{balancing}(s)$: the execution period of the energy balancing algorithms which are needed with all the DBS circuits based on multilevel circuits.
- $T_m(s)$: the modulation period used with the DBS circuits that utilize trapezoidal voltage waveforms to modulate the power dissipation on the braking resistor. It is the fundamental period of the trapezoidal voltage pulses used to chop the DC voltage and equivalent to the carrier period from classic PWM.
- $f_{switching}(Hz)$: the resulting switching frequency of the semiconductors in the DBS circuits. It is inversely proportional to $T_{carrier}$ in conventional PWM or to $T_{balancing}$ when implementing energy balancing algorithms with multilevel circuits.

3.2 The HVDC chopper DBS with lumped resistive element

This circuit is the closest representation of the idealized DC chopper normally considered in technical publications [80–85], and the circuit used in the first VSC-HVDC offshore connection project in operation [86]. The original braking

resistor concept, as used in traction applications, is up-scaled to operate at HVDC voltage levels. Fig. 3.5 shows the DBS arm structure for this topology.

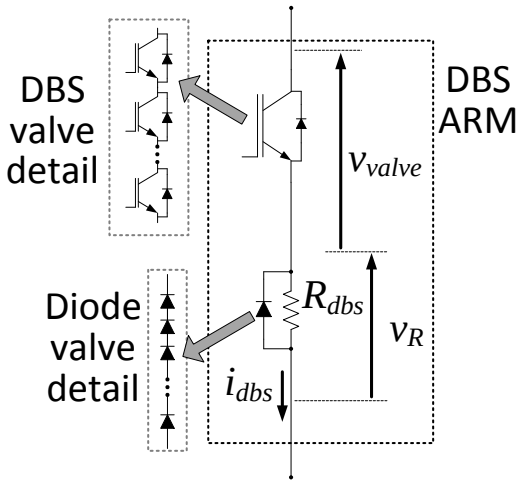


Fig. 3.5 Basic structure of the HVDC chopper DBS circuit.

Focusing on the DBS valve, the use of series connected IGBTs is necessary in order to achieve the voltage rating required for current HVDC transmission systems, which has reached ±320 kV. A lumped resistive element (R_{dbs}) configuration is used in series with the DBS valve, as observed in Fig. 3.5. Since a real resistive device always presents certain amount of parasitic inductance, the use of a diode valve connected in anti-parallel with the braking resistor is necessary. The diode valve provides an alternative current path to discharge the energy stored in the resistor's parasitic inductance when the IGBT valve turns off. In the absence of a diode, this inductance would be left in open-circuit while still charged with some energy, generating high voltages spikes across the DBS valve and stressing the semiconductors. Fig. 3.6 [87], shows a valve of series connected IGBTs used in both the VSC station valves and the DBS valves for the BorWin 1 offshore wind project [86].

3.2.1 Control strategy

Fig. 3.7 shows the block diagram of the developed controller for the HVDC chopper DBS circuit. The system consists of a HVDC voltage open loop control, which starts with the generation of an error signal by using the $LOVL$ value as the reference for the error generation. The signal is then passed through a saturation function, which only allows for V_{err} signal to take positive values. A proportional control action (P) applies a gain to the error signal in order to generate the *duty cycle* command for the pulse-with modulation (PWM) function. The output of the PWM block, *switching signal*, is the gate signal that drives the DBS braking valve semiconductors in order to modulate the voltage on the braking resistor.

Fig. 3.6 Valves of series connected IGBTs (Source: ABB, [87], 2006).

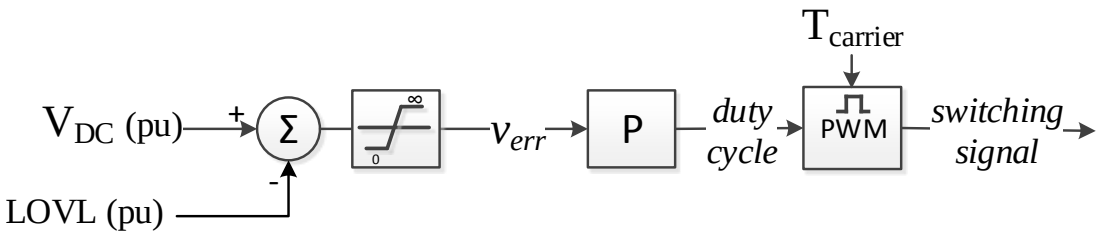


Fig. 3.7 Block diagram of the HVDC chopper DBS proposed controller.

The criteria for setting the proportional gain is to keep the operation of the modulator inhibited (duty cycle = 0) for values of V_{DC} smaller than LOVL and to apply full voltage across the braking resistor (duty cycle = 1) for values of V_{DC} equal or higher than the upper over-voltage limit (UOVL). The expression for the proportional gain is therefore calculated as:

$$k_p = \frac{1}{UOVL - LOVL} \tag{3.5}$$

Fig. 3.8 shows the evolution of the controller internal signals for a varying V_{DC} feedback signal. The over-voltage limits presented in table 3.1 are used in this example.

3.2.2 Braking resistor value

The value of the braking resistor is calculated to dissipate the HVDC system rated power when the DC voltage reaches the UOVL limit. In this way, even under the most severe AC fault when the onshore VSC cannot inject any power into the AC grid, the DC voltage will not exceed UOVL. The resulting resistance expression is:

$$R_{dbs} = \frac{(V_{DCn}\, UOVL)^2}{P_{DCn}} \qquad (\Omega) \tag{3.6}$$

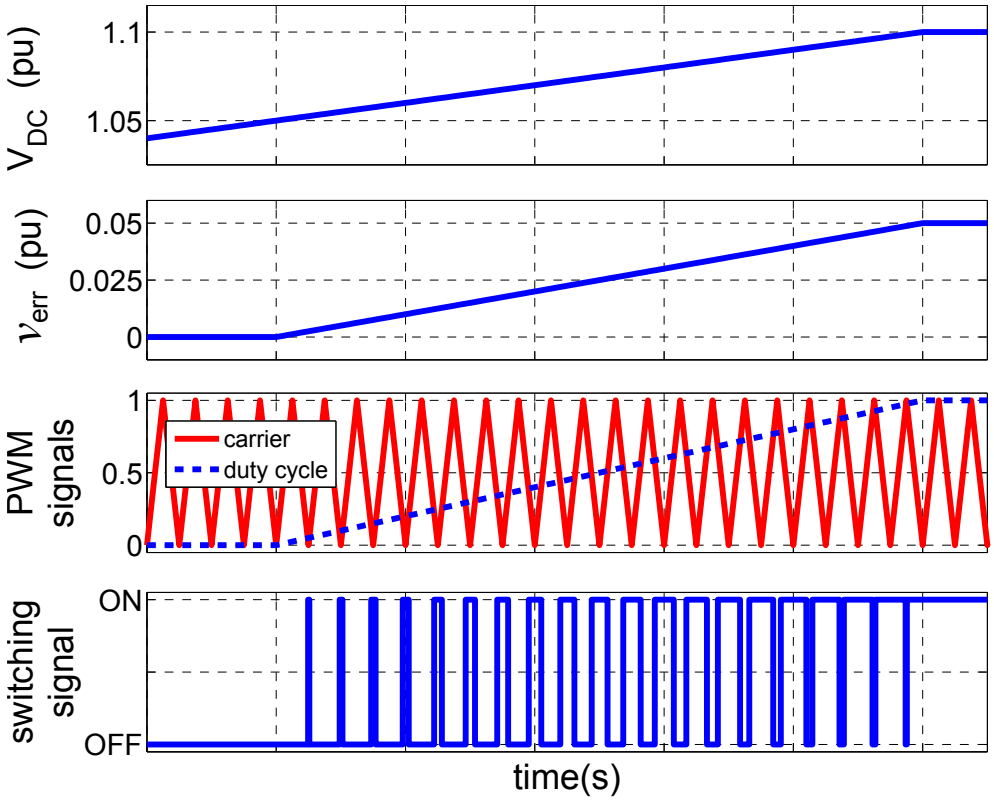


Fig. 3.8 Internal controller signals for the HVDC chopper circuit.

3.3 The multilevel chopper DBS with distributed resistive element

Following a similar trend to the one experienced with VSC converter topologies to overcome the challenge of building and operating valves of series connected IGBTs, multilevel circuits are also proposed for the implementation of dynamic braking systems. The first multilevel circuit to be analysed is described in [67] and [88] and presented here in Fig. 3.9. The name multilevel chopper DBS is chosen to indicate the presence of a reduced power chopper inside each of the cells that serve as building blocks for the braking valve. The presence of this cell-based chopper circuit, leads to the main particularity of this circuit: the use of a distributed braking resistor, as already introduced in section 3.1.2. The internal cell structure is also shown in Fig. 3.9. The cell is composed of two diodes in a halfbridge configuration, in parallel with the cell capacitance C_{cell}. The chopper circuit, an IGBT plus distributed resistor R_{dbs}, is connected across the capacitor terminals. A diode is connected in anti-parallel with the resistor to provide a discharge path for the energy stored in the parasitic inductance when the IGBT is turned off.

The circuit operation does not entail major complexity, and each level can be coordinated to dissipate a fraction of the required total power dissipation.

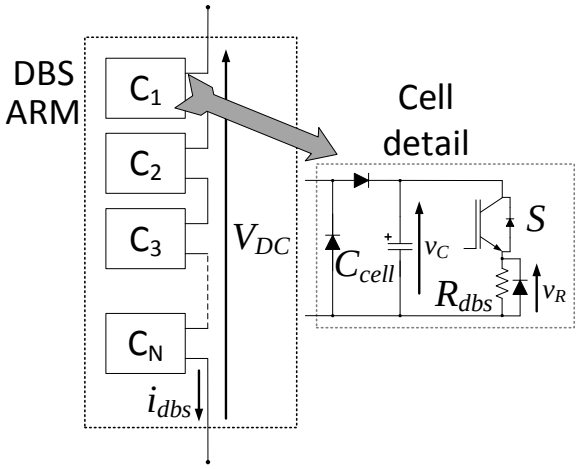


Fig. 3.9 Arm structure of the multilevel chopper DBS circuit.

Considering a DBS arm integrated by a number of cells N, when all the chopper circuits are off, each cell capacitor will be charged on average to a fraction of the HVDC pole voltage, equal to $\bar{V}_C = \frac{V_{DC}}{N}$. When power needs to be dissipated in the cells, the chopper IGBT is turned on, and the cell capacitor voltage appears across the distributed resistor. This provokes the cell capacitor to discharge into the resistor, dissipating power, and a reduction in the cell capacitor voltage. This voltage reduction generates an unbalance between the DBS arm total voltage and the HVDC voltage, forcing a current to flow through the DBS. This current (i_{dbs}) always flows with positive polarity according to the notation in Fig. 3.9. The consequence is that in those cells where the chopper IGBT (S) is turned off, the current flows through the capacitor, which stores energy and causes an increase in the cell voltage. Fig. 3.10 illustrates the two different cell commutation states as explained in this last paragraph.

The particularity with this mechanism of local power dissipation is the resulting stepped characteristic of the DBS current. The steady-state DBS current can be controlled by switching the DBS transistors. If the cell capacitor voltages are assumed ripple free, this gives a current resolution of:

$$\frac{I_{DBSn}}{N} = \frac{P_{DCn}}{N\,V_{DCn}} \tag{3.7}$$

Where,

- I_{DBSn}: nominal current through the DBS circuit when nominal power is dissipated (A)

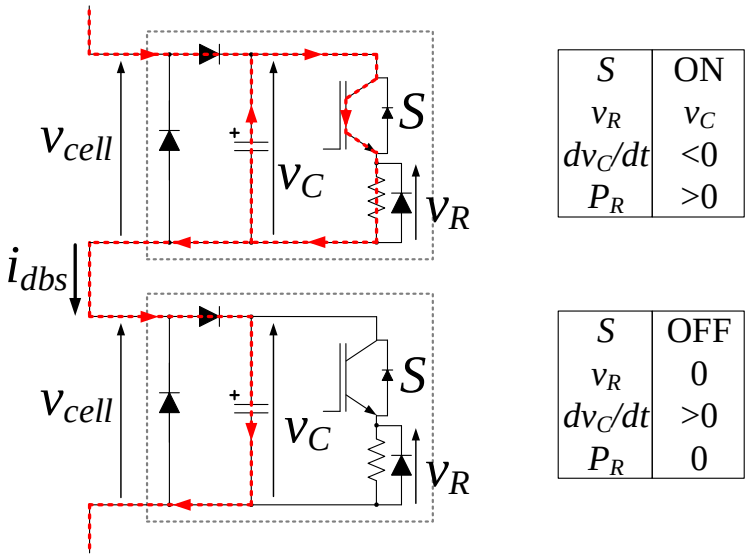


Fig. 3.10 Possible commutation states for the multilevel chopper DBS cells.

3.3.1 Control strategy

Fig. 3.11 presents the block diagram of the developed controller for the multilevel chopper circuit. The first section of the diagram is identical to the controller for the HVDC chopper circuit presented in Fig. 3.7, with the error generation, the saturation of the error signal and the proportional controller. In this case the power modulation stage contains the balancing algorithm.

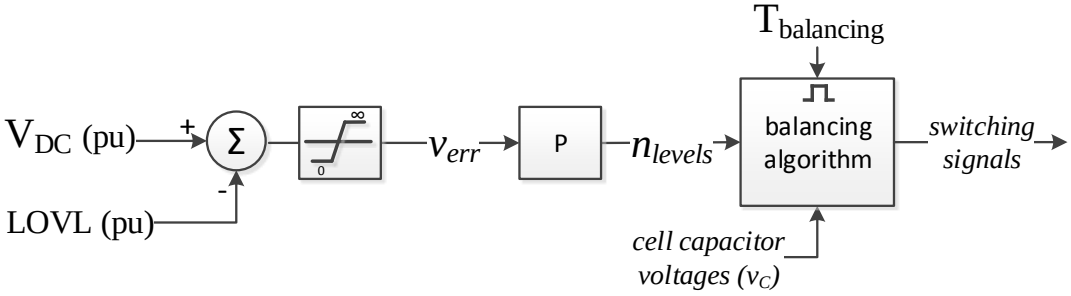


Fig. 3.11 Block diagram of the multilevel chopper DBS proposed controller.

Energy balancing is needed in converters using MMC type cells to ensure an even distribution of the total arm stored energy among the cells. Energy is stored inside each cell capacitances, so ensuring an even distribution also ensures that all the cells can produce the same voltage level and prevents an over-voltage occurring in some cells, which could result in the destruction of the capacitor and the semiconductors. The balancing algorithm receives the demand of the number of cells that need to be "ON" at any given time from the proportional controller. It then generates the switching signal for the IGBT inside each cell according to

the state of charge of the cell capacitor in order to maintain the voltages well balanced around an average value.

The principle to generate the demand for the balancing algorithm, n_{levels} which is the number of cells with transistors turned on, is simple: when no power dissipation is required, the demand is zero, and when full power dissipation is needed, the demand equals the total number of cells in the DBS arm, N. Therefore, the required proportional gain is calculated as:

$$k_p = \frac{N}{UOVL - LOVL} \tag{3.8}$$

The balancing algorithm flow diagram is displayed in Fig. 3.12. First, the cells are sorted according their capacitor voltage value. After, the chopper circuit in the n_{levels} cells with the higher voltage level is switched on, while keeping the circuits in the other cells off. The function is executed periodically at $T_{balancing}$. This execution period defines the switching frequency of the cell IGBT and the voltage ripple in the cell capacitors. The shorter $T_{balancing}$, the higher the IGBTs switching frequency and the smaller the voltage ripple in the capacitors.

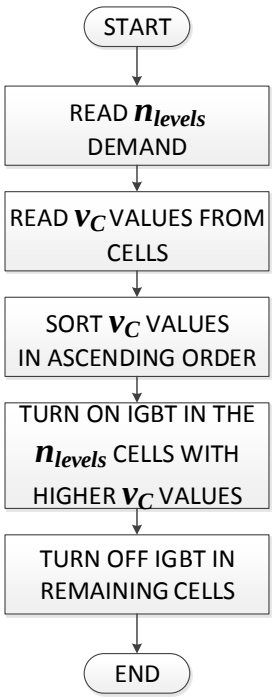


Fig. 3.12 Flow diagram for balancing algorithm in the multilevel chopper circuit.

Fig. 3.13 shows the controller internal signals when the DC link voltage V_{DC} is gradually increased up to 1.1 pu (UOVL). In this way the DBS gradually dissipates more power and the evolution of the DBS internal signals is observed from zero to nominal power dissipation. For simplicity, a system with only four cells, as opposed to the hundreds of cell in a real scale system, is shown here. It

is observed how the output of the proportional controller, n_{levels}, is discretized according to the total number of cells in the DBS valve. The discretized value is passed to the balancing algorithm. Looking at the cell gate pulses (switching signals) it is observed how with the cellular structure, the effective switching frequency of each individual IGBT is reduced with respect to that of the series connected IGBTs in the HVDC chopper. This reduces the losses in the semiconductors and allows for higher switching frequencies to be utilized, which translates in waveforms with less ripple, a well know characteristic of multilevel converters. Last, the operation of the balancing algorithm is shown with the v_C graph. The rotation of cells is observed with the discharge of the cells with the higher capacitor voltage in order to keep the balance.

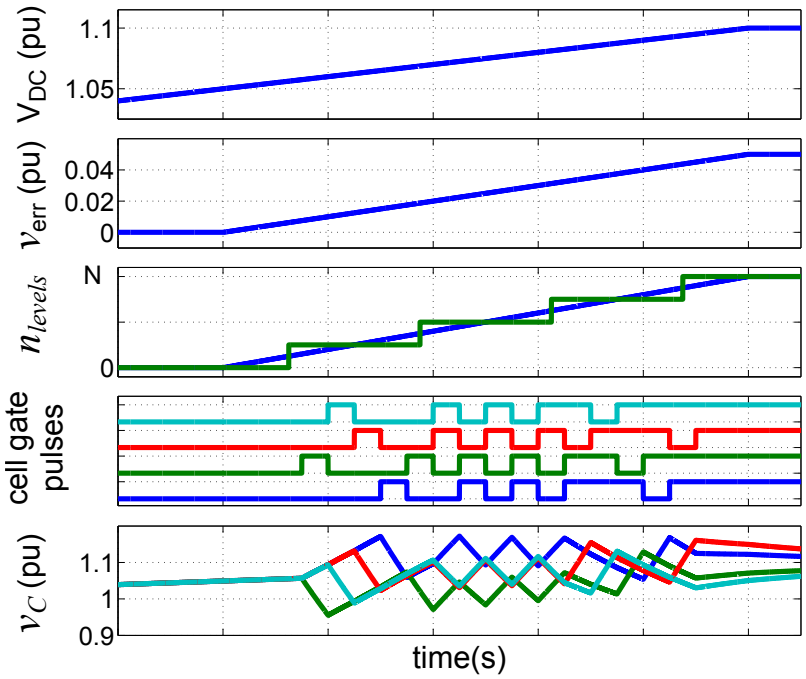


Fig. 3.13 Internal controller signals for the multilevel chopper circuit.

3.3.2 Braking resistor value

The value of the distributed braking resistors is calculated to dissipate HVDC system rated power when the HVDC system voltage reaches the upper over-voltage limit (UOVL). At that point all the chopper circuits dissipate power simultaneously. Therefore the value of the individual distributed resistors can be calculated as:

$$R_{dbs} = \frac{(V_{DCn}\, UOVL)^2}{P_{DCn}\, N} \tag{3.9}$$

3.3.3 Cell capacitor sizing

The allowed ripple in the cell capacitor voltage together with the DBS current and the execution period of the balancing algorithms are the main parameters to consider for sizing the cell capacitance. The stepped characteristic of the DBS current as seen in Fig. 3.14 results in discrete levels of power dissipation in the cell. It can also be observed how for low and high power dissipation levels (left and right ends of the plot), the switching frequency of the individual cells is lower than in the central region, where the power dissipation is half the nominal power. The reduced switching frequency translates into most of the cells being "ON" or "OFF" for most of the time, which makes the cell voltage ripple slightly higher during these two regions. This is compensated by the fact that during the low power dissipation region, with most cell capacitors in the current path, the current through the DBS is also low and for high power dissipation, where the DBS current is high, most cells capacitors are not in the current path. This helps keeping the cell capacitor voltage ripple fairly constant during the entire operation range, despite the change in the DBS current value.

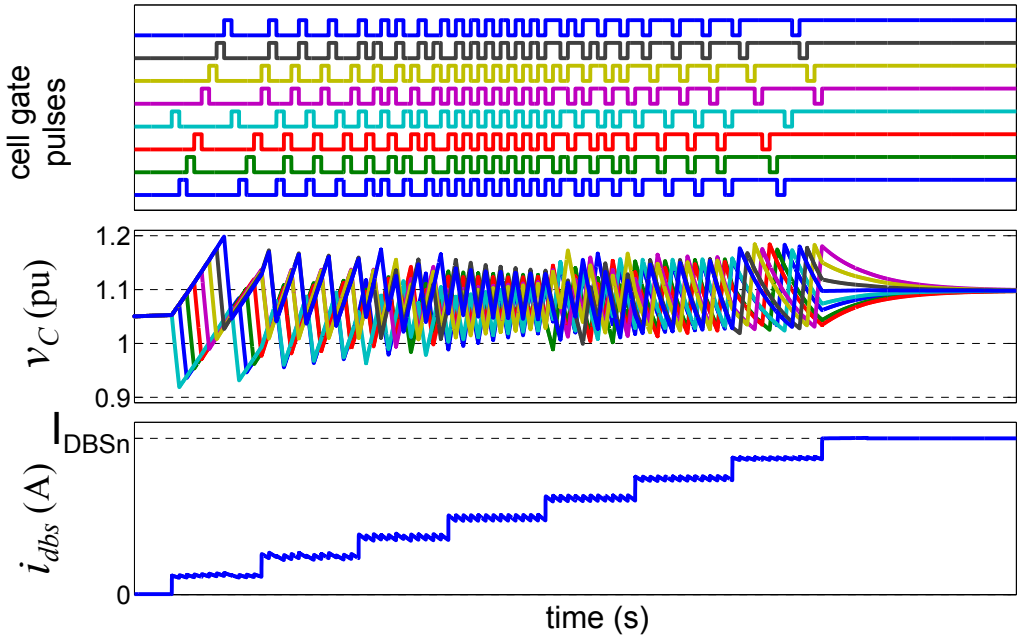


Fig. 3.14 Capacitor balancing signals detail in the multilevel chopper circuit.

For a given level of DC over-voltage, the DBS current in the arm is:

$$I_{DBS} = \frac{P_{DBS}}{V_{DC}} \tag{3.10}$$

Where,

- P_{DBS}: level of power dissipation in the DBS circuit (W)
- V_{DC}: DC link voltage (V)

The relation between the required number of active cells with respect to the total number of cells in the arm can be assimilated to an equivalent modulation index for the circuit, and is expressed as:

$$\frac{n_{levels}}{N} = \frac{P_{DBS}}{P_{DCn}} \tag{3.11}$$

The peak-to-peak ripple in the DBS cell capacitor voltage can therefore be expressed in volts as:

$$\Delta V_C = I_{DBS} \frac{n_{levels}}{N} \frac{T_{balancing}}{C_{cell}} \tag{3.12}$$

And replacing (3.10) and (3.11) in (3.12):

$$\Delta V_C = \frac{P_{DBS}^2 T_{balancing}}{V_{DC} P_{DCn} C_{cell}} \tag{3.13}$$

Considering the DBS dissipates nominal DC power (P_{DCn}) when the maximum over-voltage ($V_{DC} = V_{DCn} UOVL$) is reached, modifying (3.13) the required cell capacitance value can be expressed as:

$$C_{cell} = \frac{P_{DCn} T_{balancing}}{V_{DCn} UOVL \Delta V_C} \tag{3.14}$$

Where,

- n_{levels}: required number of active cells generated by the P controller of the multievel chopper DBS $(-)$
- n_{levels}: Value of the cell capacitance in the modular DBS circuits (F)
- ΔV_C: Peak-to-peak voltage ripple in the modular DBS cell capacitors (V)

3.4 The half-bridge multilevel DBS circuit with lumped resistive element

This alternative multilevel circuit for the implementation of a DBS is based on half-bridge cells like the ones used in the modular multilevel voltage source converters (MMC or M^2C), and therefore it might be interesting for manufacturers offering HVDC schemes based on the MMC technology. The basic arm structure is shown in Fig. 3.15. Half-bridge cells are connected in series forming the DBS braking valve, and the valve is connected in series with the lumped resistive element. The only reference to this circuit is found in a patent

application [89], where no information is given regarding the control methodology and operation of the circuit.

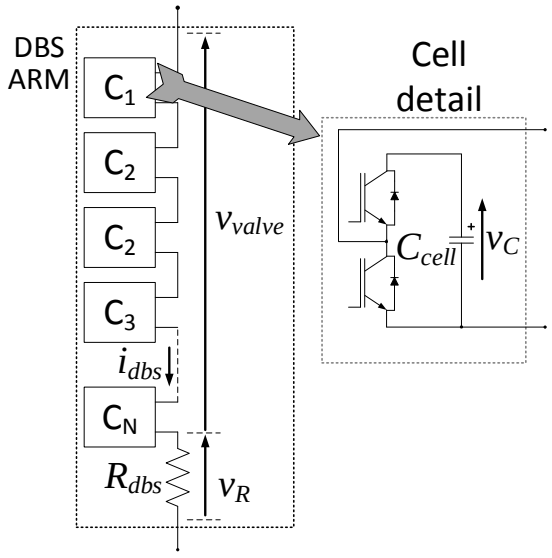
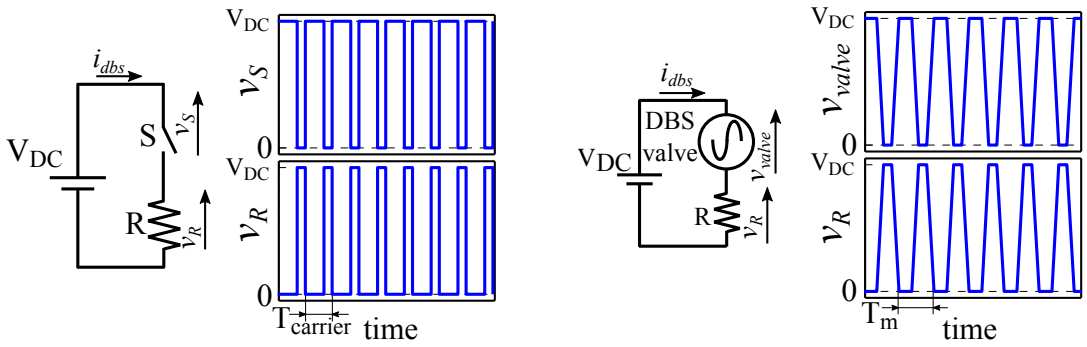


Fig. 3.15 Arm structure of the half-bridge multilevel DBS circuit.

3.4.1 Trapezoidal waveforms for power modulation

The use of trapezoidal voltages to modulate the power dissipated in a resistor has been previously proposed in [76]. As opposed to the high dv/dt voltage pulses resulting from standard PWM, the use of trapezoids allows to control the dv/dt of the voltage during the ramping up/down periods. This presents the benefit of reduced stress in semiconductor switches, passive components as well as reduced radiated EMI.

Multilevel valves in a DBS, as presented in Fig. 3.15, behave as controlled voltage sources (Fig. 3.16b). This flexibility can be used to implement the desired trapezoidal modulation. Fig. 3.16 presents the comparison between the classic PWM and the proposed modulation based on trapezoidal pulses. Both methods follow the same principle of chopping the DC voltage to produce voltage pulses across the resistor at a fixed period defined here as $T_{carrier}$ for PWM and T_m for the trapezoidal modulation. The width of the voltage pulse can be modulated (varied) in both cases from 0 to $T_{carrier}/T_m$ to adjust the average voltage applied across the resistor from 0 to V_DC. In this way average power dissipation is regulated.



(a) Classic PWM. (b) Trapezoidal modulation.

Fig. 3.16 Comparison between classic PWM and trapezoidal modulation.

The main challenge to overcome with the trapezoidal modulation is to maintain the total energy stored in the DBS valve constant while dissipating the required power in the braking resistor. The expression of the power on the DBS valve is (Fig. 3.16b):

$$p_{valve} = v_{valve}\, i_{dbs} \tag{3.15}$$

Where,

- p_{valve}: is the instantaneous power on the DBS valve (W)
- v_{valve}: is the voltage generated by the DBS valve (V)
- i_{dbs}: is the current through the DBS valve and braking resistor (W)

In the example shown in Fig. 3.16b, both the valve voltage (v_{valve}) and the DBS current (i_{dbs}) are positive according to the notation in the figure. Therefore the valve power is always positive and the valve energy will increase indefinitely. If no corrective action is taken, this energy that is stored in the valve cell capacitors will eventually lead to an over-voltage situation in the cells.

In order to maintain the energy stored in the DBS balanced around a target value, over one modulation period (T_m), negative power needs to be forced on the DBS valve during certain time in order to discharge the excess of energy stored during the time the valve generates positive power, so that a zero net energy exchange is achieved in the valve over one modulation period. This is expressed as:

$$\Delta E_{valve} = \int_{t}^{t+T_m} p_{valve}\, dt = \int_{t}^{t+T_m} v_{valve}\, i_{dbs}\, dt = 0 \tag{3.16}$$

Where,

- ΔE_{valve}: variation of energy stored inside the DBS valve over one modulation period (J)

From (3.15) and (3.16) it is observed that in order to produce negative power on the DBS valve, either the valve voltage or the current polarity needs to be reversed during part of T_m. A more detailed description of the trapezoidal waveforms proposed in this thesis work to accomplish this goal is given in sections 3.4.2 and 3.5.1.

3.4.2 Trapezoidal power modulation with the half-bridge multilevel DBS

The half-bridge cells, as shown in Fig. 3.17, can only generate zero voltage or voltage of positive polarity across their terminals (v_{cell}). Since v_{valve} results from the aggregation of all the individual cell voltages, only zero voltage or voltage with positive polarity can be generated. Therefore to achieve the required energy balance(3.16) the polarity of i_{dbs} needs to be reversed during certain parts of T_m.

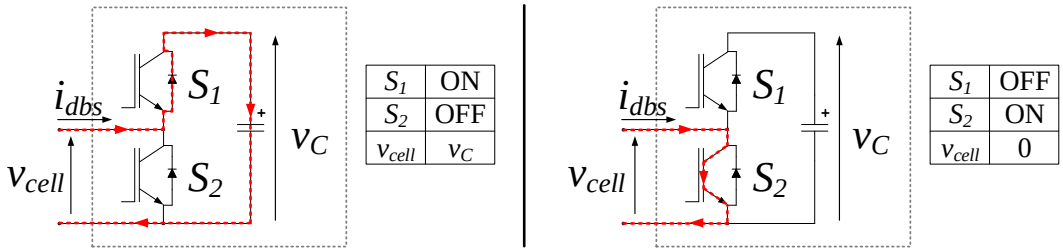


Fig. 3.17 Possible commutation states of the half-bridge cells.

The proposed trapezoidal voltage pulse to be used with the half-bridge multilevel DBS is presented in Fig. 3.18. In order to reverse the polarity of i_{dbs}, the valve voltage needs to be greater than V_{DC} during certain subintervals of T_m. This is achieved by generating a voltage of V_{DC}+V_A during subinterval T_5. The resulting negative voltage across R_{dbs} forces i_{dbs} to reverse polarity.

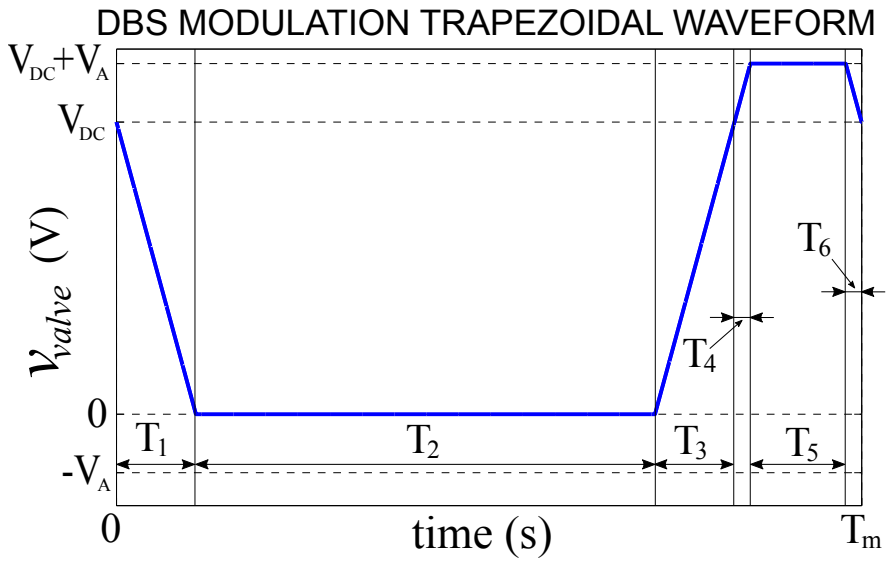


Fig. 3.18 Trapezoidal pulse for the half-bridge multilevel DBS modulation.

Fig. 3.19 illustrates the operation of the DBS and the internal energy variation over one modulation period using the proposed trapezoidal waveform. As observed, the valve generates positive power during subintervals T_1/T_3 during the voltage ramping down/up process. This produces an increase of the energy stored in the valve. As the valve voltage increases above V_{DC}, i_{dbs} changes polarity and negative power is produced on the valve during subintervals T_4, T_5 and T_6, discharging the valve from the excess of energy. During T_2, as v_{valve} is zero, the valve energy remains constant.

The resulting braking resistor voltage (v_R), instantaneous power (p_R) and average power ($\bar{P}_R$) dissipation are also displayed in the figure.

The valve voltage derivative (dv/dt) during the ramping up/down subintervals, the value of voltage V_A and the modulation period T_m are the design parameters and the criteria to choose them will be later discussed in section 3.6. The duration of the different subintervals of the modulation period T_m are the parameters that need to be adjusted in order to achieve the desired level of power dissipation in the braking resistor as well as to ensure the energy balance in the DBS valve.

A design choice has been made in this thesis work to operate at a constant dv/dt when using trapezoidal modulation. The objective, as already stated, is to keep the stress on semiconductors and passive elements of the circuit as well as radiated EMI undisturbed for the entire operation range of the DBS circuits.

The trapezoidal pulse shown in Fig. 3.18 represents the maximum possible width of the voltage pulse and therefore the maximum power dissipation in the braking resistor, equivalent to operating at duty cycle equal to 1 with classic PWM. In order to modulate the power dissipation in the resistor from zero to nominal power, the trapezoidal pulse width needs to be varied while ensuring the

valve energy balance. The proposed modulation strategy is described next.

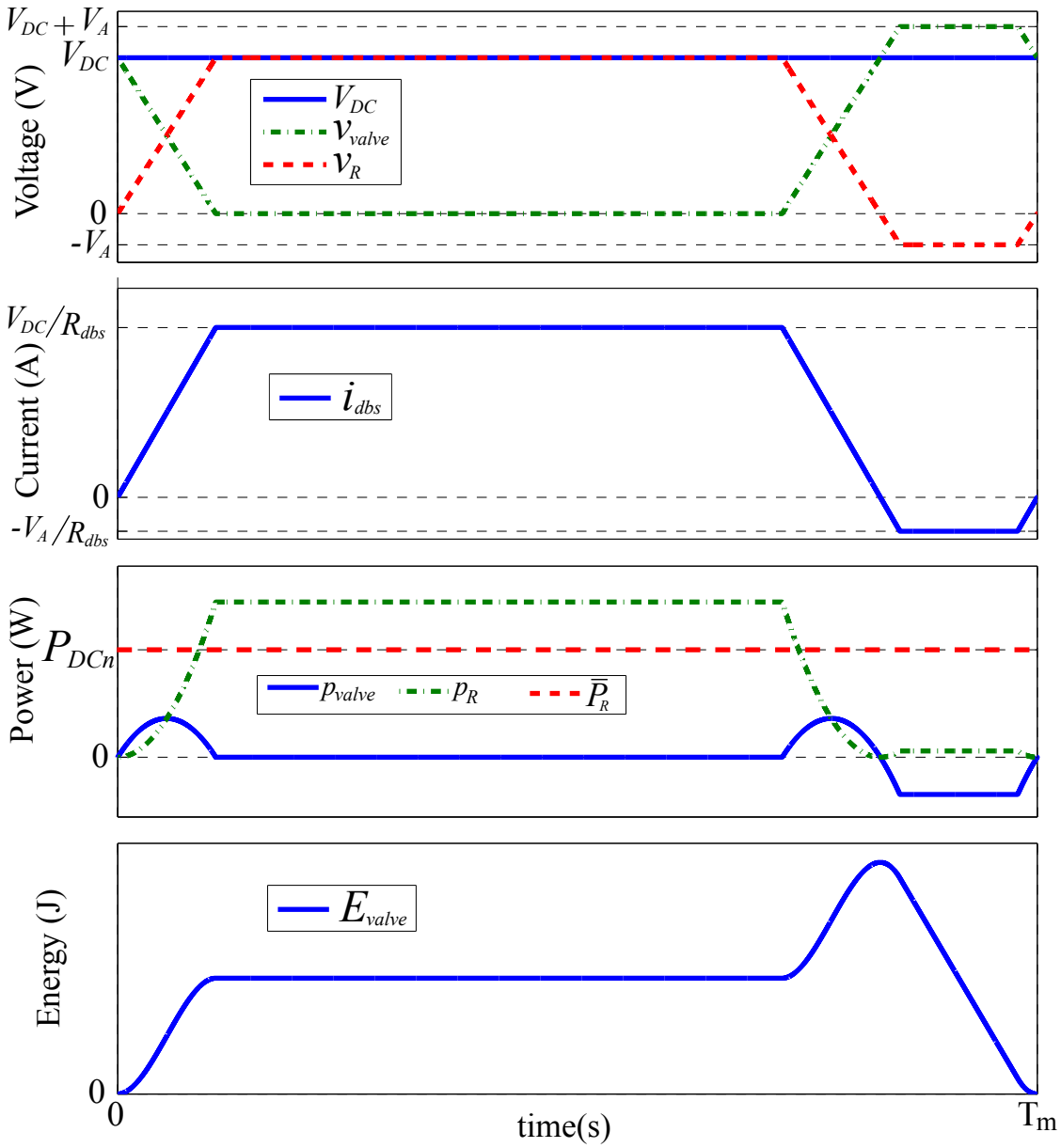


Fig. 3.19 Detail of the DBS arm waveforms over one modulation period with the half-bridge multilevel DBS.

Power modulation strategy

To dynamically vary the level of power dissipation in the braking resistor from zero to nominal power (P_{DCn}) using the proposed trapezoidal pulse, two different regions of operation are needed. These are presented in Fig. 3.20.

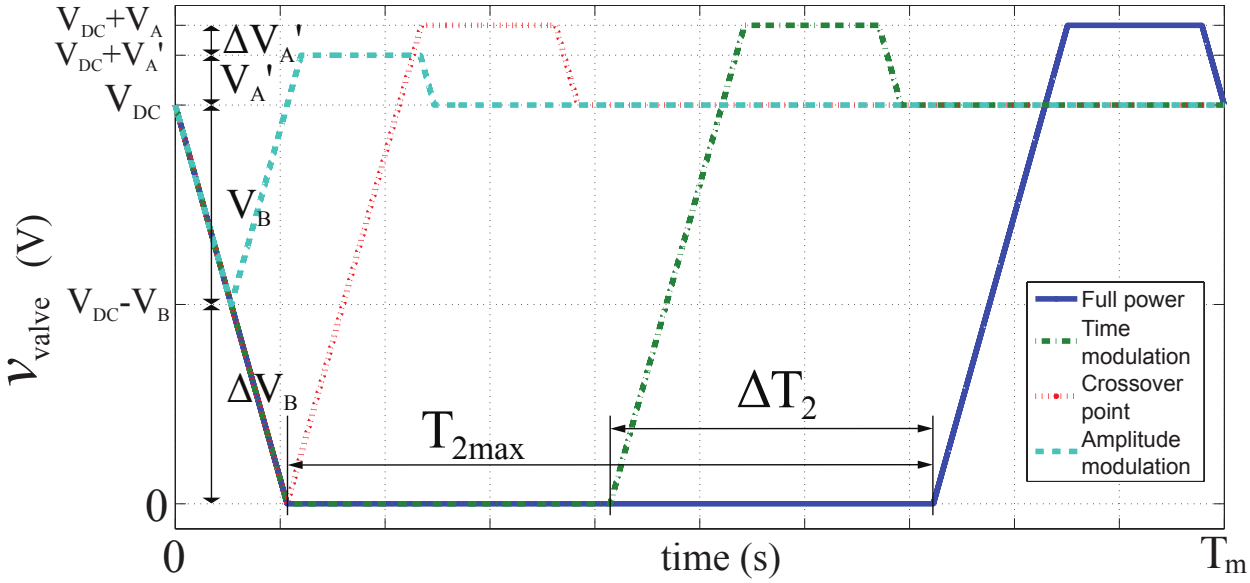


Fig. 3.20 Valve trapezoidal voltage for different operation regions of the modulation strategy.

For the first region, *"time modulation"* is used. As explained, the trapezoidal pulse in Fig. 3.18 represents the maximum power dissipation (maximum average voltage) in the braking resistor. In order to reduce the power dissipation, the width of the voltage pulse applied to the braking resistors ($V_{DC} - v_{valve}$) needs to be reduced. This is achieved by reducing the duration of subinterval T_2 from its maximum value T_{2max} as displayed in Fig. 3.20. Since during T_2 the valve energy does not change, this change in duration does not affect the valve energy balance, and all the duration of all other subintervals and amplitude of V_A can be kept unchanged. When the duration of T_2 is reduced down to zero, the power cannot be further reduced using this method. This is defined as the crossover point, where a change in modulation strategy is required.

At the crossover point, the second modulation region is entered to further reduce the power dissipation down to zero. In this second region, *"amplitude modulation"* is used. The duration of the ramping up/down subintervals T_1/T_3 is reduced while keeping a constant dv/dt and as a result v_{valve} no longer goes down to zero. This reduces the amplitude of the voltage pulse applied across the braking resistor, hence the name for this second modulation region. This does however reduce the amount of energy stored in the valve during $T1$ and $T3$. To compensate for this reduction and maintain the cell energy balance a reduction of the duration of subinterval T_5 and the amplitude of V_A are needed. The new reduced amplitude is defined as V_A' and represents the peak negative voltage across R_{dbs}. The voltage amplitude V_B represents the peak positive voltage across R_{dbs}.

A set of mathematical equations is necessary to fully characterize the modulation process and to adjust the different parameters to achieve the required level of power dissipation while keeping the valve energy balance. The expressions

for valve power and energy as well as the energy dissipation in the braking resistor for subintervals ($T_1..T_6$) are derived in appendix A. These are used to study the energy balance in the DBS valve presented next.

DBS valve energy balance and required braking resistor value

The energy balance in the valve, already introduced with expression (3.16), can be expressed as a function of the valve energy variation during the different modulation subintervals:

$$\begin{aligned}\Delta E_{valveT1} + \Delta E_{valveT2} + \Delta E_{valveT3} + \Delta E_{valveT4} + \Delta E_{valveT5} + \Delta E_{valveT6} = 0 \Longrightarrow \\ \Longrightarrow 2\,\Delta E_{valveT1} + \Delta E_{valveT2} + 2\,\Delta E_{valveT4} + \Delta E_{valveT5} = 0\end{aligned} \tag{3.17}$$

Replacing with values (A.5), (A.7), (A.13) and (A.18) from section A.1 in appendix A, and solving the equation, the value for the required duration of subinterval T_5 in the time modulation region, to ensure the energy balance for a given value of V_A and dv/dt (design parameters) is:

$$T_{5max} = \frac{{V_{DC}}^2 - V_{DC}\,V_A - 2\,{V_A}^2}{3\,V_A\,dv/dt} \tag{3.18}$$

Where,

- $T_1..T_6$: are the different subintervals of the trapezoidal modulation period (s)
- V_A: voltage level used in the trapezoidal modulation (V)
- dv/dt: voltage derivative in the DBS valve voltage (V/s)

Given a certain modulation period T_m, the maximum duration of subinterval T_2 (T_{2max} in Fig. 3.20) can also be determined. By replacing the values of T_1, T_4 and T_5 from (A.1), (A.9) and (3.18) respectively, T_2 can be expressed as:

$$\begin{aligned}T_{2max} = T_m - T_1 - T_3 - T_4 - T_5 - T_6 = T_m - 2\,T_1 - 2\,T_4 - T_5 = \\ = T_m - \frac{{V_{DC}}^2 - V_{DC}\,V_A - 2\,{V_A}^2}{3\,V_A\,dv/dt} - \frac{2\,V_A}{dv/dt} - \frac{2\,V_{DC}}{dv/dt}\end{aligned} \tag{3.19}$$

Next, the expression for the braking resistance needed to dissipate the desired maximum average power over one modulation period is derived. With the expressions of the energy in the braking resistor (E_R) during the different subintervals derived in Appendix A, the average power dissipation in the braking

resistor over one modulation period ($\bar{P}_R$ in Fig. 3.19) is expressed as:

$$\begin{aligned}\bar{P}_R = \frac{1}{T_m}\left(E_{RT1} + E_{RT2} + E_{RT3} + E_{RT4} + E_{RT5} + E_{RT6}\right) = \\ = \frac{1}{T_m}\left(2E_{RT1} + E_{RT2} + 2E_{RT4} + E_{RT5}\right)\end{aligned} \tag{3.20}$$

Where,

- $\bar{P}_R$: average power dissipation in the braking resistor over one modulation period (W)
- $E_{RT1}..E_{RT6}$: energy dissipated in the braking ressitor during the different modulation subintervals (J)
- dv/dt: Voltage derivative in the DBS valve voltage (V/s)

Replacing by(A.6), (A.8), (A.14) and (A.19):

$$\bar{P}_R = \frac{3\,{V_A}^2\,dv/dt\,T_5 + 3\,{V_{DC}}^2\,dv/dt\,T_2 + 2\,{V_A}^3 + 2\,{V_{DC}}^3}{3\,R_{dbs}\,T_m\,dv/dt} \tag{3.21}$$

And substituting T_5 and T_2 from (3.18) and (3.19), the expression for the maximum average power dissipation in the braking resistor is:

$$\bar{P}_{R_{max}} = \frac{3\,T_m\,{V_{DC}}^2\,V_A\,dv/dt - V_{DC}\,{V_A}^3 - 3\,{V_{DC}}^2\,{V_A}^2 - 3\,{V_{DC}}^3\,V_A - {V_{DC}}^4}{3\,R_{dbs}\,T_m\,V_A\,dv/dt} \tag{3.22}$$

By solving for R_{dbs} and replacing $\bar{P}_{R_{max}}$ by the nominal power of the HVDC link (P_{DCn}), the required value of the braking resistor is:

$$R_{dbs} = \frac{V_{DC}\left(3\,T_m\,V_{DC}\,V_A\,dv/dt - {V_A}^3 - 3\,V_{DC}\,{V_A}^2 - 3\,{V_{DC}}^2\,V_A - {V_{DC}}^3\right)}{3\,P_{DCn}\,T_m\,V_A\,dv/dt} \tag{3.23}$$

In the time modulation region, the duration of T_2 is reduced from T_{2max} down to zero in order to reduce the amount of power dissipation while T_5 is kept constant at T_{5max}. With the value of the braking resistor already fixed, replacing (3.18) in (3.21) and solving for T_2:

$$T_2 = \frac{3\,\bar{P}_R\,R_{dbs}\,T_m\,dv/dt + V_{DC}\,{V_A}^2 - {V_{DC}}^2\,V_A - 2\,{V_{DC}}^3}{3\,{V_{DC}}^2\,dv/dt} \tag{3.24}$$

Which can be used to determine the required duration of T_2 to dissipate the desired amount of power over one modulation period.

When T_2 is reduced to zero, the *crossover point* is reached, the power cannot be further reduced, and the amplitude modulation region is entered. The new set

of equations to characterize the modulation process in this region are derived in section A.2 of appendix A.

Voltages V'_A, V_B as well as the duration of subinterval T_5 are the variables to be adjusted to ensure the energy balance. Since T_2 does not exists, the valve energy balance expression for the amplitude modulation region is:

$$\begin{aligned} \Delta E_{valveT1} + \Delta E_{valveT3} + \Delta E_{valveT4} + \Delta E_{valveT5} + \Delta E_{valveT6} = 0 \Longrightarrow \\ \Longrightarrow 2\,\Delta E_{valveT1} + 2\,\Delta E_{valveT4} + \Delta E_{valveT5} = 0 \end{aligned} \tag{3.25}$$

Replacing with (A.24), (A.30) and (A.35) from appendix A, the duration of T_5 as a function of voltages V'_A and V_B to ensure the valve energy balance is:

$$T_5 = \frac{3\,V_{DC}\,{V_B}^2 - 3\,V_{DC}\,{V'_A}^2 - 2\,{V_B}^3 - 2\,{V'_A}^3}{3\,V'_A\,dv/dt\,(V'_A + V_{DC})} \tag{3.26}$$

Where,

- V'_A and V_B: voltage levels used in the trapezoidal modulation (V)

The average power dissipation in the braking resistor equally depends on parameters V'_A, V_B and T_5. Using the expressions of resistor energy from section A.2 of appendix A, the average power dissipation in the amplitude modulation region is:

$$\begin{aligned} \bar{P}_R = \frac{1}{T_m}\left(E_{RT1} + E_{RT3} + E_{RT4} + E_{RT5} + E_{RT6}\right) = \\ = \frac{1}{T_m}\left(2E_{RT1} + 2E_{RT4} + E_{RT5}\right) \end{aligned} \tag{3.27}$$

Replacing with (A.25), (A.31) and (A.36):

$$\bar{P}_R = \frac{3\,{V'_A}^2\,dv/dt\,T_5 + 2\,{V_B}^3 + 2\,{V'_A}^3}{3\,R_{dbs}\,T_m\,dv/dt} \tag{3.28}$$

And substituting T_5 from (3.26) the final expression is:

$$\bar{P}_R = \frac{V_{DC}\,(V_B + V'_A)^2\,\,(2\,V_B - V'_A)}{3\,R_{dbs}\,T_m\,\,(V'_A + V_{DC})\,\,dv/dt} \tag{3.29}$$

In this thesis work the design choice to keep the ratio between V'_A and V_B constant is made. This mimics the situation during the time modulation region where the ratio between V_{DC} and V_A is also kept constant. The reason behind this choice is to keep constant the number of cells in the valve that are needed to generate the voltage amplitude V_A even when variations in V_{DC} occur. This

relation is expressed as:

$$\frac{V_B}{V'_A} = \frac{V_{DC}}{V_A} \tag{3.30}$$

3.4.3 Controller implementation

By making use of the trapezoidal modulation strategy presented in section 3.4.2, the controller for the half-bridge multilevel DBS circuit is implemented. Fig. 3.21 shows the block diagram of the controller that has been developed.

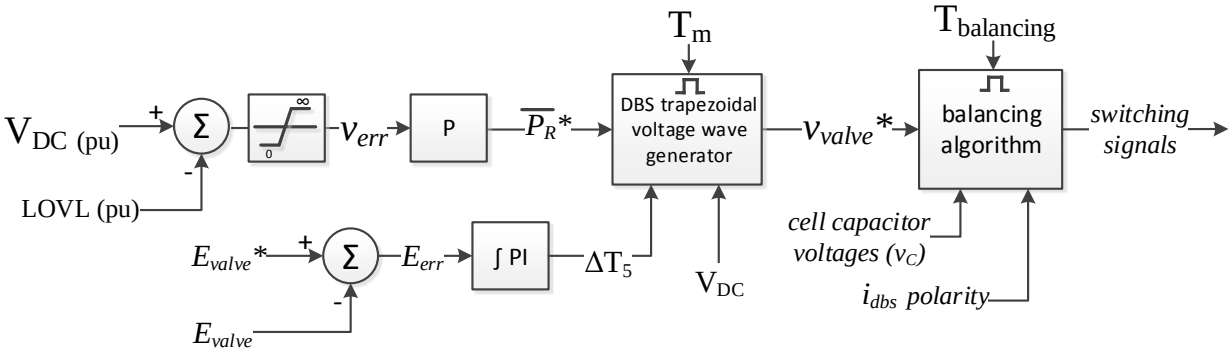


Fig. 3.21 Block diagram of the half-bridge multilevel DBS proposed controller.

The first section with the error generation and the proportional action is the same as for the previous two circuits. The output of the proportional block is the average power dissipation demand for the trapezoidal voltage generation function. The demand is given as a per unit with respect to the HVDC nominal power (P_{DCn}). Nominal power (1) is requested when the DC over-voltage reaches the UOVL limit, and zero power while the over-voltage remains below the LOVL limit. Therefore, the gain for the proportional controller is expressed as:

$$k_p = \frac{1}{UOVL - LOVL} \tag{3.31}$$

Valve energy regulator

An additional proportional-integral (PI) action is included to compensate for deviations of stored energy in the DBS cell capacitors with respect to a target value. The controller receives the valve energy error signal and its output is an offset to modify the duration of subinterval T_5 which is fed to the trapezoidal voltage generator. As already explained, T_5 subinterval affects the exchange of energy between the HVDC system and the DBS and therefore, by modifying its duration, the controller can force the cells to release or accumulate energy, according to the offset polarity.

Equation (3.32) shows the calculation to generate the valve energy feedback, which relies on the individual measured cell capacitor voltages to compute the total stored energy. Equation (3.33) shows the generation of the energy reference value, which uses the measured HVDC voltage to compute the valve energy level which corresponds to an equal distribution of the HVDC voltage among the cell capacitors.

$$E_{valve} = \frac{1}{2} C_{cell} \sum_{n=0}^{N} (v_C(n))^2 \tag{3.32}$$

$$E_{valve}{}^{*} = \frac{1}{2\,N} C_{cell} {V_{DC}}^2 \tag{3.33}$$

Where,

- v_C: voltage in the cell capacitor (V)

Trapezoidal voltage generator

Fig. 3.22 shows the flow diagram for this function. With the constant values for dv/dt, R_{dbs}, T_m and the ratio V_{DC}/V_A fixed during the design stage, and the measured value for V_{DC}, the trapezoidal voltage generation function repetitively reads the power demand input and ΔT_5 offset and calculates the remaining variables to generate the trapezoidal voltage reference. According to the modulation region the function calculates the duration of each subinterval by making use of the equations already presented.

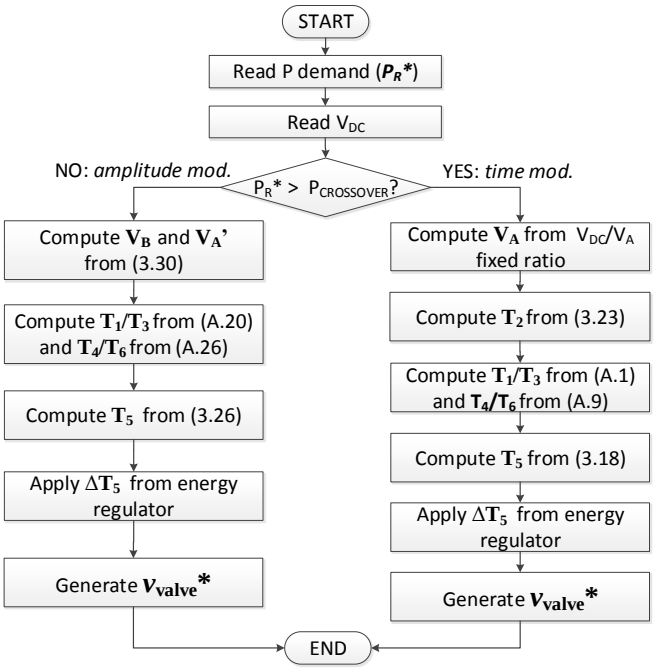


Fig. 3.22 Flow diagram for the trapezoidal generation function.

For operation in the *time modulation* region, T_1/T_3, T_4/T_6 and T_5 are fixed according to expressions (A.1), (A.9) and (3.18). For operation in the *amplitude modulation* region, the values of V_B and V_A' are calculated from (3.29) according to the predefined fixed ratio (3.30). T_1/T_3 and T_4/T_6 are calculated according to (A.20), (A.26) and the required T_5 to maintain the energy balance in the valve is calculated from (3.26) and after the offset from the energy regulator is applied. With these calculations, the function can generate the trapezoidal voltage demand.

Fig. 3.23 shows some of the internal control signals to illustrate the evolution of the trapezoidal valve voltage demand for a varying HVDC voltage amplitude such that the average power dissipation demand varies from 0 to 1 pu.

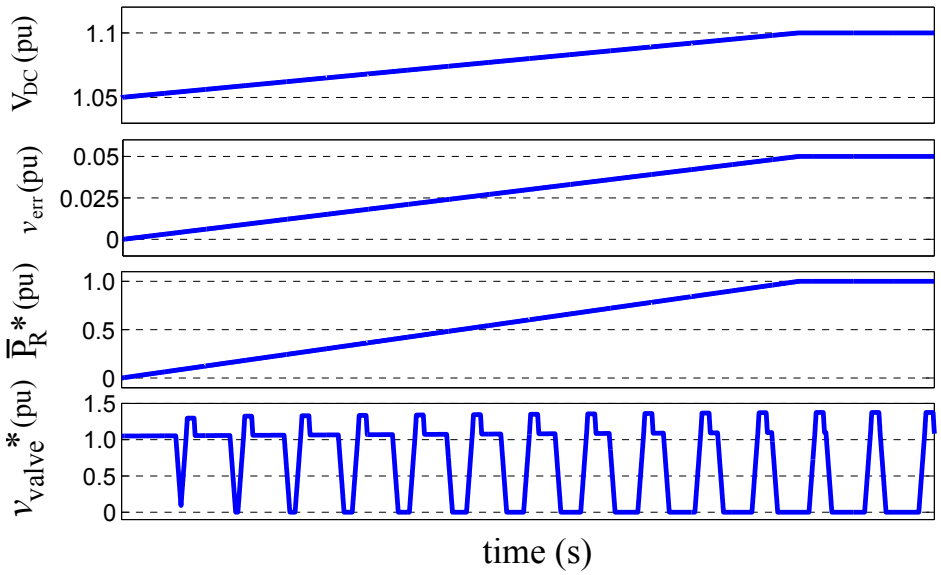


Fig. 3.23 Internal controller signals for the half-bridge multilevel circuit.

Balancing algorithm

Once the trapezoidal voltage demand for the valve is generated, it is received by the balancing algorithm. This function takes into account the capacitor voltage for all cells and the polarity of the current through the DBS valve. Based on them it generates the switching pulses to drive the gate of each IGBT inside the cells, in order to produce the requested DBS valve voltage while keeping the cell capacitor voltages well balanced around an average value. Fig. 3.24 show the flow diagram for the balancing algorithm. Fig. 3.25 shows the results of the balancing algorithm operation. It can be observed how the execution period of the algorithm has a direct impact on the quality of the generated trapezoidal pulses. In this simplified example, only 8 cells are utilized, and the ratio between subinterval T_1 $T_{balancing}$ is 4.4. As observed in the image, this allows for only 4 to 5 switching events, which translate in voltage steps, to take place during the ramping-down and ramping-up events for T_1 and T_3 subintervals. The shorter the balancing

period, the better the approximation of the generated valve voltage to the ideal trapezoidal ramps. The main limiting factor here is the achievable control loop rate with the controller, which includes the voltage and current measurement delays, delays in the communication channels between the cells and the control hardware, computing delays in the control hardware and delays of the individual gate drivers inside the cells.

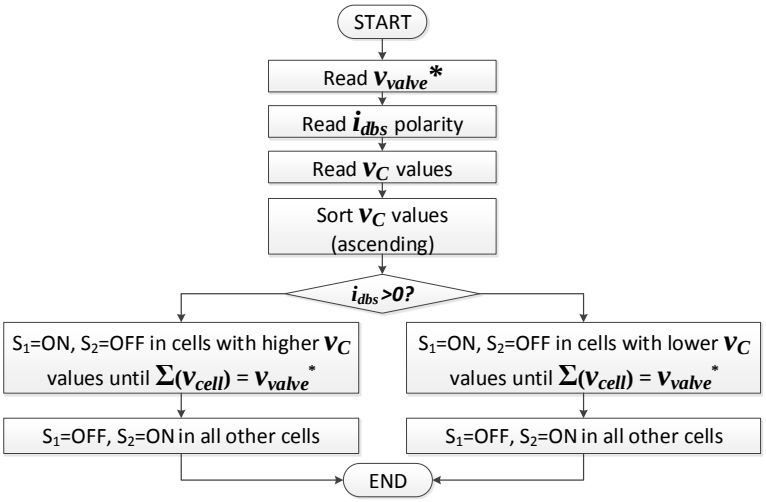


Fig. 3.24 Flow diagram for balancing algorithm in half-bridge multilevel circuit.

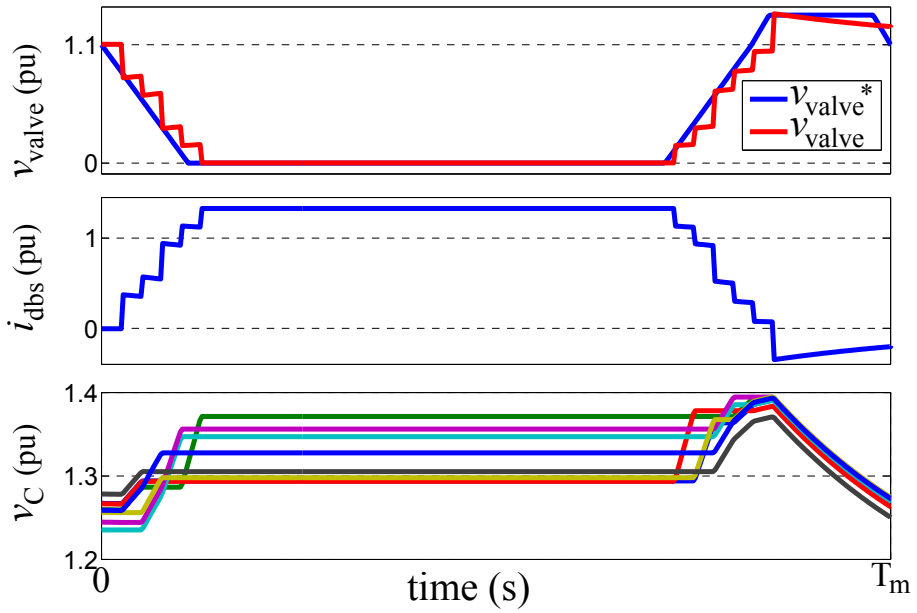


Fig. 3.25 Capacitor balancing signals detail in the half-bridge multilevel circuit.

3.4.4 Cell capacitor sizing

In order to derive the expression of the required cell capacitance, Fig. 3.25 allows for a detailed analysis of the signals which have an influence on the required capacitance during the operation at full power dissipation, this is, when

V_{DC} reaches the upper over-voltage limit ($UOVL$). The top plot in the figure shows the trapezoidal valve voltage demand and real generated voltage. The different subintervals in the trapezoidal voltage can be identified as per Fig. 3.18. The capacitors charge during subintervals T_1 and T_3, and discharge during subintervals T_4, T_5 and T_6. Subintervals T_1 and T_3 have equal duration, therefore the corresponding total charge is:

$$\Delta Q_{tot} = \hat{I}_{DBS}\, T_1 = \frac{(V_{DC}\, UOVL)^2}{R_{dbs}\, dv/dt} \tag{3.34}$$

Where,

- ΔQ_{tot}: charge variation in the cell capacitors (C)
- $\hat{I}_{DBS}$: peak DBS current (A)

T_1 is taken from Appendix A, equation (A.1). Assuming that on average, due to the balancing algorithm, one cell capacitor is inserted in the circuit for around 50% of the charging time during the ramping up/down periods, then:

$$C_{cell} = \frac{\Delta Q_{tot}}{2}\, \frac{1}{\Delta V_C} \tag{3.35}$$

And replacing the charge expression from (3.34) and the peak to peak ripple expressed in volts (ΔV_C) by the equivalent value in per unit ($\Delta V_{C,pu}$), the final expression for the required cell capacitance is:

$$C_{cell} = \frac{V_{DCn}\, UOVL\, N}{2\, R_{dbs}\, dv/dt\, \Delta V_{C,pu}} \tag{3.36}$$

3.5 The full-bridge multilevel DBS circuit with lumped resistive element

The last circuit to be studied is the full-bridge multilevel DBS proposed in [76]. It has an identical structure to the half-bridge multilevel DBS, with the difference that the half-bridge cells are replaced by full-bridge cells, as observed in Fig. 3.26.

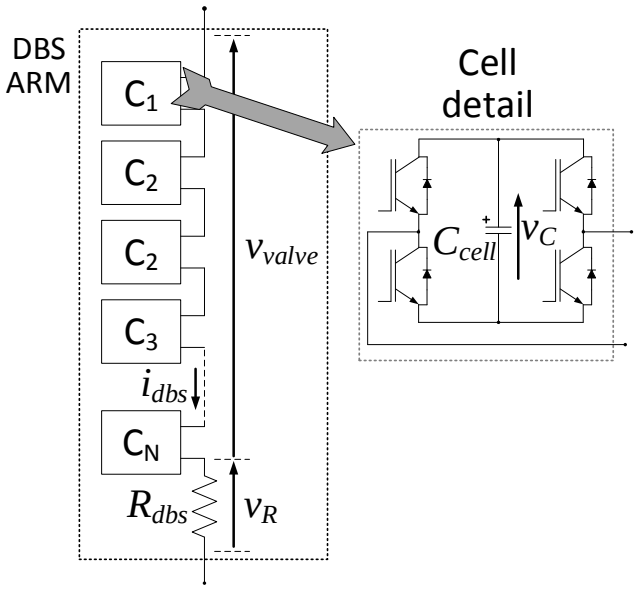


Fig. 3.26 Basic structure of the full-bridge multilevel DBS circuit.

The full-bridge cells can generate three different voltage levels at its output terminals. As displayed in Fig. 3.27, v_{cell} can be of positive or negative polarity ($\pm v_C$) or zero. This allows for the DBS valve to generate a voltage of either polarity, providing a mechanism to maintain the energy balance according to (3.16) without having to reverse the i_{dbs} current polarity, as was the case with the half-bridge multilevel DBS.

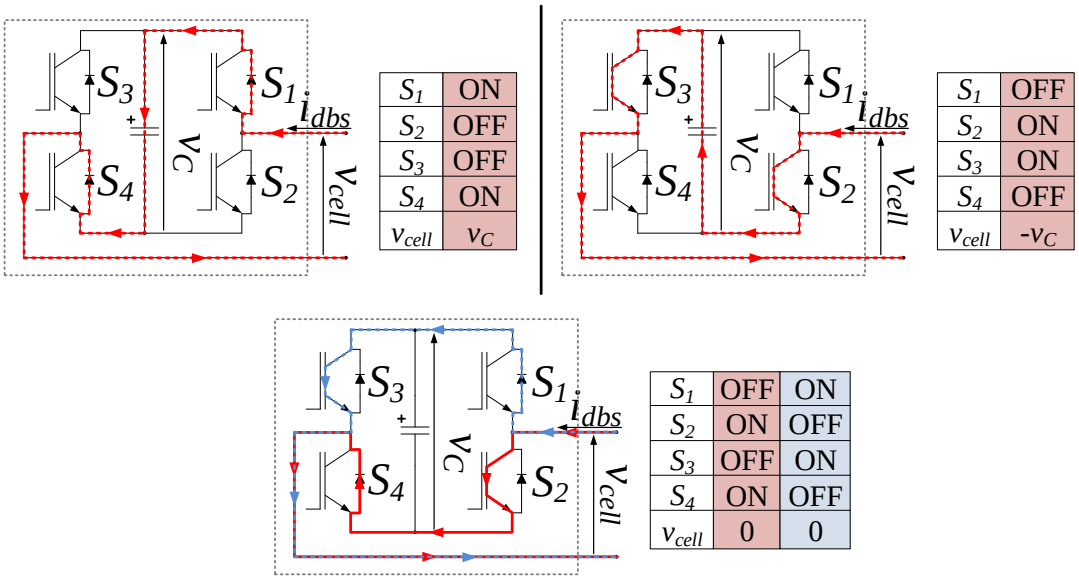


Fig. 3.27 Possible commutation states of the full-bridge cells.

This capability also makes this topology the only one whose application in classical HVDC, with thyristor based current source converters (CSC), is

straightforward. In CSC based schemes, the DC current always flows in the same direction, and a power reversal is achieved by reversing the DC voltage polarity, as shown in Fig. 3.28. By reversing the output voltage polarity of each individual cell, the full-bridge multilevel DBS can adapt itself to the change in the HVDC system voltage polarity. This however is not possible with the previous three circuits, and the only possibility would be the use of an external mechanical switch arrangement, as suggested in [90] and shown in Fig. 3.29. By operating pairs SW1-SW3 and SW2-SW4 in a complementary manner, for example SW1 and SW2 open and SW3 and SW4 closed, the voltage polarity on the DBS arm can be kept constant while the HVDC voltage polarity changes. However, each of these switches needs to be rated to withstand full HVDC voltage and therefore it is a costly and bulky alternative.

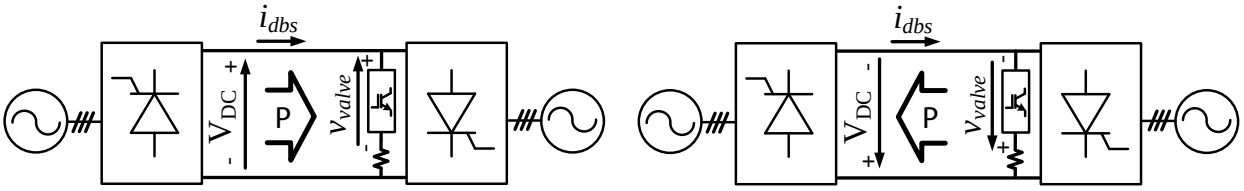


Fig. 3.28 Full-bridge multilevel DBS in classical HVDC scheme during power reversal.

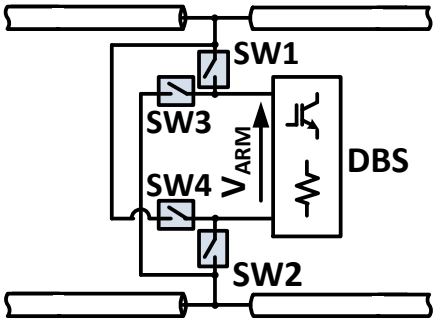


Fig. 3.29 Mechanical switches arrangement to reverse arm voltage polarity in DBS circuits.

3.5.1 Trapezoidal power modulation with the full-bridge multilevel DBS

Due to the similarity with the half-bridge multilevel DBS, the modulation strategy is almost identical, apart from the already mentioned detail of reversing the valve voltage polarity instead of the DBS current polarity to achieve the energy balance.

The proposed trapezoidal voltage pulse to be used with the full-bridge multilevel DBS is displayed in Fig. 3.30. The difference with the half-bridge

case (Fig. 3.18) occurs during subintervals T_3, T_4 and T_5, with the voltage pulse going negative with an amplitude $-V_A$. In this case the valve voltage never goes above V_{DC} since there is no need to reverse the DBS current polarity.

Fig. 3.31 illustrates the operation of the circuit and the internal energy variation over one modulation period using the proposed trapezoidal waveform. In this case, the valve generates positive power during subintervals T_1 and T_6 which are compensated by the negative power generated during subintervals T_3, T_4 and T_5 thanks to the reversal of the valve voltage polarity in order to achieve the valve energy balance. AS for the half-bridge circuit, since the valve voltage during subinterval T_2 is zero, the valve energy remains constant. The resulting braking resistor voltage (v_R), instantaneous power (p_R) and average power ($\bar{P}_R$) dissipation are also displayed in the figure.

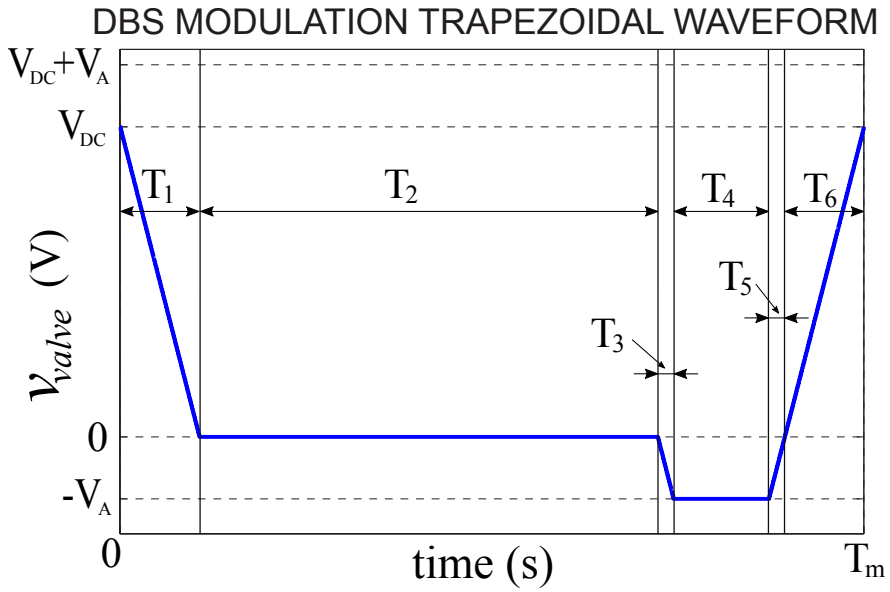


Fig. 3.30 Trapezoidal pulse for the full-bridge multilevel DBS modulation.

Power modulation strategy

The modulation strategy to dynamically vary the level of power dissipation in the braking resistor with the full-bridge circuit is very similar to that of the half-bridge circuit. Two different modulation regions are also used in this case, and in the first region, the same *"time modulation"* principle is employed. The duration of T_2 subinterval is progressively reduced from it maximum value (T_{2max}) in order to reduce the average power dissipation as presented in Fig. 3.32. When the duration of T_2 is reduced to zero, the crossover point is reached and a change in strategy is needed.

As opposed to the half-bridge case, *"amplitude modulation"* is not an option to further reduce the power dissipation since the negative part of the voltage pulse generated by the valve is used to discharge the excess of energy and therefore, by

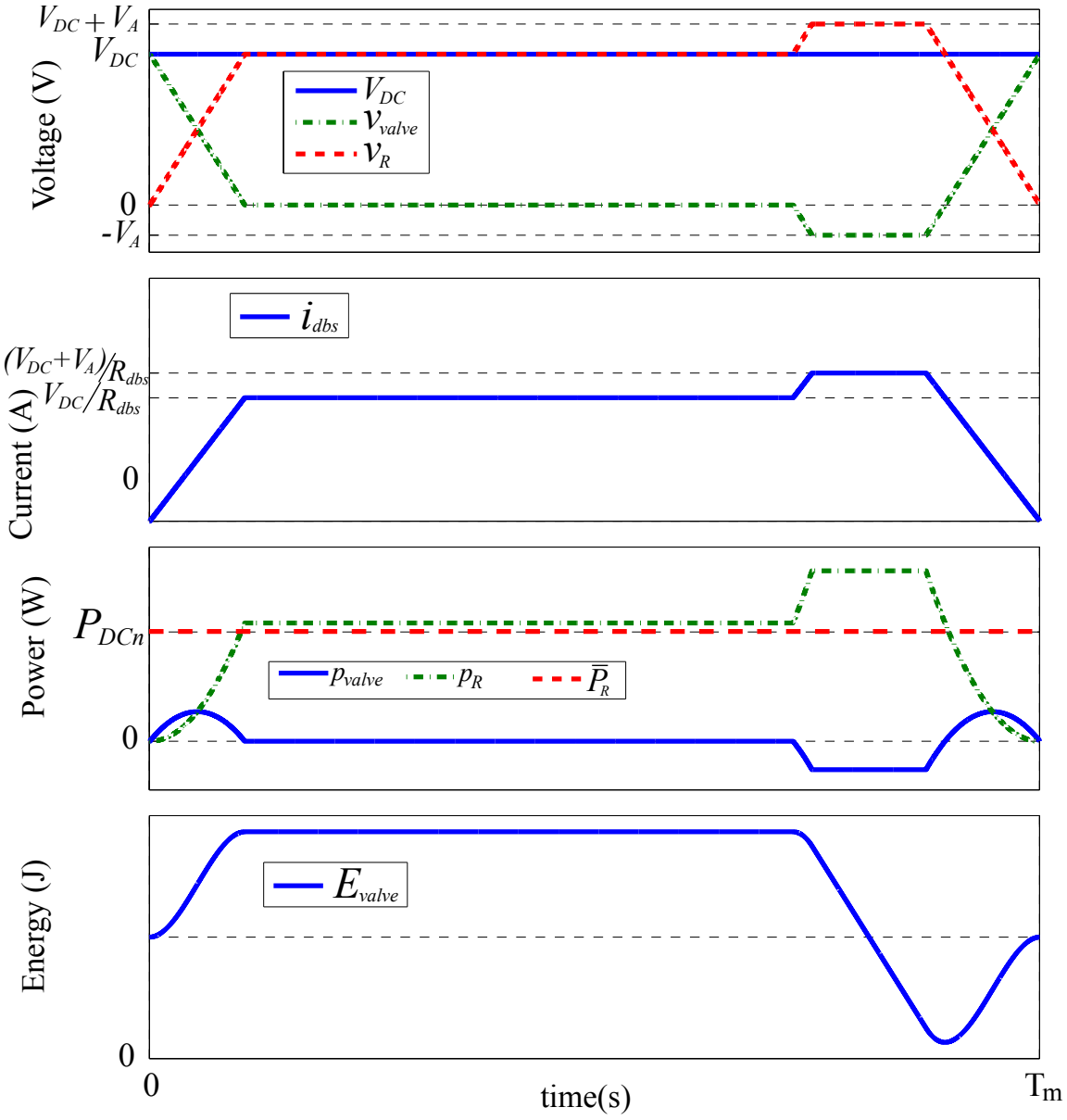


Fig. 3.31 Detail of the DBS arm waveforms over one modulation period with the full-bridge multilevel DBS.

eliminating it, the energy balance would become impossible. A second *"time modulation"* region is therefore used with this circuit, where the duration of subinterval T_4 is progressively reduced from its maximum value (T_{4max}) down to zero as illustrated in Fig. 3.32. This reduction of T_4 does however have an impact on the energy balance of the valve, and in order to maintain the balance the duration of intervals T_1 and T_6 also needs to be reduced. The result is that during this second modulation region, the valve is forced to operate at variable dv/dt.

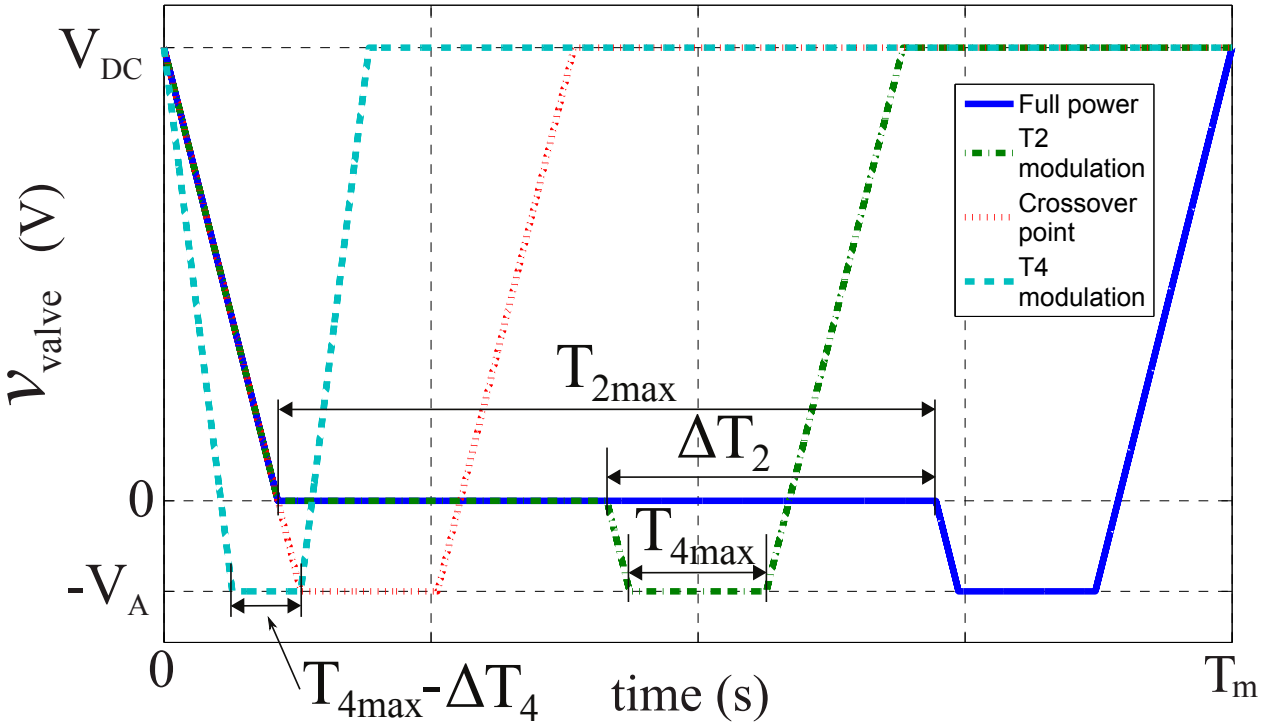


Fig. 3.32 Valve trapezoidal voltage for different operation regions of the modulation strategy.

The equations needed to characterize this new modulation strategy during the different modulation subintervals have been derived in section A.3 of Appendix A. These are used to study the energy balance in the DBS valve which is presented next.

DBS valve energy balance and required braking resistor value

The energy balance in the valve can be expressed as a function of the valve energy variation during the different subintervals as:

$$\Delta E_{valveT1} + \Delta E_{valveT2} + \Delta E_{valveT3} + \Delta E_{valveT4} + \Delta E_{valveT5} + \Delta E_{valveT6} = 0 \Longrightarrow$$
$$\Longrightarrow 2\,\Delta E_{valveT1} + 2\,\Delta E_{valveT3} + \Delta E_{valveT4} = 0 \tag{3.37}$$

Replacing with values (A.43), (A.51) and (A.56) from Appendix A, and solving the equation, the required duration of T_4 to ensure the valve energy balance during the first time modulation region, for a given value of V_A and dv/dt is:

$$T_{4\,max} = \frac{{V_{DC}}^2 - V_{DC}\,V_A - 2\,{V_A}^2}{3\,V_A\,dv/dt} \tag{3.38}$$

Given a certain modulation period T_m, the maximum duration of subinterval T_2 (T_{2max} in Fig. 3.32) can also be determined. By replacing the values of T_1, T_3 and T_4 from (A.39), (A.47) and (3.38) respectively, T_{2max} is expressed as:

$$\begin{aligned} T_{2\,max} &= T_m - T_1 - T_3 - T_4 - T_5 - T_6 = T_m - 2\,T_1 - 2\,T_3 - T_4 = \\ &= T_m - \frac{{V_{DC}}^2 - V_{DC}\,V_A - 2\,{V_A}^2}{3\,V_A\,dv/dt} - \frac{2\,V_A}{dv/dt} - \frac{2\,V_{DC}}{dv/dt} \end{aligned} \tag{3.39}$$

By using the expressions of the energy in the braking resistor for the different subintervals derived in Appendix A, the average power dissipation in the braking resistor over one modulation period ($\bar{P}_R$ in Fig. 3.31) is calculated:

$$\begin{aligned} \bar{P}_R &= \frac{1}{T_m}\left(E_{RT1} + E_{RT2} + E_{RT3} + E_{RT4} + E_{RT5} + E_{RT6}\right) = \\ &= \frac{1}{T_m}\left(2E_{RT1} + E_{RT2} + 2E_{RT3} + E_{RT4}\right) \end{aligned} \tag{3.40}$$

Replacing by(A.44), (A.46), (A.52) and (A.57) from appendix A:

$$\begin{aligned} \bar{P}_R = &\frac{\left(3\,{V_A}^2 + 6\,V_{DC}\,V_A + 3\,{V_{DC}}^2\right)\,dv/dt\,T_4 + 3\,{V_{DC}}^2\,dv/dt\,T_2}{3\,R_{dbs}\,T_m\,dv/dt} + \\ &+ \frac{2\,{V_A}^3 + 6\,V_{DC}\,{V_A}^2 + 6\,{V_{DC}}^2\,V_A + 2\,{V_{DC}}^3}{3\,R_{dbs}\,T_m\,dv/dt} \end{aligned} \tag{3.41}$$

And substituting T_4 and T_2 from (3.38) and (3.39), the expression for the maximum average power dissipation in the braking resistor is:

$$\bar{P}_{R_{max}} = \frac{3\,T_m\,{V_{DC}}^2\,dv/dt + V_{DC}\,{V_A}^2 - {V_{DC}}^2\,V_A - 2\,{V_{DC}}^3}{3\,R_{dbs}\,T_m\,dv/dt} \tag{3.42}$$

By solving for R_{dbs} and replacing $\bar{P}_{R_{max}}$ by the nominal HVDC link power (P_{DCn}), the required value of the braking resistor is:

$$R_{dbs} = \frac{V_{DC}\,\left(3\,T_m\,V_{DC}\,dv/dt + {V_A}^2 - V_{DC}\,V_A - 2\,{V_{DC}}^2\right)}{3\,P_{DCn}\,T_m\,dv/dt} \tag{3.43}$$

When operating within the first time modulation, the value of T_4 is kept constant at T_{4max} while T_2 is progressively reduced from T_{2max} down to zero.

With the value of the braking resistor already fixed, replacing 3.38 in 3.41 and solving for T_2:

$$T_2 = \frac{3\,P_R\,R_{dbs}\,T_m\,V_A\,dv/dt - V_{DC}\,{V_A}^3 - 3\,{V_{DC}}^2\,{V_A}^2 - 3\,{V_{DC}}^3\,V_A - {V_{DC}}^4}{3\,{V_{DC}}^2\,V_A\,dv/dt} \quad (3.44)$$

Which can be used to determine the required duration of T_2 to dissipate the desired amount of power over one modulation period.

When T_2 is reduced to zero, the *crossover point* is reached, and the second *"time modulation"* region is entered in order to further reduce the power dissipation. In this region, the duration of T_4 is progressively reduced while V_A is kept constant, as illustrated in Fig. 3.32. As mentioned, in order to maintain the valve energy balance, the duration of subintervals T_1 and T_6 also needs to be reduced, which effectively increases the value of dv/dt according to the following expression:

$$dv/dt = \frac{{V_{DC}}^2 - V_{DC}\,V_A - 2\,{V_A}^2}{3\,V_A\,T_4} \quad (3.45)$$

As the duration of T_4 reduces the value of dv/dt increases. When T_4 approaches zero, dv/dt approaches infinity. The result is that for very low power dissipation levels the DBS valve voltage becomes quasi-square pulses and all the cells need to be switched off simultaneously. The solution to this problem would be to impose a limit to the maxim permitted value of dv/dt which would limit the circuit from entering this very low power dissipation region.

3.5.2 Controller implementation

Fig. 3.33 shows the block diagram of the developed controller. Due to the similarities in the operation with the half-bridge multilevel circuit, the controller is almost identical to the one shown in Fig. 3.21, and the differences are on the implementation of some of the functions represented in the blocks, as explained in this section.

DC voltage regulator

The implementation of the proportional (P) controller remains identical, with the output being the average power dissipation demand in per unit, to be passed to the trapezoidal voltage generation block. Therefore, the gain for the proportional controller is the same as presented in (3.31).

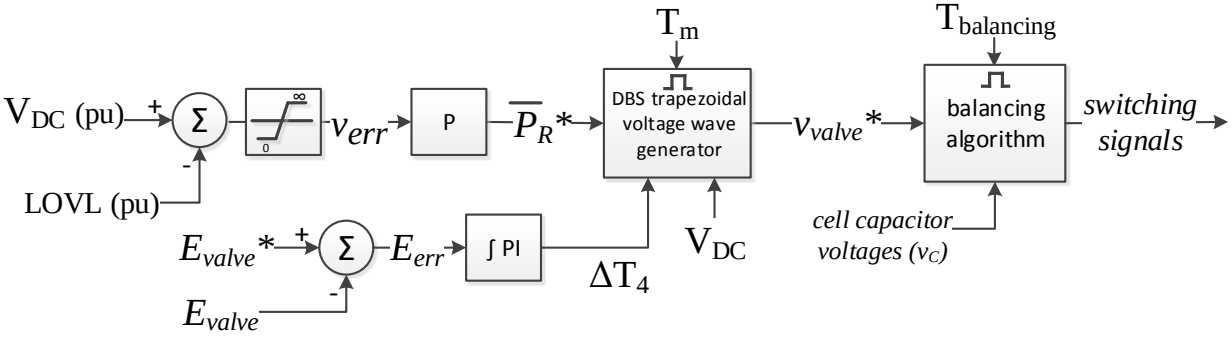


Fig. 3.33 Block diagram of the full-bridge multilevel DBS proposed controller.

Valve stored energy regulator

The controller also includes the same proportional-integral (PI) action to compensate for deviations in the total amount of stored energy in the DBS capacitance. Both the reference and the feedback signal are calculated according to (3.33) and (3.32). The output of the PI action in this case is an offset to be applied by the trapezoidal generator to the duration of T_4 subinterval, since it directly affects the cell energy balance, as explained earlier in this section.

Trapezoidal voltage generator

This block implements the generation of the voltage pulses for the modulation strategy represented in Fig. 3.32. As mentioned, the strategy consist on two different time modulation regions, where by modifying the duration of subintervals T_2 and T_4 in the trapezoidal voltage pulse the average power dissipation in the braking resistor can be regulated. The inputs to the function are the average power dissipation demand ($P_R{}^*$), the measured DC voltage value and the offset value coming from the valve energy regulator.

Fig. 3.34 shows the flow diagram for the trapezoidal generation function, with two different paths for each of the two modulation regions. When operating in the first time modulation region, T_2 is first calculated based on the power dissipation demand using (3.44). Then subinterval T_1/T_6 and T_3/T_5 durations are calculated using (A.39) and (A.47) from appendix A and using the constant dv/dt specified as a design parameter. The duration of time subinterval T_4 is calculated according to (3.38) in order to ensure the cell energy balance. The offset value from the valve energy regulator ΔT_4 is then applied to the computed value for T_4.

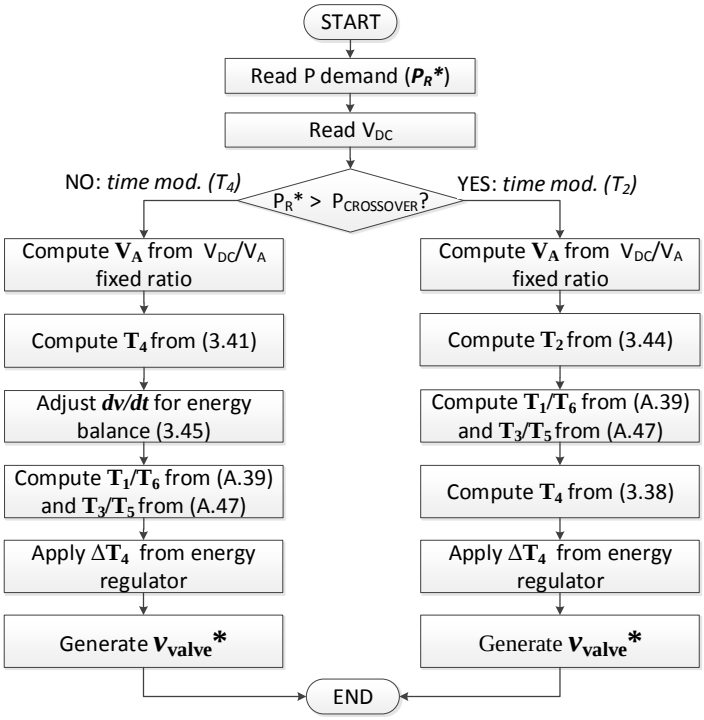


Fig. 3.34 Flow diagram for the trapezoidal generation function.

In the second time modulation region, the required value of T_4 is calculated from (3.41). Then the required value of the dv/dt to maintain the cell energy balance is calculated with (3.45). After, the values of T_1/T_6 and T_3/T_5 can be determined using expressions (A.39) and (A.47) from appendix A. The offset value coming from the valve energy regulator ΔT_4 is applied to the calculated duration of T_4, and the output trapezoidal voltage pulse demand is generated.

Fig. 3.35 shows the internal control signals to illustrate the evolution of the trapezoidal arm voltage demand when the average power dissipation demand varies from 0 to 1 pu.

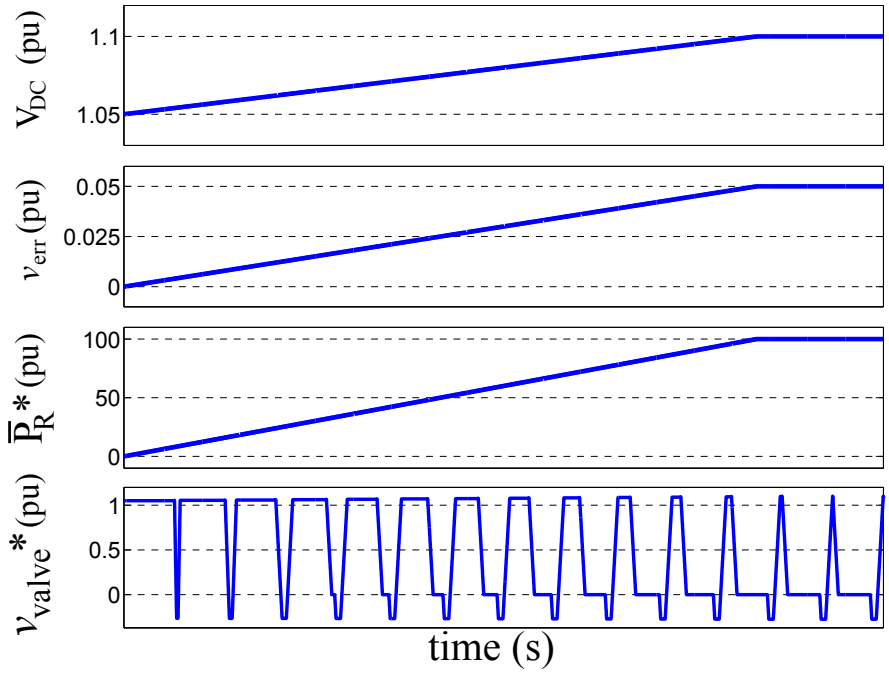


Fig. 3.35 Internal controller signals for the full-bridge multilevel circuit.

Balancing algorithm

Fig. 3.36 shows the flow diagram of the balancing algorithm for the full-bridge circuit. The main difference with respect to the half-bridge circuit is the lack of DBS current feedback. Since the modulation strategy in this case does not reverse the current polarity through the DBS arm, it does not need to be accounted for when deciding the commutation state of each cell. When the valve voltage to be generated is positive, the cell voltage to be generated is also positive and the cell capacitors inserted in the current path will charge. Therefore, cells with the lower capacitor voltage are inserted first and the internal switches are commutated according to Fig. 3.27 to generate the positive cell output voltage, until the valve voltage matches the value in the demand signal. When the valve voltage to be generated is negative, the cell capacitors in the current path will discharge. Hence, cells with the higher capacitor voltages are inserted first and the internal switches commutated to generate the required cell output negative voltage.

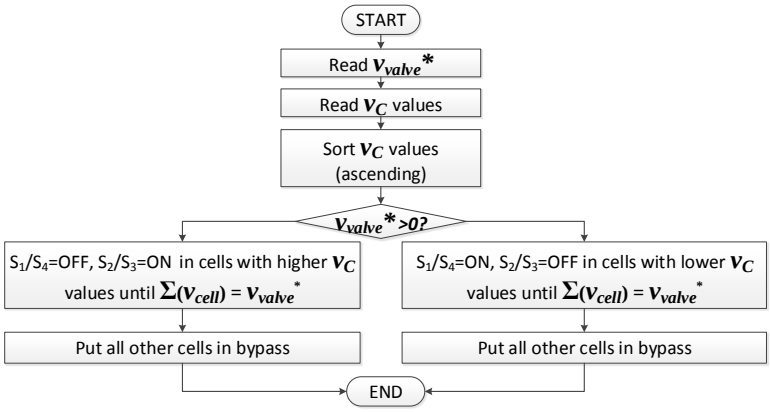


Fig. 3.36 Flow diagram for balancing algorithm in full-bridge multilevel DBS.

3.5.3 Cell capacitor sizing

The detail of the relevant waveforms to derive the expression of the cell capacitance is shown in Fig. 3.37, for the operation of the DBS circuit during full power dissipation. In this case the capacitors charge during subintervals T_1 and T_6, and discharge during subintervals T_3, T_4 and T_5 (Fig. 3.30). Expression (3.34) and (3.35) are also valid for the full-bridge circuit, and therefore the required cell capacitance value in this case is also calculated by using (3.36).

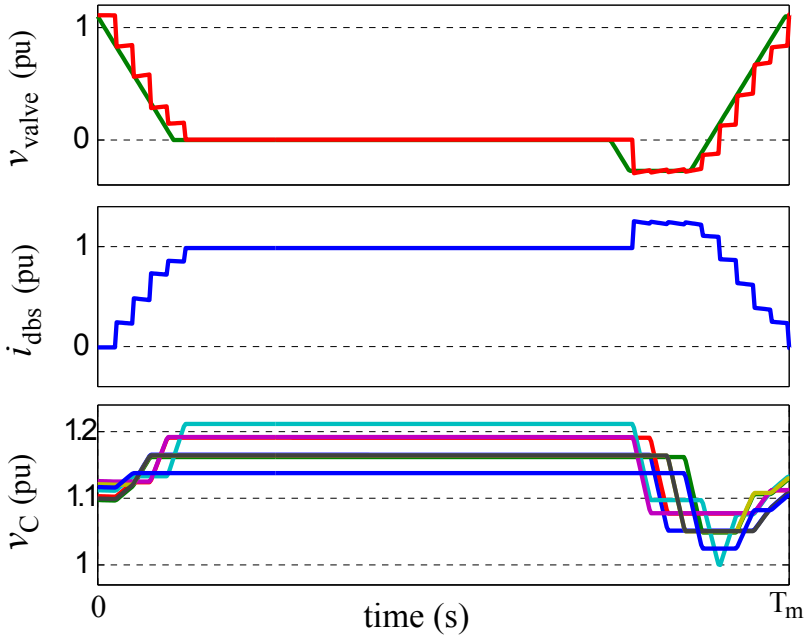
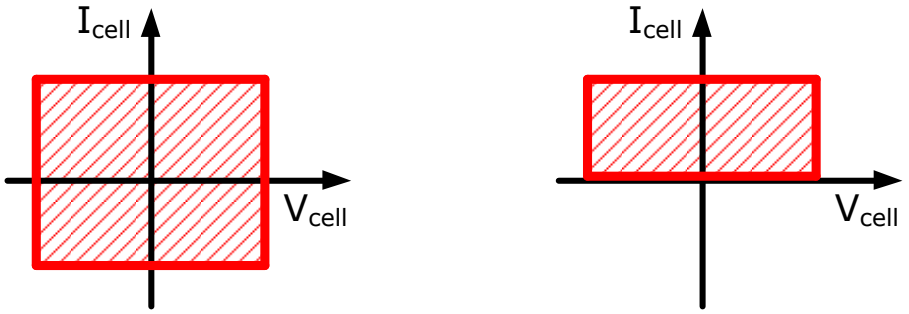


Fig. 3.37 Capacitor balancing signals detail in the full-bridge multilevel circuit.

3.5.4 Alternative cell configuration: the sparse bridge

At the beginning of this section, the capability of the full-bridge multilevel chopper to operate in a conventional HVDC scheme, with CSC converters, was explained. This is possible thanks to the ability of the full-bridge cell to operate

in four quadrants, with any combination of cell voltage and current of either polarity, as shown in Fig. 3.38a. However, when connected to a VSC-HVDC scheme, the HVDC voltage polarity is constant, and therefore, with the type of modulation proposed in this section, the polarity of the current through the DBS arm remains constant whereas the cell voltage polarity has to be inverted during certain operation subintervals. Therefore a two quadrants operation, as shown in Fig. 3.38b, is sufficient.



(a) Four quadrants operation. (b) Two quadrants operation.

Fig. 3.38 Different cell operation characteristic.

A sparge bridge cell (named in this way in [76]) is displayed in Fig. 3.39. In this cell two complimentary IGBTs have been replaced by diodes while keeping a full bridge configuration.

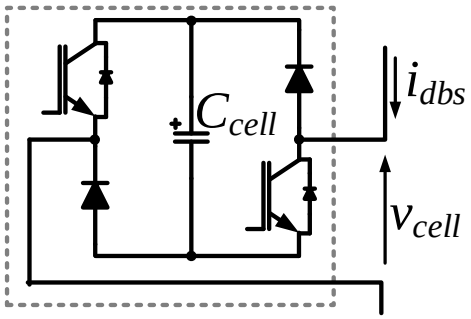


Fig. 3.39 Sparse bridge cell.

The result is that the current can only flow through the cell with the positive polarity as shown in the figure, but it still can generate three different voltage levels v_{cell} $(0, +v_C, -v_C)$ according to the commutation state of both IGBTs. This makes the sparge bridge suitable for operation in the two quadrant mode of the full-bridge DBS valve, as shown in Fig. 3.38b. By replacing the full bridge cells by sparse bridge cells, the total IGBT count and gate drive electronics is halved

in the converter. The only disadvantage as already mentioned, is the inability of the DBS using sparse bridge cells to operate in LCC based HVDC schemes. The operation of the DBS remains otherwise identical, and all the concepts presented in this section for the control of the converter are valid for the modified version.

3.6 Design parameters selection for the half-bridge and full-bridge multilevel circuits

The trapezoidal waveforms proposed to modulate the power dissipation have a number of parameters whose value needs to be set during the system design stage. Each of those parameters affects not only the system performance but also the quantity and physical characteristics of certain components in the DBS converter, and therefore, they also have an impact on the cost/size of the converters. The selection of the optimal value for one design parameter is often detrimental for the system performance or for achieving the optimal value in another parameter, and therefore some trade-offs are necessary.

The parameters that need to be considered for a detailed study are:

- Voltage derivative during trapezoidal ramps generation: dv/dt.
- Amplitude of trapezoidal voltage: V_A.
- Period of trapezoidal modulating signal: T_m.

DBS valve voltage derivative: *dv/dt*

One of the main advantages with both multilevel circuits is their capability to produce valve voltage pulses, which result from the aggregation of individual cell voltages, with a controlled dv/dt. The use of square pulses, like the ones generated by the HVDC chopper circuit, together with the resulting high di/dt currents, put a high level of stress in certain components, such as inductors, capacitors or valve semiconductors. Furthermore, radiated EMI can be high and additional shielding of the converter stations becomes necessary. In this respect, it would be desirable to reduce the dv/dt value as much as possible. However, the instantaneous power dissipation in the braking resistor (p_R) is lower during the ramping-up and ramping-down subintervals as observed in Fig. 3.19. In order to achieve the desired average power dissipation ($\bar{P}_R$), the instantaneous power p_R needs to have a peak value larger than the average power. This produces higher currents in the DBS arm and increased current rating for the cell semiconductors when compared to the case where square voltage pulses are used. The energy accumulation in

the cell capacitance also takes place exclusively during these voltage ramping subintervals. Therefore in order to maximise the average power dissipation and minimize the energy accumulated in the cell capacitors during the voltage ramping subintervals, a high dv/dt value is more attractive. From a control system perspective, the generation of voltage ramps with high derivatives and good accuracy, requires short balancing periods which might be challenging for the control hardware. The use of a fixed value of dv/dt makes the implementation of the modulation strategy simpler, and therefore it is the approach chosen in this work.

Voltage amplitude: V_A

In order to rebalance the energy stored in the DBS capacitance, subintervals of negative voltage or above the HVDC system voltage are used. In the two different trapezoidal pulses presented (Figs. 3.18 and 3.30), the voltage amplitude during these rebalancing subintervals is defined by parameter V_A. Its value determines the magnitude of the instantaneous negative arm power, and therefore a higher value of V_A allows to re-balance the cell energy faster, or for the same subinterval duration, to remove more energy from the cells. A direct relation exists then between the value of dv/dt and V_A. A reduced dv/dt implies that larger values of V_A are required to rebalance the energy.

For the half-bridge circuit, parameter V_A defines the amount of additional voltage the DBS arm needs to generate above the HVDC system voltage. The greater the value of V_A, the greater the average cell voltage needs to be or the larger the number of arm cells required. Considering converter components are normally utilized close to their maximum safe operation ratings for economical reasons, the latter option is the most likely one. Larger values of V_A do not have any impact on the required number of cells for the full-bridge circuit. They do however increase the DBS peak current and therefore the current rating for the circuit components.

Trapezoidal modulation period: T_m

T_m determines the duration of the modulation period and is always kept constant during the DBS operation. As presented, the parameters that define the trapezoidal voltage pulses (subinterval durations and voltage amplitudes) are continuously recalculated at the beginning of a new modulation period to ensure the valve energy balance. This also implies that the average power dissipation in the braking resistor can only be adjusted at the beginning of each modulation period. Therefore T_m heavily influences the DBS circuit dynamic response to adapt the power dissipation level when fast changes in the DC voltage occur.

Fig. 3.40 illustrates the influence of using different modulation periods with an example of a DC over-voltage situation starting at time zero. Both the DC voltage evolution and the average power dissipation are displayed. The DBS dynamic response to increase the power dissipation as a reaction to the DC over-voltage is slower for larger values of T_m.

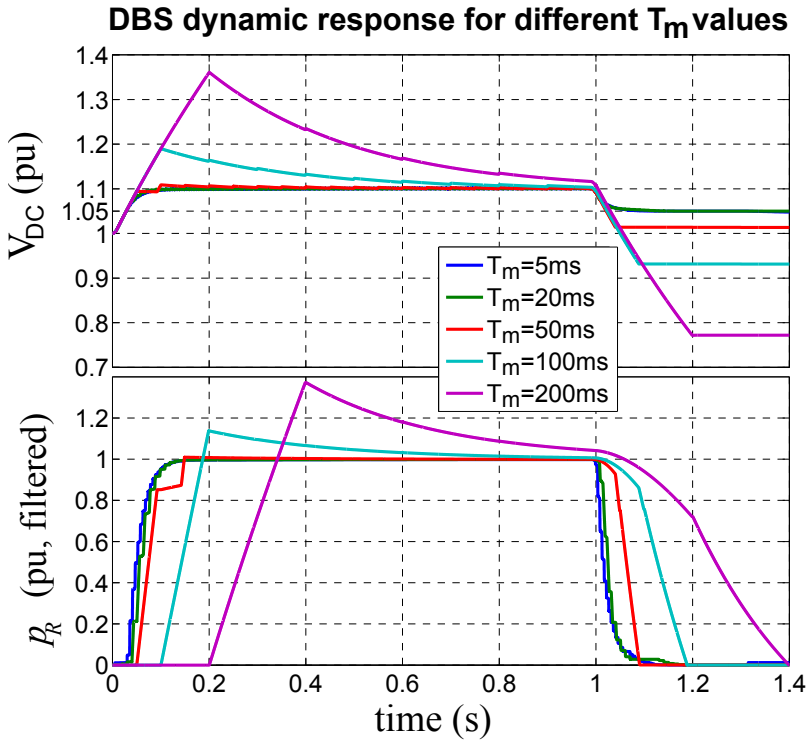


Fig. 3.40 DBS dynamic response for different values of modulation period T_m.

The required DBS power dissipation dynamic response for a particular project is influenced by the HVDC system characteristics, mainly the nominal DC voltage, nominal power and DC system capacitance. Therefore the acceptable maximum value of T_m is expressed based on the time it takes for the DC link voltage to reach the UOVL when the onshore VSC station cannot extract any power from the DC link. This can be expressed as:

$$T_{m_{max}} = \frac{C_{DC}\, {V_{DCn}}^2\, (UOVL^2 - 1)}{2\, P_{DCn}} \tag{3.46}$$

In the example of Fig. 3.40, UOVL is 1.1 pu, V_{DCn} is 8 kV, P_{DCn} is 11.2 MW and C_{DC} is 80 mF. Replacing in (3.46) gives a maximum T_m of 48 ms. It can be observed in the figure that for values of T_m greater than this limit, the HVDC voltage presents an overshoot at start-up, exceeding the desired UOVL.

The duration of the different subintervals in one modulation period ($T_1..T_6$) is defined by the values of dv/dt and V_A and therefore, implicitly, those two parameters also limit the minimum possible duration of T_m. Larger dv/dt and V_A result in shorter duration of subintervals $T_1..T_6$, hence for a shorter T_m. Since

high dv/dt and V_A values also put more stress in some converter components, a compromise for choosing the value of each of the three parameters is needed.

3.6.1 Trade-offs analysis

The current amplitude is a key parameter in the design of the DBS, since it defines the current rating for the different circuit components. The trade-offs analysis for the half-bridge and full-bridge multilevel circuits is therefore performed taking into account the peak current in the DBS during the circuit operation. For this analysis, Dolwin3 project ratings (320kV and 450MW per DBS valve) are used in the calculations. Mitsubishi's CM1500HG-66R 3.3-kV 1.5-kA HVIGBT module is used as the reference cell semiconductor. The SOA in this device defines a maximum 3 kA collector current and therefore a maximum of 2 kA peak DBS current is considered.

The relation between V_A, dv/dt and T_m is studied for both half-bridge and full-bridge circuits using expressions (3.23) and (3.43) in order to keep the valve energy balance for a desired level of power dissipation. To simplify the analysis, only four values of peak DBS current (1.4, 1.6, 1.8 and 2 kA) and six different values of voltage V_A (16, 32, 48, 64, 80 and 96 kV) are considered. From the peak current value, the value of R_{dbs} can be calculated and replaced in both (3.23) and (3.43). The value of voltage V_A is directly replaced in the equations, as well as the V_{DC} and P_{DCn} values from Dolwin 3 example. Then T_m as a function of dv/dt can be plotted and the results are displayed in Fig. 3.41 for the half-bridge circuit and Fig. 3.42 for the full-bridge circuit. In both cases, an increase in dv/dt reduces the required minimum modulation period duration, which as previously analysed, improves the DBS dynamics response against DC voltage variations. An increase in the peak DBS current also allows for shorter modulation periods. When considering the value of voltage V_A, the effect is different in both circuits. In the half-bridge circuit the required modulation period reduces as V_A increases, as less time will be needed to rebalance the valve energy during subinterval T_5 (Fig. 3.19). However for the full bridge case, an increase in the value of V_A has the opposite effect. This is because as V_A increases so does the peak DBS current (Fig. 3.31). Therefore increasing V_A for a fixed value of DBS peak current requires a larger R_{dbs} to be used. This decreases the DBS average current over the modulation period and therefore a longer modulation period is needed to achieve the same average power dissipation.

Comparing the results for both circuits it is observed that the full-bridge circuit needs shorter modulation periods for the same operating conditions. This is due to the presence of the current polarity reversal subinterval during the half-bridge circuit operation. Comparing the DBS current waveforms from Figs. 3.19 and 3.31 it is observed that this subinterval causes a reduction in the DBS

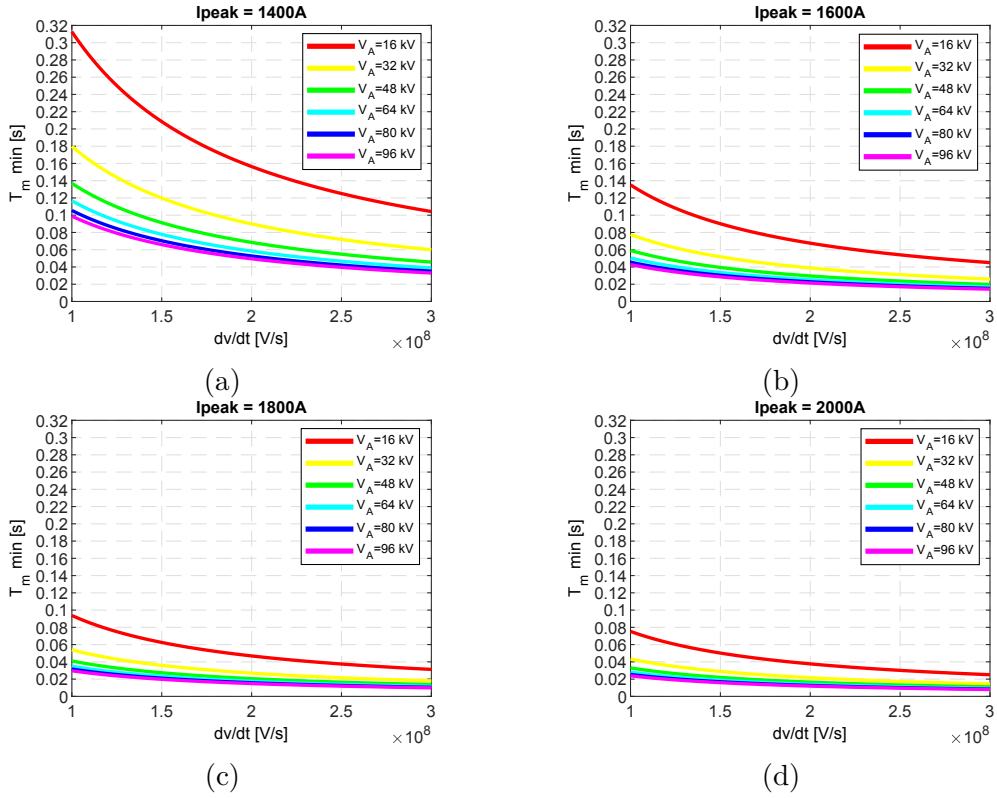


Fig. 3.41 Minimum modulation period (T_m) as a function of dv/dt and V_A for different values of DBS peak current in the half-bridge multilevel DBS.

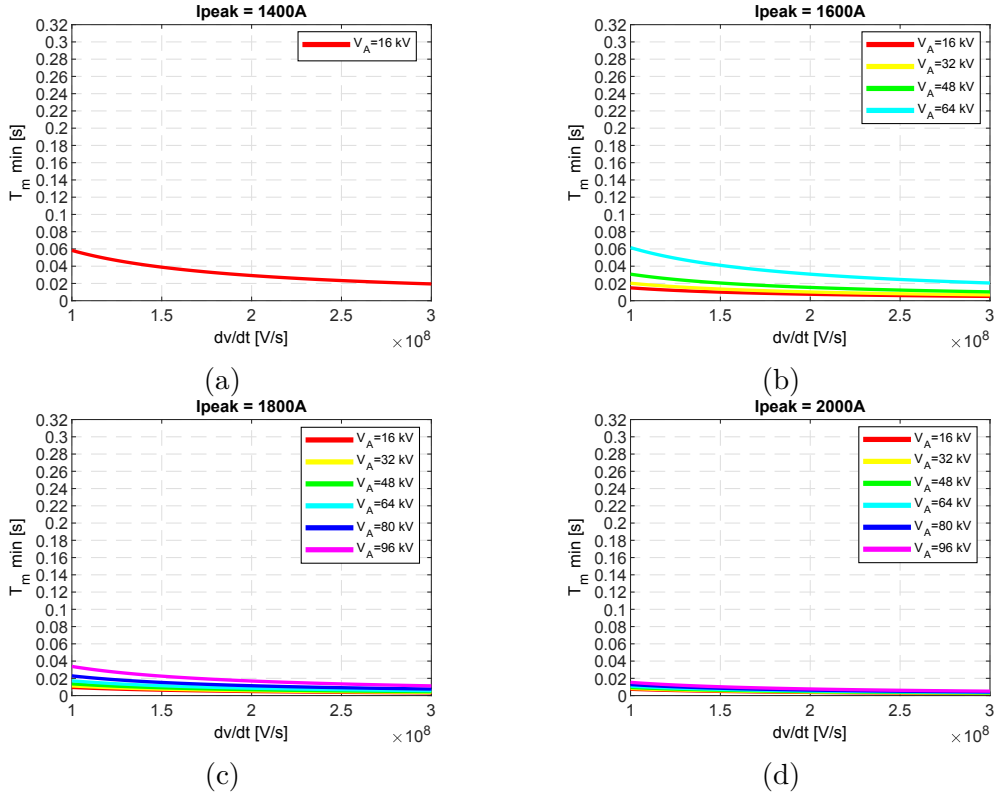


Fig. 3.42 Minimum modulation period (T_m) as a function of dv/dt and V_A for different values of DBS peak current in the full-bridge multilevel DBS.

average current which explains the need for longer modulation periods to achieve the same average power dissipation.

3.7 Economical considerations

While most research works acknowledge the superior operational performance and safety offered by the DBS solution with respect to alternative techniques, its cost and size is generally identified as the main drawback. The basic components of the DBS are the semiconductor switches and the braking resistors. In the case of the multilevel topologies, the cell capacitor also needs to be considered.

3.7.1 Braking resistor

Fig. 3.43 shows the lumped braking resistors for the BorWin 1 project (400MW, 300kV) [91]. Resistors need to be dimensioned to dissipate HVDC link rated power for the maximum possible duration of a fault event, as specified by grid codes. These two parameters define the energy rating of the required resistor. As presented in [81], the thermal mass of the resistor needs to be sufficient to stay below the maximum temperature when absorbing the resulting energy. Transmission system operators can impose more strict requirements. In the Dolwin 3 project for instance, the braking resistor is to be dimensioned to dissipate the HVDC rated power for 2 seconds. The resistor needs to cool down before a new fault-ride through event can take place. In the event of multiple faults occurring sequentially with short cooling periods, the braking resistor needs to be monitored to avoid exceeding the maximum operating temperature.

Fig. 3.43 Lumped braking resistors for Borwin 1 project (Source: ABB, [91], 2014).

Example

Using Dolwin 3 rated power of 900 MW for 2 seconds results in an energy absorption by the braking resistors of 1.8 GJ. Assuming the use of two DBS

Table 3.2 Characteristics of braking resistors for the different DBS circuits.

	HVDC Chopper	Multilevel Chopper
# of R per arm	1	196
Value of R [Ω]	275	1.4
E rating [MJ]	900	4.6
V rating [kV]	352	1.8
	Half-Bridge Multilevel	Full-Bridge Multilevel
# of R per arm	1	1
Value of R [Ω]	164	247
E rating [MJ]	900	900
V rating [kV]	352	422

arms results in two braking resistors with an energy rating of 900 MJ each. This is the case for the HVDC chopper DBS and both the half and full-bridge multilevel DBS, where lumped resistance is used. As observed in Fig. 3.43, due to the high required energy rating, the arm resistor can be divided into several series connected resistive elements. In the case of multilevel chopper circuit, with its distributed resistance, and considering a DBS arm integrated by 196 cells (1.8 kV average cell voltage), 392 braking resistors are needed with an individual energy rating of 4.6 MJ each. Table 3.2 shows the resulting braking resistor characteristics. The calculations are performed considering the UOVL from Table 3.1. For the half and full-bridge multilevel circuits the following assumptions are made: T_m: 10 ms, dv/dt: 250 MV/s and V_A: 0.2*V_{DC}.

3.7.2 Semiconductor switches

A significant difference between the alternative DBS circuits lies in the number of semiconductors. They have to be rated to support full DBS current and in the case of the IGBTs there are associated gate drives which also increase the system cost.

Example

Table 3.3 shows the results of the semiconductor requirements for the four different DBS circuits, expressed as installed power in one DBS valve for both IGBTs and diodes. As with the braking resistor comparison, Dolwin 3 project ratings are used and the same T_m and dv/dt parameters are used for the half-bridge and full-bridge circuits. Two different V_A values are used in the case of the half-bridge multilevel circuit and for the full-bridge multilevel circuit, the sparse-bridge option is also considered. The same 3.3kV IGBT, operating at 1.8 kV nominal voltage is considered for the 3 circuits to perform a fair comparison.

Table 3.3 Comparison of semiconductor requirements in the four DBS circuits.

	HVDC Chopper		Multilevel Chopper	
# of levels/cells	392		392	
Total IGBT VA rating	1.65 GVA		1.65 GVA	
Total diode VA rating	1.65 GVA		4.96 GVA	
	Half-Bridge Multilevel		Full-Bridge Multilevel	
			full-bridge	sparse-bridge
V_A	0.2*V_{DC}	0.4*V_{DC}	0.2*V_{DC}	0.2*V_{DC}
# of cells	470	548	392	392
Total IGBT VA rating	4.58 GVA	5.11 GVA	6.2 GVA	3.1 GVA
Total diode VA rating	0 GVA	0 GVA	0 GVA	3.1 GVA

This is in line with the type of cells currently used by the manufacturers of MMC converters. It is however acknowledged that in the case of the HVDC chopper circuit, the manufacturer prefers the use of 4.5 kV devices connected in series to implement the IGBT valves [92].

Looking at the results from the table, it can be concluded that the HVDC chopper, which uses valves of series connected IGBTs, is the topology that requires the smallest amount of installed semiconductor power. Despite the higher complexity of the gate drivers and the need for passive snubbers to operate the series connected devices, this fact plus the absence of a cell capacitance translates in the most compact solution out of the four circuits.

Regarding the multilevel topologies, the multilevel chopper requires the smallest amount of IGBT installed power but the largest amount of diode installed power. The full-bridge cell presents the highest needs of all the circuits in terms of IGBT installed power and therefore represents the higher cost in silicon and associated gate drivers. However when utilizing the sparse bridge cell, the full-bridge circuit is a more attractive option with respect to the half-bridge circuit since the total amount of IGBT installed power is lower.

3.7.3 Cell capacitors

Multilevel DBS circuits include a capacitor inside each cell. In MMC cells, this capacitor represents the largest size element, and also a significant portion of the total cost. As presented earlier in this chapter, the required cell capacitance is a function of the average current, balancing period and desired cell voltage ripple. As opposed to a VSC, where minimizing switching losses is important to improve the overall efficiency, in a DBS, with the efficiency not being a concern, shorter balancing periods are possible, as far as the thermal limits of the semiconductors are not exceeded. This allows for a reduction of the required cell capacitance,

reducing size and cost.

Example

Table 3.4 presents the resulting capacitance values for each of the circuits as well as the total energy stored in the DBS valve. Expression (3.14) is used for the multilevel chopper circuit, and (3.36) for the half-bridge and full-bridge multilevel circuits. Dolwin 3 ratings and LOVL and UOVL values from table 3.1 are used. For the half and full-bridge circuits, V_A is set as 20% of V_{DC}. The value of the braking resistor is taken from Table 3.2, and a dv/dt of 250 MV/s is considered. A 10% cell voltage ripple is chosen and 100μs balancing period is selected for a consistent comparison in the three cases.

Table 3.4 Total stored energy for multilevel DBS circuits.

	Multilevel Chopper	Half-Bridge Multilevel	Full-Bridge Multilevel
# of cells per arm	196	235	196
Value of C_{cell} [μF]	744	143	114
Total DBS valve energy [kJ]	236.2	54.4	36.2

The results show that for this particular set of parameters, the multilevel chopper requires the largest amount of stored energy in the converter. This is explained by the fact that in the half-bridge and full-bridge circuits current flows through the cell capacitors only during certain commutation period subintervals. This is not true for the multilevel chopper circuit, where current flows permanently through some capacitors in the valve.

The stored energy in the half-bridge and full-bridge circuit valves are reduced to 1/5th and 1/6th of the value for the multilevel chopper, which anticipates more compact valves.

3.8 Summary of the chapter

Dynamic braking systems are the current solution to implement fault ride-through capability in VSC-HVDC connected offshore wind farms. A DBS basic structure combines a power electronics valve arrangement and one or several resistive devices for energy dissipation. Four alternative DBS circuits have been studied in the chapter.

In a similar trend to the one experienced in voltage source converters, three multilevel topologies, made up with identical series connected cells have been

studied to mitigate some of the drawbacks of the HVDC chopper solution, usually considered in literature. Since multilevel alternatives present switched capacitors in the current path, a correct balancing of the cell stored energy must be ensured, keeping the cell capacitor voltages within the desired levels. A control strategy has been developed for each circuit to ensure a correct power modulation while keeping the HVDC system over-voltage during the fault within predefined limits. In the case of the multilevel topologies, additional control functions have been implemented to ensure the cell energy balance.

The multilevel chopper circuit, with local energy dissipation inside each cell, allows for a relatively straightforward energy balancing mechanism, whilst both the half-bridge and full-bridge multilevel topologies require a particular voltage modulation strategy to ensure the energy balance. The equations which govern the proposed modulation techniques have been derived. These have been used to size the different circuit components and to identify the circuit trade-offs.

Cost and size, often mentioned as the drawback with dynamic braking systems, have been discussed with examples to show how the different circuits compare.

The concepts presented in this chapter have set the foundations for understanding the operation of each circuit and the implementation of a real-scale DBS. Computer simulations and results from a laboratory scaled-down test platform are presented in the coming chapters to demonstrate the validity of these concepts.

Chapter 4

Dynamic Braking Systems: Simulation studies

In this chapter the operation of the four DBS circuits explained in Chapter 3 is analysed using the results obtained from computer simulations. This is the first step towards the validation of the design methodology and the novel control strategies proposed for the circuits to limit the DC over-voltage during a fault ride-through event. This validation is later complemented in Chapter 6 with the results from a laboratory scaled-down experimental model.

A simplified model of a VSC-HVDC interconnector system is developed and presented at the beginning of the chapter together with the method of emulating the AC grid fault event using the fault ride-through (FRT) characteristic from existing grid codes. Matlab-Simulink with the SymPowerSystems toolbox is used for the modelling and simulation of the electrical system, the power electronics and control functions. The diagrams of the simulation models and the controller gains are available in Appendix D.

The comparison of the performance of the four DBS circuits is presented at the end of the chapter and conclusions are drawn.

4.1 Model of the HVDC interconnector

A simplified model of an HVDC interconnector for offshore wind farms (OWF) is implemented in order to test the DBS circuits in a realistic environment. The model, displayed in Fig. 4.1, includes both onshore and offshore VSC stations and associated AC supply. The VSC stations are implemented using a lossless average model which neglects the AC harmonics generated by the converter commutation, which are not necessary for the study of the DBS operation. The HVDC cables are implemented using an equivalent pi-section model which imposes certain limitations on the frequency range that can be represented, but sufficient to

represent the frequencies of interest. Finally a detailed switched model of the DBS circuits is used, since these are the main subject of the study.

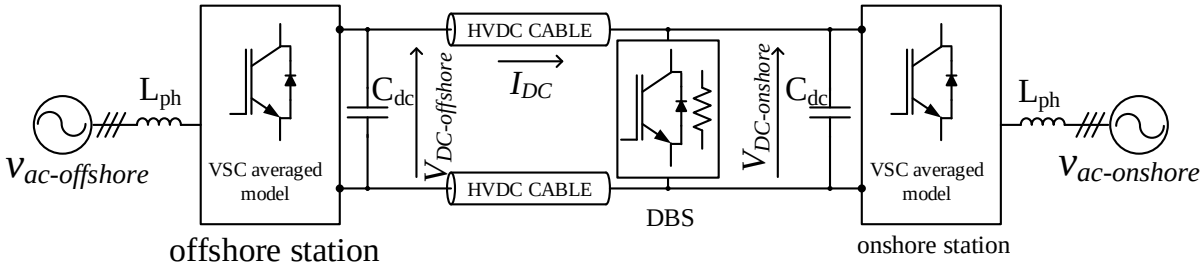


Fig. 4.1 HVDC interconnector model used in simulations.

4.1.1 VSC station equivalent averaged model

For this study AC side harmonics are of secondary importance. Therefore full switching models of the VSC stations are not required and an averaged model is sufficient and gives good results. The equivalent lossless averaged model [93], shown in Fig. 4.2, generates the average response of the controller and the switching devices in each converter. The model is built using controllable voltage sources on the AC side and a controlled current source on the DC side. The AC voltage sources generate the output of each of the 3 phases of the converter according to the output of the VSC controller current loop transformed into the abc reference frame. For the calculation of the DC current, an ideal lossless converter is considered and the principle of power balance between the AC and the DC side (4.1) is used, resulting in expression (4.2):

$$V_{DC}\, I_{DC} = v_a\, i_a + v_b\, i_b + v_c\, i_c \tag{4.1}$$

$$I_{DC} = \frac{v_a\, i_a + v_b\, i_b + v_c\, i_c}{V_{DC}} \tag{4.2}$$

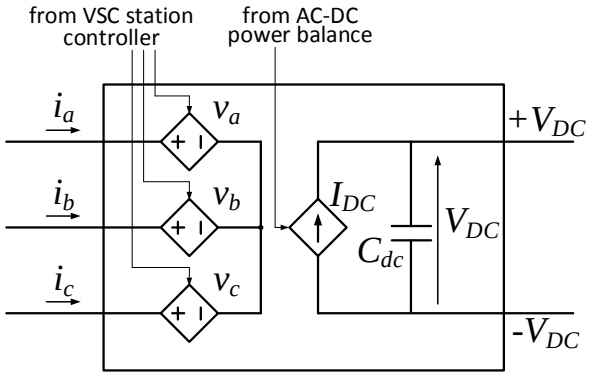


Fig. 4.2 Averaged model of the VSC station.

4.1.2 HVDC cable equivalent model

Transmission lines and cables have capacitive, resistive and inductive components which, for long transmission distances, are significant and need to be taken into account for the simulation of the HVDC transmission system. These components are uniformly distributed along the cable. However, models based on lumped parameters, such as the pi-section equivalent, can be used in order to reduce the complexity of the simulation at the expense of some accuracy loss in the results [94], being this the main reason for choosing it for this work. Another advantage of this equivalent model is that it can also be physically implemented in an experimental set-up using discrete components.

Equivalent model using π-sections

The N-sections pi equivalent circuit of the cable is displayed in Fig. 4.3. Being an approximation, this way of modelling HVDC cables has its own limitations. The number of sections required for the simulation depends on the range of frequencies of interest for the study. The maximum frequency that can be represented with a pi equivalent model is approximated with expression (4.3):

$$f_{max} = \frac{N_{sect}\, v}{8\, l_{cable}} \tag{4.3}$$

Where,

- N_{sect}: number of π-sections included in the equivalent model $(-)$
- v: propagation speed in the cable calculated as $\frac{1}{\sqrt{L\,C}}$ with L expressed in H/km and C in F/km (km/s)
- l_{cable}: the total cable length (km)

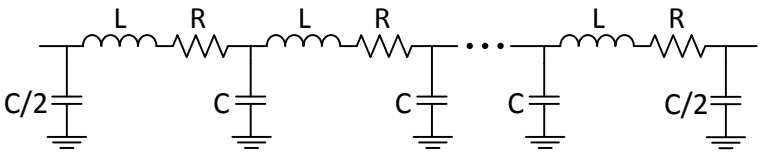


Fig. 4.3 Equivalent cable model based on π-sections.

The experience within GE when running this type of simulation has shown that best results are obtained when using one pi section for each 50 km of cable, and to always use a minimum of two pi-sections. Once the number of pi-sections to be used for the model is decided, the values of R, L and C are calculated. Data from the cable manufacturer can be used if available. Alternatively, the mathematical equations that allow calculating these parameters when data is not available are presented next.

Cable parameter approximation

Offshore HVDC interconnectors based on VSC converter technology use DC cables with cross-linked polyethylene (XLPE) insulation. Data from manufacturers concerning the electrical parameters of the cables are scarce since they are generally kept confidential. A method for calculating the cable's RLC parameters for the pi-sections model was established at the beginning of this research project and is presented next.

The simplified cable structure represented in Fig. 4.4 is used for this approximation. Only two layers are considered: the copper core and the XLPE insulation. Two parallel radial cables placed at a distance D from each other, as it is the case for the submarine cables of the HVDC interconnector, are considered. The required parameters for the calculations are, with all the values specified in meters:

- r: radius of the copper conductor (m).
- t: insulator layer thickness (m).
- D: distance between the two conductors (m).

The following additional parameters also need to be defined:

- ρ_{cu}: copper resistivity = 17.8 x 10^{-9} ($\Omega.m$).
- ϵ_0: permittivity of free space = 8.8541 x 10^{-12} (F/m).
- ϵ_r: relative permittivity of XLPE insulator = 2.3 (-).
- μ_0: permeability of free space = 4π x 10^{-7} (H/m).

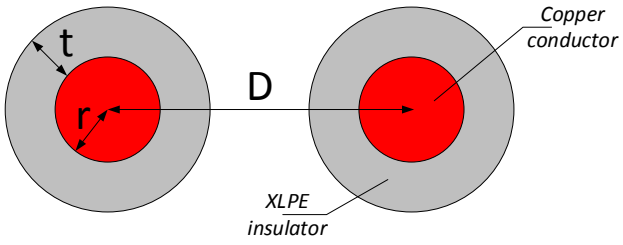


Fig. 4.4 Simplified cable layers for the RLC parameters estimation.

Based on the previous parameters all expressed in SI units, the mathematical expressions to calculate the cable parameters per meter of cable are presented in (4.4), (4.5) and (4.6) [95]:

$$R = \frac{\rho_{cu}}{\pi\, r^2} \qquad (\Omega/m) \tag{4.4}$$

$$C = \frac{2\,\pi\,\epsilon_0\,\epsilon_r}{ln\left(\frac{r+t}{r}\right)} \qquad (F/m) \tag{4.5}$$

$$L = \frac{\mu_0}{4\,\pi}\left(0.5 + ln\left(\frac{D^2}{r^2}\right)\right) \qquad (H/m) \tag{4.6}$$

Expression (4.6) represents the mutual inductance between the parallel cables (loop inductance) and is valid for small values of D (D<2m), which is usually the case for HVDC interconnections where both cables are laid together inside the same trench. For larger separations the cable internal inductance starts playing a significant role and needs to be taken into account. However, this approximation is generally valid for the offshore interconnector where both submarine cables are laid inside the same trench.

4.1.3 Full size interconnector scaling down

For the simulations of the HVDC interconnector a detailed switching model of the DBS circuits is implemented. The simulation of a full scale DBS would have been complex, with excessively long simulation times and large memory requirements due to the large number of switching events to be processed. Taking as a reference the parameters for Dolwin 3 project [24], a scaled down model with a rated DC voltage of 25 kV and 1.375 MW of active power is implemented. The resulting ratings for the model are summarized in Table 4.1. The DC capacitance is calculated to maintain the same time constant of the HVDC link $\tau_{hvdc} = E_{stored}/P_n$ as in the full scale system which is around 50 ms.

The DC cable parameters are calculated using expressions (4.4), (4.5) and (4.6) for a cable core section of 1200 mm^2, XLPE insulator thickness of 25 mm [96] and a distance between the two parallel cables of 0.2 m. The resulting values per km are displayed in Table 4.2. The fastest dynamics among the DBS circuits correspond to the HVDC chopper which switches at a frequency of 1 kHz. Using this values in expression (4.3) results in 12 π-sections required to implement the

Table 4.1 Parameters of the reduced scale model used in simulations.

Parameter	Value
Nominal power	1.375 MW
DC bus voltage	25 kV
Converter side AC voltage	13.7 kV
Equivalent VSC DC capacitance	210 μF
Phase inductor	226 mH
DBS valve	16 cells
DBS cell voltage	1.6 kV

cable equivalent model.

Table 4.2 DC cable parameters.

Parameter	Value	Units
Conductor section (Cu)	1200	mm^2
Cable length	160	km
Resistance	14.16	$m\Omega$/km
Capacitance	157	nF/km
Inductance	510	μH/km
π-sections	12	-

4.1.4 Fault ride-through event simulation

In order to emulate the onshore grid fault and to test the operation of the DBS circuits at different power dissipation levels, the amplitude of the onshore AC supply is controlled to follow the voltage-time profile displayed in Fig. 4.5, which is based on the UK fault ride-through characteristic that was presented in Fig. 2.12 of Chapter 2.

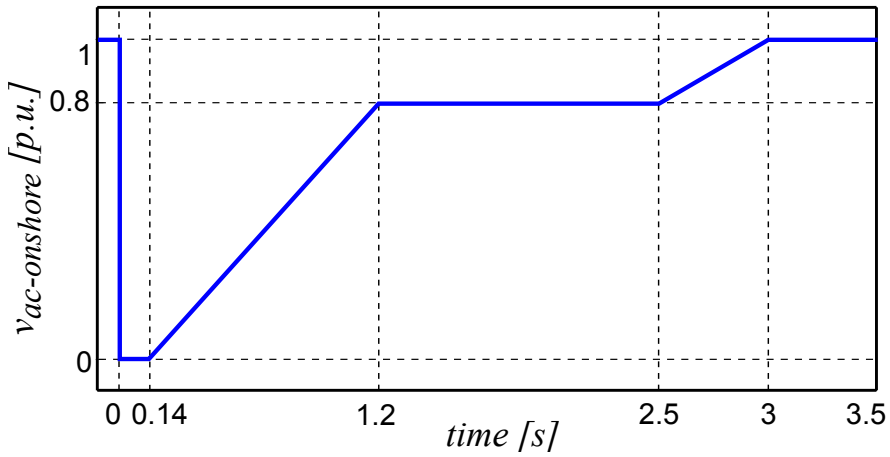


Fig. 4.5 Voltage-time profile used for emulating the onshore grid fault.

4.2 Evaluation of the fault ride-through event using DBS

The results of the HVDC interconnector operation study during an onshore grid fault are presented in this section. For ease of comparison, the obtained results are expressed as per unit (pu) values using the base system presented in Chapter 3. Along the text the different DBS circuits are numbered from 1 to 4. Both nomenclatures are used indistinctly through the text:

- DBS#1: HVDC chopper circuit
- DBS#2: Multilevel chopper circuit
- DBS#3: Half-bridge multilevel circuit
- DBS#4: Full-bridge multilevel circuit

4.2.1 Onshore AC grid fault

Firstly, the fault ride-through event is simulated without any protective measure to mitigate the DC over-voltage. The resulting waveforms are presented in Figs. 4.6 and 4.7. As observed in Fig. 4.6a, at time 1.5 s the fault is applied, and the onshore AC voltage collapses to zero per unit. At the same time, the onshore VSC converter enters the over-current protection mode, limiting the maximum current value to 1.1 pu, this is, 10% above the nominal value (Fig. 4.6b).

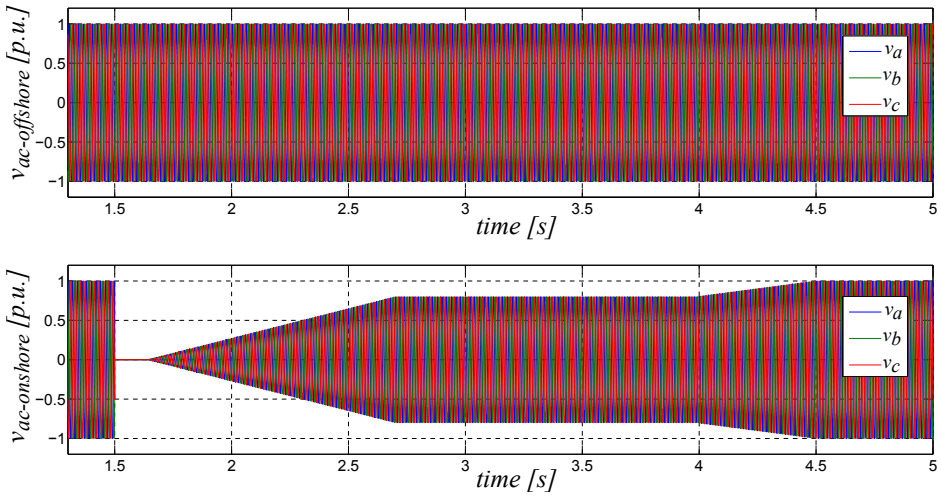
As a result of the fault, the onshore VSC loses the capability to inject active power in the AC grid while the offshore VSC continues to inject nominal power into the HVDC link (Fig. 4.7a). This creates the power unbalance with the excess power flowing into the DC equivalent capacitance which results in a rapid increase of the DC voltage as observed in Fig. 4.7b. During the solid 3-phase short circuit emulated for the first 140 ms (voltage collapse to zero per unit), the time to reach a predefined DC over-voltage level is expressed as (4.7):

$$T_{OV} = \frac{C_{DC}\, V_{DCn}}{2\, P_{DCn}} \left(V_{OV}^2 - V_{PF}^2 \right) \tag{4.7}$$

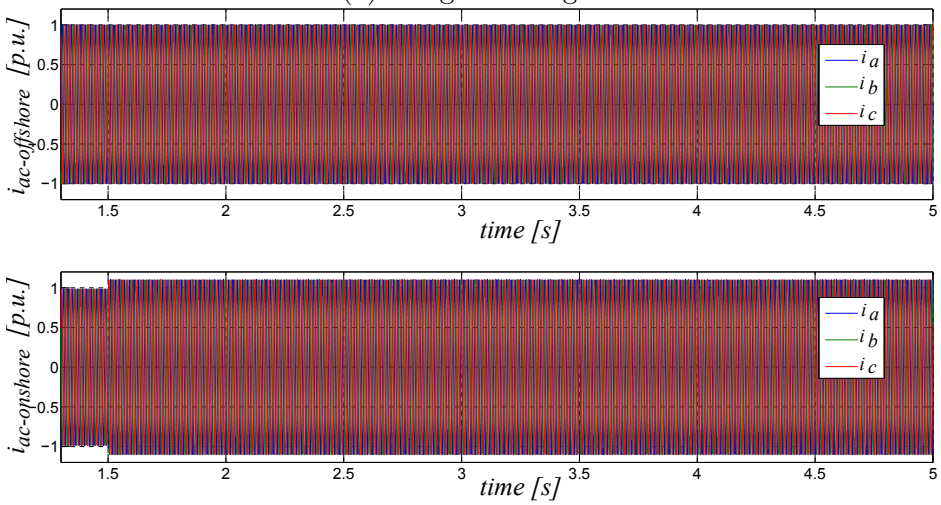
Where

- T_{OV}: is the time to reach the predefined DC over-voltage level (s)
- C_{DC}: is the equivalent DC link capacitance (F)
- V_{DCn}: is the DC system nominal voltage (V)
- P_{DCn}: is the DC system nominal power (W)
- V_{OV}: is the DC over-voltage level (per unit)
- V_{PF}: is the DC voltage pre-fault level (per unit)

As mentioned in [66] the over-voltage threshold for the transmission system and wind farm trip is normally set at around 1.3 pu. In this work, as was presented in Table 3.1, the DBS operation is designed to limit the maximum over-voltage to 1.1 pu at the onshore station. Using the interconnector parameters from Table 4.1 in (4.7) gives a reaction time for the DBS to reach nominal power dissipation of 20 ms before the 10% over-voltage level is reached. The zoomed window of Fig.

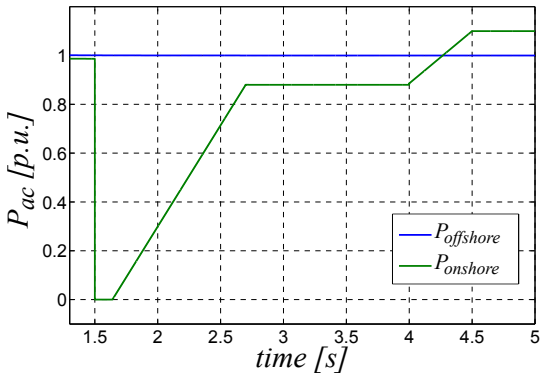


(a) AC grid voltages

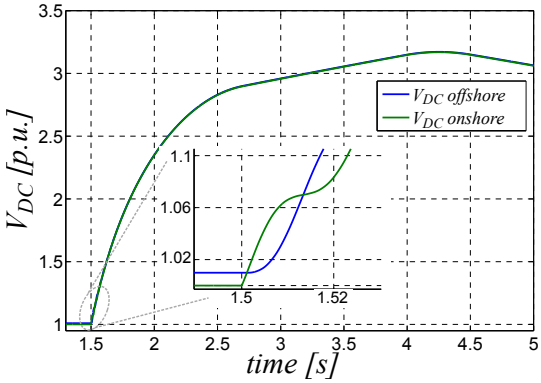


(b) AC grid currents

Fig. 4.6 AC grid waveforms both onshore and offshore during the specified fault event.



(a) Active power flow on both VSC stations



(b) DC voltage on both VSC station

Fig. 4.7 Active power flow and DC voltage during a fault with no DBS in operation.

4.7b shows how the DC voltage at the onshore station exceeds the 1.1 pu voltage just after time 1.52 s, this is, 20ms after the start of the fault. Without any protection in place, as observed in the figure, the reached over-voltage exceeds 3 times the DC voltage nominal value (V_{DCn}). The control of both VSC stations allows for a maximum AC current of 1.1 pu, as commonly implemented in real converters. As observed in Fig. 4.7a this allows for the active power injection, once the AC grid voltage is recovered, to go up to 1.1 pu, which helps for a faster DC voltage stabilization.

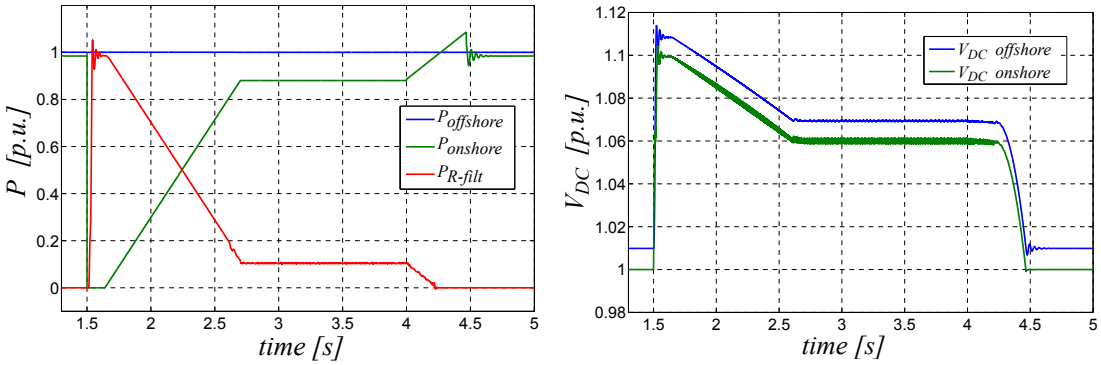
4.2.2 Operation of the HVDC chopper DBS

The first circuit to be tested, DBS#1, is the high voltage version of the standard motor drive choppers, which uses series connection of IGBTs to reach the required voltage blocking capability. Using expression (3.6), the required braking resistor value is calculated. Table 4.3 shows the DBS parameters used in simulation, where a 1kHz carrier frequency is chosen for the PWM with the DBS, in line with the switching frequencies used with power IGBTs in HVDC converters. The resulting waveforms of the FRT event when the operation of DBS#1 is enabled are presented in Fig. 4.8.

In Fig. 4.8a it is observed how the loss of power injection capability by the onshore VSC is perfectly compensated by the power dissipation in the DBS all along the fault event. In the figure the displayed DBS power has been filtered using a moving average filter with a window size of 10 commutation periods of the DBS in order to show the evolution of the average power dissipation for the fault duration. The instantaneous power dissipation in the DBS is presented in Fig. 4.8c, where the characteristic chopped waveform of this circuit is observed, in this case operating at 1 kHz. For almost 10 ms after the fault start, the DBS does not dissipate any power. This is the delay experienced for the DC voltage to reach the LOVL of 1.05 pu that triggers the DBS operation, as defined in Table 3.1. From this point onwards, it can be seen how the duty cycle of the power pulse in Fig. 4.8c progressively increases until maximum power dissipation is reached at time 1.53 s, with the DBS valve permanently turned on. In Fig. 4.8a it is observed how the power extracted onshore is slightly inferior to the power

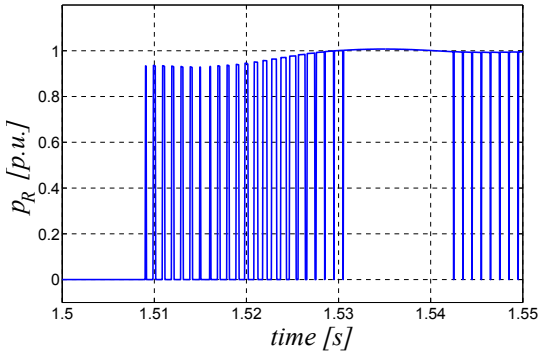
Table 4.3 DBS#1 circuit dimensioning.

DBS#1		
Parameter	Value	Units
R_{dbs}	550	Ω
$f_{carrier} = {T_{carrier}}^{-1}$	1	kHz



(a) Active power flows

(b) VSC station DC voltages



(c) Instantaneous power dissipation in R_{dbs}

Fig. 4.8 Simulation results with the HVDC chopper circuit (DBS#1).

injected offshore. This is due the power loss in the resistive part of the cable equivalent model, and the reason why the DBS valve does not reach 1 pu power dissipation at the beginning of the fault. As the AC grid voltage recovers, the DBS power is progressively reduced, until the operation of the DBS is completely stopped once the DC voltage goes below 1.05 pu. Fig. 4.8b corroborates the successful operation of the DBS circuit to limit the maximum over-voltage to 1.1 pu at the onshore location. The higher voltage at the offshore location, reaching almost 1.11 pu, is due to the voltage drop in the HVDC cable. The DC voltage falls below the LOVL at time 4.2 s, stopping the power dissipation by the DBS.

4.2.3 Operation of the multilevel chopper DBS

The relevant parameters employed for the simulation of the FRT event when DBS#2 is enabled are displayed in Table 4.4. The DBS valve is implemented with 16 cells, which results in a cell average voltage of 1.6 kV. The value of the distributed braking resistor is calculated according to (3.9). For the cell voltage balancing function, which ensures the total valve energy is well distributed among all the cells, a frequency of execution for the balancing algorithm of 2 kHz is implemented. This frequency is chosen so that the effective switching frequency for each IGBT switch inside the cells is below the 1kHz value taken as a reference from HVDC converters. The cell capacitance is then calculated using (3.14) for

a 10% peak to peak voltage ripple.

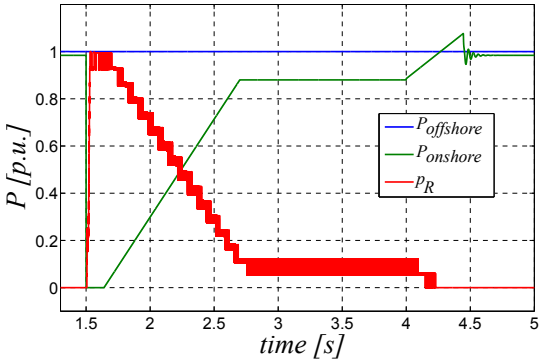
Table 4.4 DBS#2 circuit dimensioning.

DBS#2		
Parameter	Value	Units
N	16	-
R_{dbs}	34.4	Ω
C_{cell}	145	μF
$f_{balancing} = {T_{balancing}}^{-1}$	2	kHz

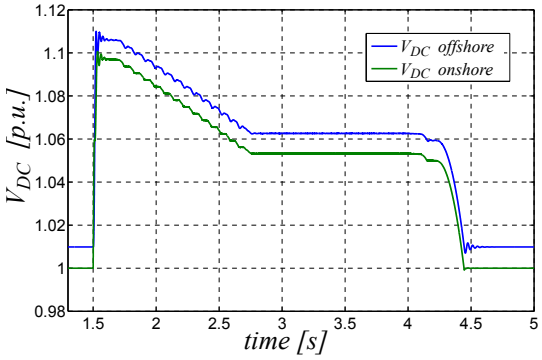
The results of the simulation are presented in Fig. 4.9. In Figs. 4.9a and 4.9c the most remarkable characteristic of this circuit is observed, this is, the ability to achieve a very fine regulation of the dissipated power, which can be adjusted in as many steps as cells are present in the DBS valve. Fig. 4.9c clearly shows this stepped power characteristic when the power dissipation is increased from zero to nominal power at the start of the fault, when the DC link voltage starts raising. The current absorbed by the DBS has the same curve as this instantaneous power dissipation, this is, a DC component with a small superimposed ripple. This is a big advantage since it also reduces the ripple in the DC link voltage as observed in Fig. 4.9b. This figure also validates the successful operation of this second circuit to keep the DC link over-voltage within desired limits and ride through the fault. Figs. 4.9d and 4.9e display the voltage of the 16 cell capacitors. Fig. 4.9d presents the detail of the cell capacitor voltage evolution as the power dissipation is ramped-up at the start of the fault. It is observed that at nominal power dissipation the currents circulate through the braking resistors in all the cells and therefore there is no ripple in the cell capacitor voltages. In both figures it is also observed that the maximum voltage ripple is within the desired 10% peak to peak, which demonstrates the validity of expression (3.14) for sizing the cell capacitance. Fig. 4.9e validates the success of the cell capacitor balancing function to keep the valve energy well distributed through the whole operation span of the circuit.

4.2.4 Operation of the half-bridge DBS

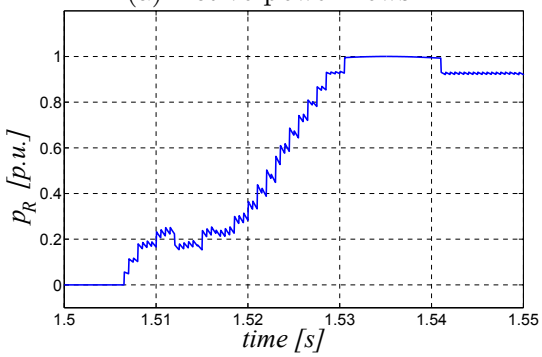
The simulation results of DBS#3 help to demonstrate the validity of the developed novel modulation technique. The relevant parameters of the simulated model are displayed in Table 4.5. The value of voltage parameter V_A is defined for the DBS to generate a valve voltage 25% larger than the DC voltage. This additional voltage makes it necessary to also increase the number of cells in the DBS valve by 25% in order to keep the same cell average voltage of 1.6 kV as in the other two modular circuits. Using expression (3.23) the value of the lumped



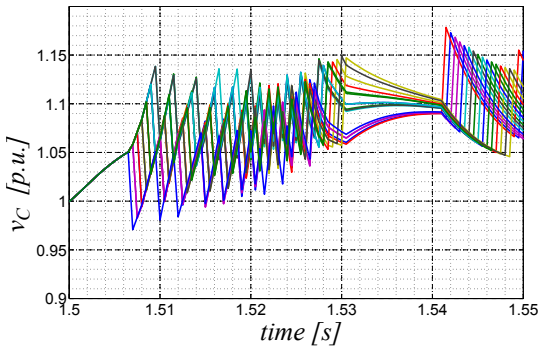
(a) Active power flows.



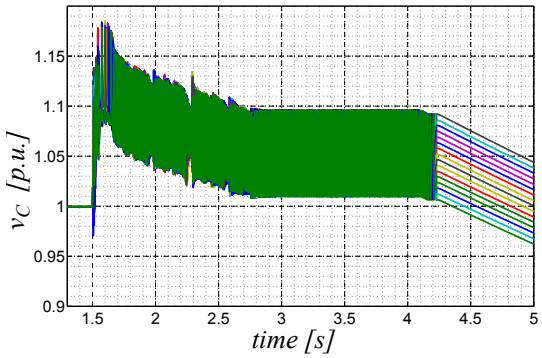
(b) DC voltage on both VSC stations.



(c) Detail of instantaneous power dissipation in R_{dbs} during the first 50ms of the fault.



(d) Detail of cell capacitor voltage during the first 50ms of the fault.



(e) Cell capacitor voltages evolution for the complete fault duration.

Fig. 4.9 Simulation results with the multilevel chopper circuit (DBS#2).

Table 4.5 DBS#3 circuit dimensioning.

DBS#3		
Parameter	Value	Unit
N	20	-
V_A	$V_{dc}/4$	V
R_{dbs}	428	Ω
C_{cell}	55	μF
T_m	4	ms
dv/dt	125	V/μs
$f_{balancing} = {T_{balancing}}^{-1}$	20	kHz

braking resistor is calculated while (3.36) is used to size the cell capacitance for a 10% peak to peak voltage ripple as with the previous circuit. The values for the trapezoidal pulse period, the DBS voltage derivative and the execution frequency of the cell voltage balancing function are also defined in the table. The balancing function is executed substantially faster than for the DBS#2 circuit. This is required to obtain a good resolution in the ramps of the trapezoidal pulses. A minimum of 4 voltage steps has been used here as the dimensioning criteria. A faster frequency will allow to increase this resolution even further. The effect of the balancing frequency choice and the voltage quantization due to the reduced number of cells can be observed in the steps of the real valve voltage waveform from the simulation results in Fig. 4.10. The minimum of 4 voltage steps during the ramping up/down process is met. Additionally, the voltage quantization effect, which introduces an error between the desired and real DBS valve voltage, is observed particularly well during the peak voltage generation. This errors have an impact on the level of power dissipation and the DBS energy balance, which has to be compensated by the DBS controller. A full size converter, with around 400 cells, would offer a much better resolution, almost eliminating this problem.

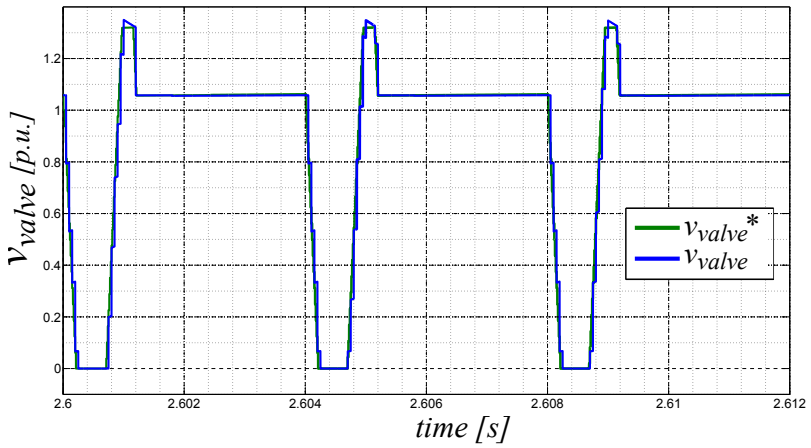
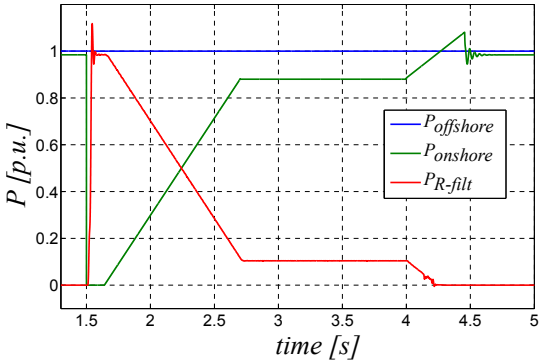
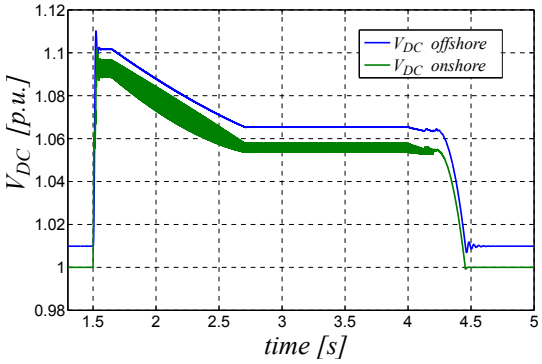


Fig. 4.10 Quantization effect in the DBS#3 valve voltage with the controller demand (green) and the real DBS valve voltage (blue).

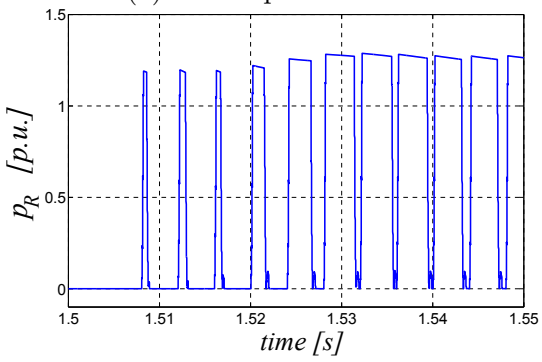
The additional simulation results are presented in Fig. 4.11. As with DBS#1, in Fig. 4.11a the averaged power dissipation in the DBS circuit shows a good match with the power injected in the DC link by the offshore VSC station to absorb the excess power in the DC link. The detailed instantaneous power dissipation is presented in 4.11c, where the evolution of the modulation function to increase the power dissipation is observed by the increase in the width of the power pulse. Fig. 4.11e shows the cell capacitor voltage evolution for the complete duration of the fault, where a correct operation of the proposed energy balancing function and the valve energy balance achieved by the proposed modulation strategy are both validated. The peak to peak ripple is well within the 10% value used for sizing the cell capacitors.



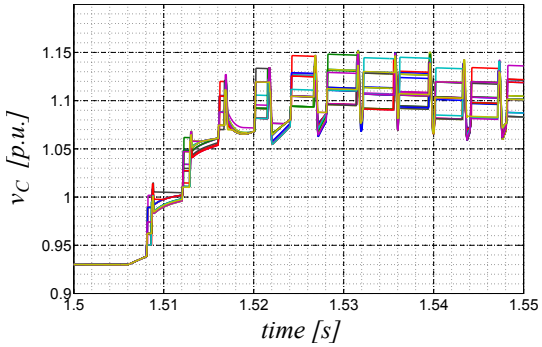
(a) Active power flows.



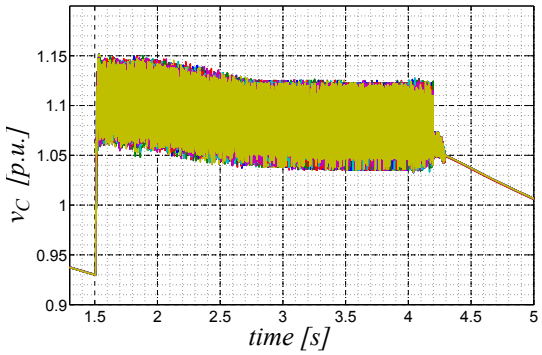
(b) DC voltage on both VSC stations.



(c) Detail of instantaneous power dissipation in R_{dbs} during the first 50ms of the fault.



(d) Detail of cell capacitor voltage during the first 50ms of the fault.



(e) Cell capacitor voltages evolution for the complete fault duration.

Fig. 4.11 Simulation results with the half-bridge multilevel circuit (DBS#3).

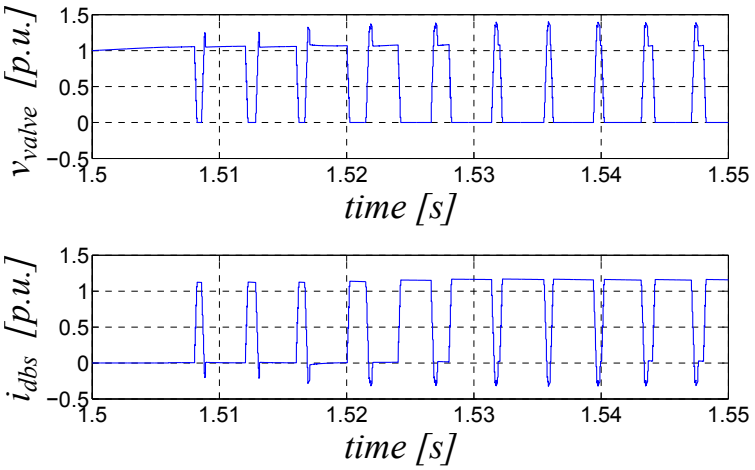
Fig. 4.11d presents the detail of the cell capacitor voltage evolution at the fault start. When the DBS is not in operation, there is no commutation of the cells, and the DC link voltage is shared by the 20 cells, so at this point the maximum voltage the DBS valve can produce is V_{DC} (1 pu), and not the required $V_{DC} + V_A$ (1.25) peak voltage for the trapezoidal pulse. As was presented in Fig. 3.19, it is this period where the valve generates $V_{DC} + V_A$ which ensures the valve energy balance by discharging the extra energy stored inside the cells. When the fault takes place, the DC link voltage starts raising and when it reaches the LOVL level, the DBS operation starts. At this point the DBS valve can only produce a peak voltage of V_{DC} and therefore, it starts storing energy in the cells but not discharging it, which causes the cell voltage to rapidly increase. Once the voltage in all the cells has increased to the point where the valve can generate the peak voltage $V_{DC}+V_A$, the energy balance in the valve can be maintained, as presented in Fig. 3.19. Therefore no control action is needed to pre-charge the DBS cells as this happens naturally during the initial instants of the fault as observed in Fig. 4.11d. At last, Fig. 4.11b confirms the successful operation of DBS#3 to limit the DC over-voltage to the desired levels during the fault ride-through event.

Fig. 4.12 shows a detail of the DBS valve voltage and current at three different points of operation during three different instants of the fault. Fig. 4.12a displays the change in the trapezoidal pulses when the power dissipation is ramped up from zero to nominal power during the first 50 ms of the fault starting at time 1.5 s. As observed the circuit operates inside the time modulation region (Fig. 3.20) and the duration of interval T_2 is progressively increased resulting in the progressive increase in the amount of power dissipated in the DBS, as needed since the onshore VSC does not extract any power from the DC link during the first 140 ms after the fault starts. Fig 4.12b shows the DBS operation at time 2.6 s, when dissipating 0.105 pu power and T_2 duration approaches zero (crossover point), which confirms that the modulation works as expected when the power dissipation demand goes down to low values. Finally Fig. 4.12c displays both valve voltage and currents when the power dissipation falls below 0.1 pu (after time 4 s) and the DBS operates in the amplitude modulation region in order to regulate the power dissipation to very small values. This confirms that the trapezoidal modulation operates correctly in order to adapt the DBS power dissipation to the needs of the DC link.

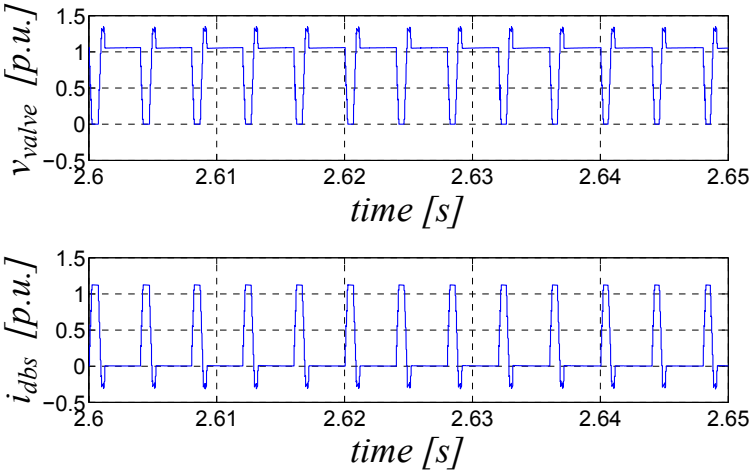
All of these results corroborate the validity of the developed modulation and control strategy for the operation of DBS#3.

4.2.5 Operation of the full-bridge multilevel DBS

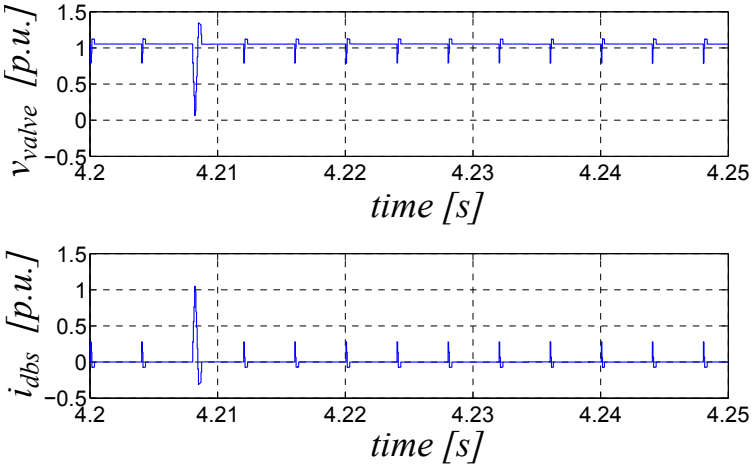
The simulation of DBS#4 is also used to demonstrate the validity of the modulation technique, which is very similar to that of DBS#3. The relevant



(a) DBS valve voltage and currents during the power ramping up from zero to nominal power dissipation.



(b) DBS valve voltage and currents when operating in the time modulation region.



(c) DBS valve voltage and currents when operating in the amplitude modulation region.

Fig. 4.12 Detail of the different modulation regions during the DBS#3 operation.

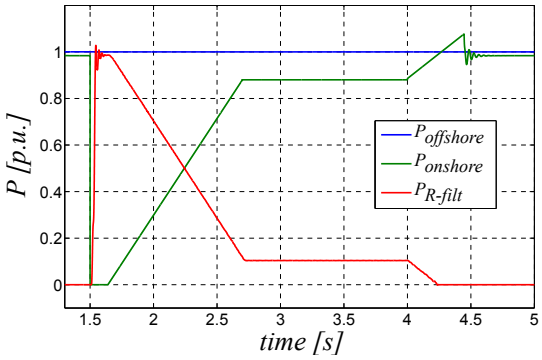
Table 4.6 DBS#4 circuit dimensioning.

DBS#4		
Parameter	Value	Units
N	16	-
V_A	$V_{DC}/8$	V
R_{dbs}	529	Ω
C_{cell}	35	μF
T_m	4	ms
dv/dt	125	V/μs
$f_{balancing} = {T_{balancing}}^{-1}$	20	kHz

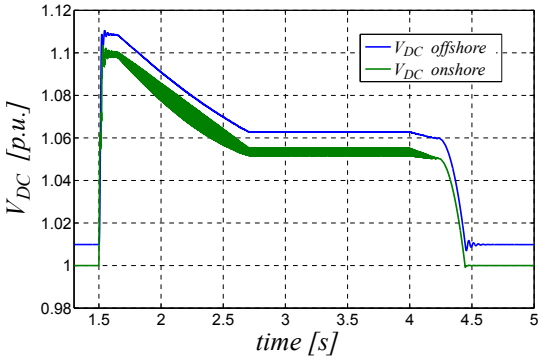
parameters of the simulated model are displayed in Table 4.6. In this case the value of voltage parameter V_A, which represents the amplitude of the negative voltage pulse generated by the DBS valve to discharge the energy stored in the cells, is set to $1/8^{\text{th}}$ of the DC voltage value. Therefore in the simulated circuit, 2 cells are used to generate this voltage. In this case, as for DBS#2, 16 cells are used in the DBS valve. The value of the braking resistor is calculated using expression (3.43) while the cell capacitance is calculated from (3.36) for a 10% peak to peak voltage ripple. The values of the modulation period, voltage derivative and balancing frequency remain the same as the ones used with DBS#3.

The simulation results are displayed in Fig. 4.13. Fig. 4.13a displays, as already presented with other circuits, the correct operation of the DBS circuit in order to perfectly match the difference between the power in and out of the HVDC link through the VSC converters. The detail of the instantaneous power evolution at the start of the fault is shown in Fig. 4.13c, where the increase of the power pulse width with the raising DC voltage is well observed. Figs. 4.13e and 4.13d validate the valve energy balance obtained with the proposed modulation strategy and the correct operation of the cell capacitor balancing function, which keeps this total valve energy well distributed among the cells. The voltage ripple also corresponds well with the desired 10% value. At last, Fig. 4.13b proves the successful operation of DBS#4 to keep the DC voltage within the desired limits for the complete duration of the fault event.

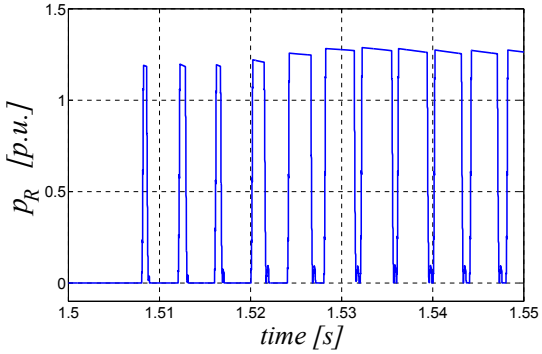
Fig. 4.14 presents the detail of the DBS valve voltage and current at three different points of operation of the trapezoidal modulation function during three different instants of the fault. Fig. 4.14a displays the change in the trapezoidal pulse when the power dissipation is ramped up from zero to nominal power during the fist 50 ms of the fault starting at time 1.5 s. As observed the circuit operates inside the first time modulation region (Fig. 3.32) and the duration of interval T2 is progressively increased resulting in the progressive increase in the amount of power dissipated in the DBS, as needed since the onshore VSC does not extract



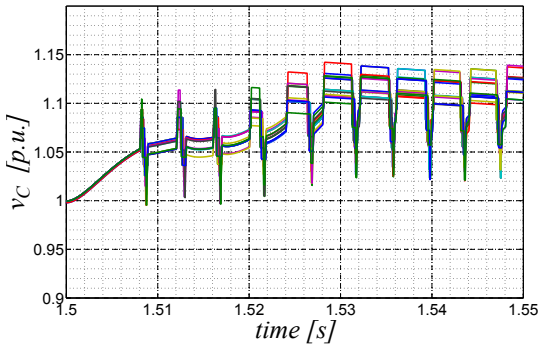
(a) Active power flows.



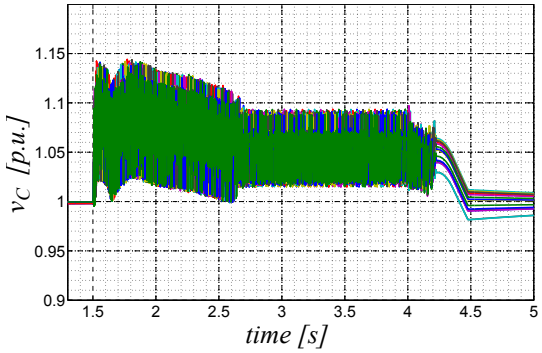
(b) DC voltage on both VSC stations.



(c) Detail of instantaneous power dissipation in R_{dbs} during the first 50ms of the fault.

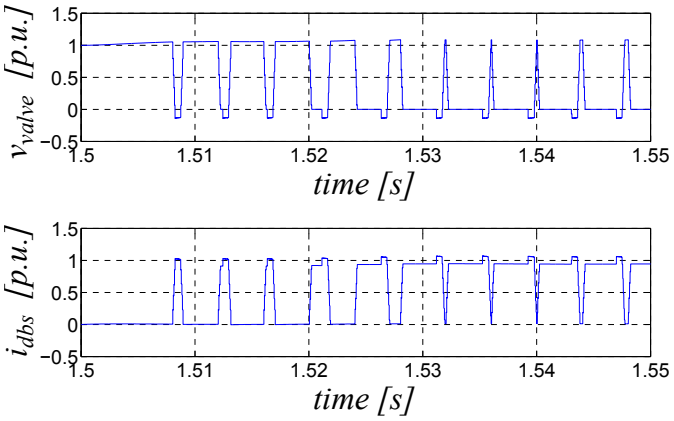


(d) Detail of cell capacitor voltage during the first 50ms of the fault.

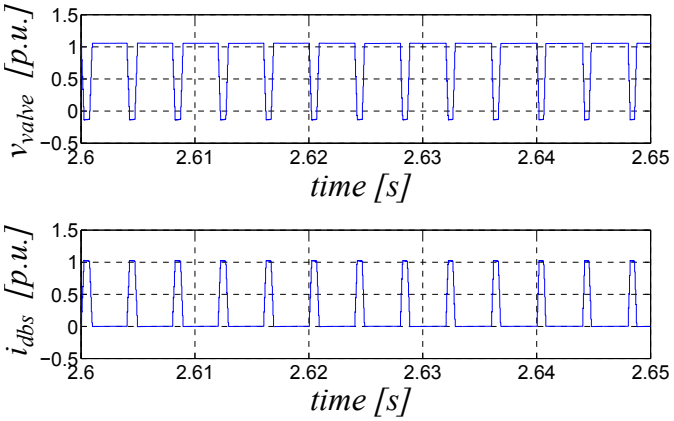


(e) Cell capacitor voltages evolution for the complete fault duration.

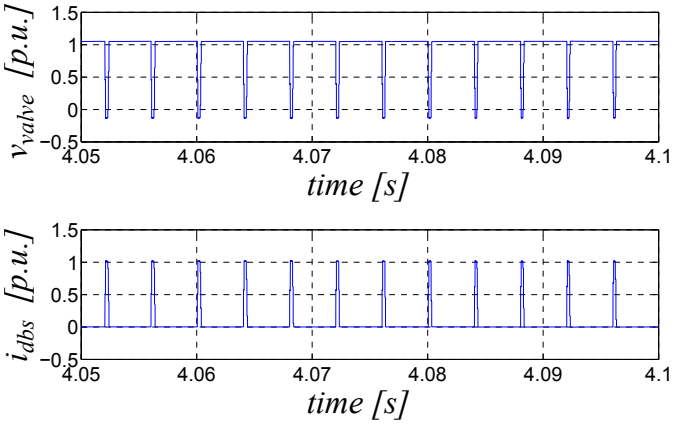
Fig. 4.13 Simulation results with the full-bridge multilevel circuit (DBS#4).



(a) DBS valve voltage and currents during the power ramping up from zero to nominal power dissipation.



(b) DBS valve voltage and currents when operating in the first time modulation region.



(c) DBS valve voltage and currents when operating in the second time modulation region.

Fig. 4.14 Detail of the different modulation regions during the DBS#4 operation.

any power from the DC link during the fist 140 ms after the fault starts. In this region a constant dv/dt is used to ramp up/down the trapezoidal pulses. Fig. 4.14b shows the DBS valve voltage at time 2.6 s when the duration of subinterval T_2 has reached zero at the point where the modulation exists the first time modulation region to enter the second time modulation region in order to further reduce the amount of power dissipation in the braking resistor. At last Fig. 4.14c shows the valve voltage when the circuit operates within the second modulation region that goes from the crossover point down to zero power dissipation. Within this region of operation, the duration of interval T_4 is reduced. Simultaneously, the value of dv/dt is increased to keep the valve energy balance, as described in section 3.5.2.

The presented results for DBS#4 equally corroborate the validity of the proposed modulation and control strategy to protect the HVDC interconnector during the fault ride-through event while ensuring the correct balance of the energy stored in the DBS valve. Identical simulation results are obtained when the sparse-bridge (section 3.5.4) is used in place of a full-bridge for the cell implementation, and therefore seems a better option in order to reduce the required number of IGBTs in the circuit.

4.3 Comparison of the four DBS circuits

A qualitative and quantitative comparison of the four DBS circuits is presented in this section in order to draw conclusions comparing the advantages of one circuit with respect to the others.

4.3.1 DBS valve voltage *dv/dt* and current

The voltage across the braking resistor generated by each of the DBS circuits is displayed in Fig. 4.15 and the current absorbed from the DC link is displayed in Fig. 4.16. Large voltage and current derivatives stress different components in the system, such as inductors, and present problems with radiated EMI, which can cause interference in adjacent structures and telecommunication equipment and for which proper shielding of the converter stations is needed. As observed in the figure, one of the advantages of DBS#3 and DBS#4 with respect to DBS#1 is the capability to control within certain margins the DBS valve voltage dv/dt, which results from the aggregation of the individual cell voltages, , slightly improving this aspect. However, DBS#2 with its distributed chopper inside each cell, offers the best performance of the four circuits, with a reduced voltage applied across each braking resistor and absorbing DC currents with minimal ripple from the HVDC link, which avoids voltage drops in the DC links inductance and the

charge/discharge of the DC link capacitors, hence minimizing the voltage ripple in the DC bus.

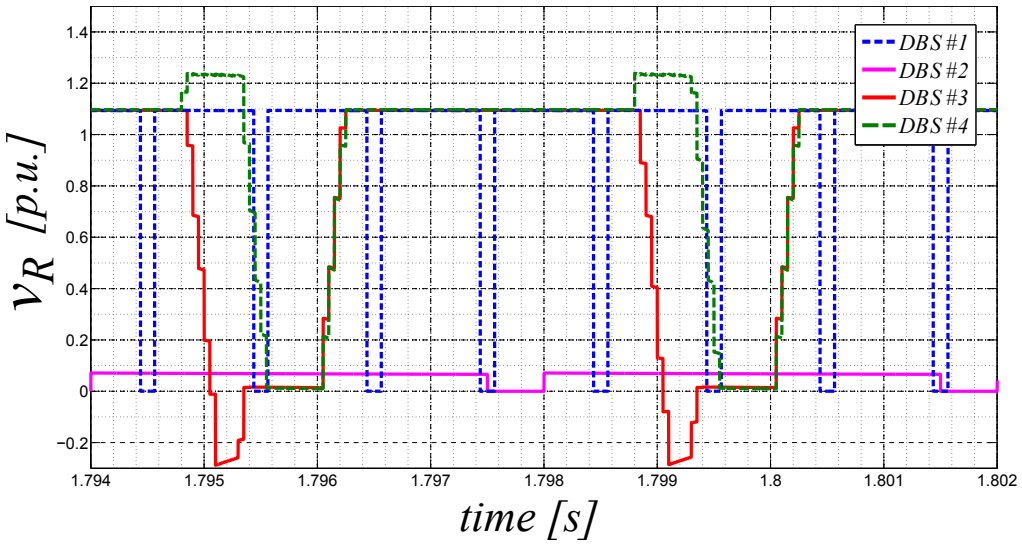


Fig. 4.15 Comparison of the voltage across the braking resistor in each DBS circuit.

From these same voltage and current waveforms, the characteristics of the required braking resistors can be determined, and are presented in Table 4.7. As observed, for this particular aspect, both DBS#3 and DBS#4 circuits present a small disadvantage since the voltage rating of the required resistor is slightly larger than for the other two circuits, which is likely to increase the resistor cost.

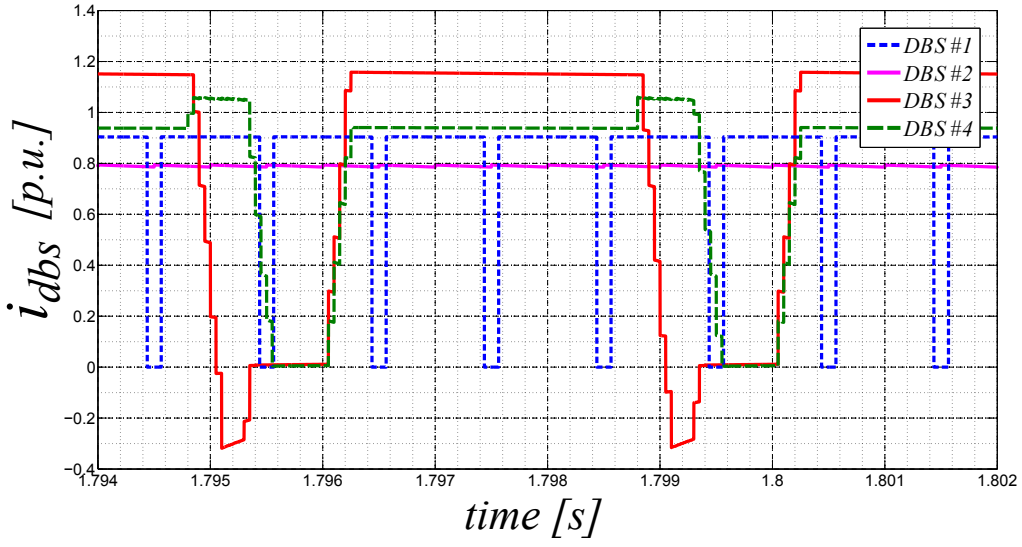


Fig. 4.16 Comparison of the current absorbed by each DBS circuit.

4.3.2 DC voltage during the fault

Fig. 4.17a shows the onshore DC voltage evolution during the fault event for the four circuits. As discussed, the four circuits succeed in limiting the DC

Table 4.7 Braking resistor requirements in the four simulated circuits.

	DBS#1	DBS#2	DBS#3	DBS#4 (sparse bridge)
# of R per arm	1	16	1	1
Value of R [Ω]	550	34.4	428	529
Energy rating [MJ]	3.5	0.22	3.5	3.5
V_{rating} [kV]	27.5	1.72	27.5	31.25

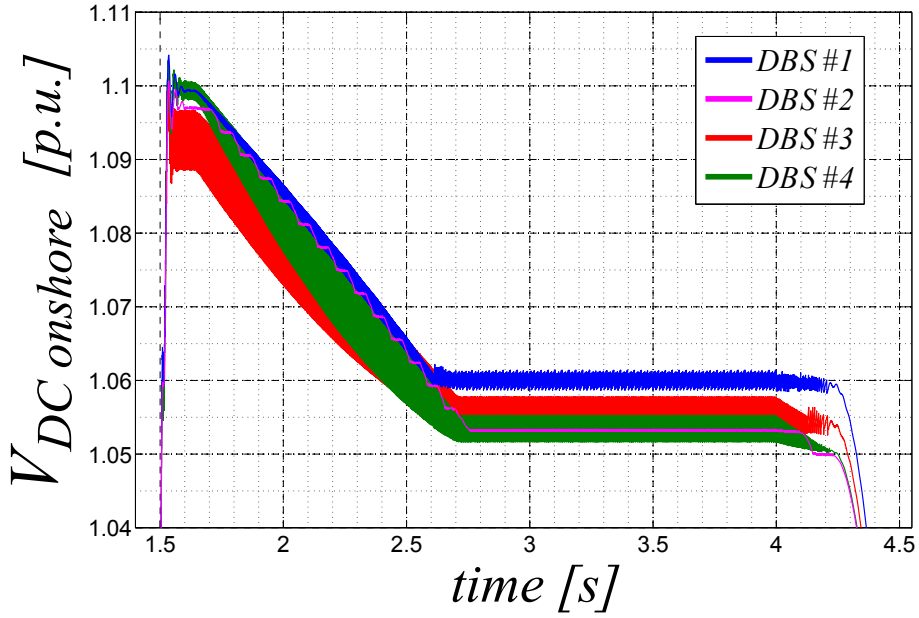
over-voltage below the desired value of 1.1 pu. However, as observed in the zoomed view of 4.17b, the main difference in the operation of the four circuits lies in the generated ripple as a consequence of the charge/discharge of the DC capacitance. DBS#2 generates the lower ripple thanks to the constant DC current absorbed by the circuit during the operation, as was shown in Fig. 4.16. The other three circuits absorb a pulsed current from the DC link, however, DBS#1 with a larger frequency of operation (1 kHz against 250 Hz), results in a lower DC link voltage ripple than with circuits DBS#3 and DBS#4, which show the worst performance for this particular aspect.

4.3.3 Number and rating of semiconductor switches

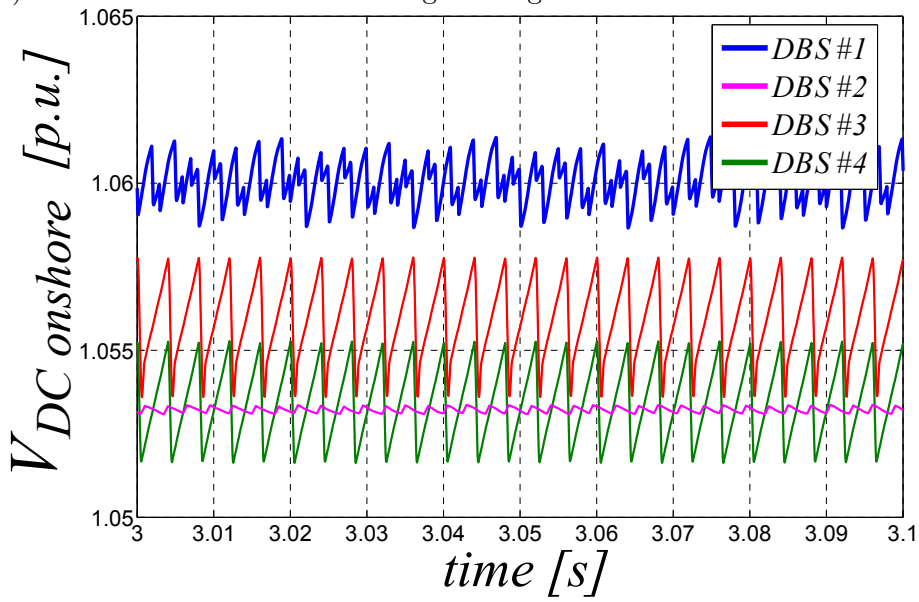
The next criteria used to compare the four DBS circuits evaluates the number and rating of the required semiconductors. The results of this comparison is summarized in Table 4.8. In the case of DBS#4, the sparse-bridge cell as presented in section 3.5.4 is used. As observed, concerning the VA rating of semiconductor switches, DBS#1 presents the best performance. Nonetheless, the limited number of suppliers of suitable IGBT devices and the complexity of the required technology to avoid dynamic voltage sharing problems when using hundreds of devices, still make this option very challenging. The second best performance is obtained with DBS#2, which despite presenting a higher total semiconductor VA rating than DBS#3, 66% of the total power is for diodes, reducing the cost and the required number of driving circuits. Modular circuits DBS#3 and DBS#4 both present the disadvantage of presenting a large IGBT VA rating. DBS#4 represents the worst performance of the four circuits despite the fact of halving the IGBTs VA rating which is replaced by diodes when using the sparse-bridge cell.

4.3.4 Cell capacitors

The last criteria to compare the four DBS circuits is the total amount of stored energy in the cell capacitors of the three modular DBS circuits. The results are presented in Table 4.9. The results confirm the analysis that had already been made in Chapter 3, with the multilevel chopper being the circuit which requires



(a) Evolution of the DC link voltage during the fault for each DBS circuit.



(b) Zoomed view of the DC link voltage ripple for each DBS circuit.

Fig. 4.17 Detail of the different modulation regions during the DBS#4 operation.

Table 4.8 Semiconductor requirements in the four simulated circuits.

	DBS#1	DBS#2	DBS#3	DBS#4 (sparse bridge)
# of levels/cells	16	16	20	16
Total IGBT VA rating [MVA]	2.6	2.6	7.4	5.3
Total diode VA rating [MVA]	2.6	5.2	0	5.3

the largest amount of stored energy since the current permanently flows through the capacitors during the circuit operation. This is different in the half-bridge and full-bridge multilevel circuits where the current only flows through the cell capacitors during certain subintervals of the trapezoidal voltage pulse, reducing the size of the required capacitors, hence reducing the total amount of stored energy in the valve. The slightly higher needs in terms of stored energy in the half-bridge circuit with respect to the full-bridge are explained due to the higher number off cells which are present in the DBS valve in order to generate the peak voltage of the trapezoidal pulse $V_{DC} + V_A$.

4.3.5 Conclusions

Starting with DBS#1, its biggest advantage would be the circuit simplicity and the best performance in terms of semiconductor VA rating. The use of series connected switches results in a very compact DBS valve (Fig. 3.6) with respect to the modular topologies, where the cell assembly including the capacitor takes significantly more space. Also the voltage rating for the braking resistor is lower than for circuits DBS#3 and DBS#4. The main concerns with the circuit are related to this same use of series connected switches. The complexity to master this technology for the operation of stacks of hundreds of devices, as required in HVDC, was one of the main drivers behind the development of modular alternatives in the case of VSC converters. Furthermore, the number of semiconductors suppliers which provide components suitable for this arrangement is also very limited. Finally, the high frequency commutation of the high-voltage valve results in large amplitude pulses with very large current and voltage derivatives, with the subsequent stress to system components and high levels of radiated EMI which can cause interference and require special shielding of the converter stations.

Circuit DBS#2, thanks to its distributed choppers, presents a very smooth operation, preventing large voltage or current pulses with large derivatives. As a result, DC currents with a very small ripple are absorbed from the DC link

Table 4.9 Total stored energy for multilevel DBS circuits.

	Multilevel Chopper	Half-Bridge Multilevel	Full-Bridge Multilevel
# of cells per arm	16	20	16
Value of C_{cell} [μF]	145	55	35
Total DBS valve energy [kJ]	2.97	1.4	0.72

for any power level. This minimizes the stress to DC system inductors and also results in a much lower ripple level in the DC link when compared to the other three circuits. In turn, its main drawback would be the requirement for a larger total VA rating of semiconductors than in circuit DBS#1 and also a less compact design due to the cellular structure and the distributed braking resistor.

Circuit DBS#3 presents the advantage of re-using the half-bridge cell topology which can be interesting from an economical and maintenance point of view, since the same resources can be shared for the implementation of both the DBS and the main VSC stations. With respect to DBS#1, the capability of the circuit to control the derivative of the generated voltage pulses is an advantage that helps mitigating EMI problems and reduces the stress in inductive components. However, the lower frequency of operation also results in a larger voltage ripple in the DC link, which is detrimental. An additional drawback is the requirement for a larger number of cells with respect to the other modular topologies, which makes it the topology that presents the highest IGBT VA rating.

Finally, DBS#4 shares a good part of the advantages and disadvantages of DBS#3 such as the capability to control the dv/dt on the positive side, but also the higher DC voltage ripple and the largest total semiconductor VA rating of all four circuits. Concerning the braking resistor, DBS#4 requires of an increased voltage rating in this element, which can also be regarded as problematic. In view of this analysis, this fourth circuit might not look very interesting. However, its main distinctive factor is its capability to generate a valve voltage of either polarity. This could be useful if DBS circuits find applications in LLC based DC grids.

Overall it can be concluded that DBS#2 presents the better balance between number and rating of semiconductors and circuit performance for the HVDC link over-voltage mitigation during a FRT event.

4.4 Summary of the chapter

The study of the four DBS circuits described in Chapter 3 has been performed using computer simulations. The scaling down of the HVDC interconnector and averaged models of the VSC stations has been presented together with an equivalent lumped parameters model for the HVDC cables. The detailed switching models of the four DBS circuits have been tested during a fault ride-through event and the results have validated the correct dimensioning and control strategies proposed in Chapter 3. The results have shown that the four circuits succeed in limiting the DC over-voltage but some differences in terms of performance have been highlighted. The comparison of these differences together with the number and rating of semiconductors and passive components has shown

that the best compromise is obtained with the multilevel chopper circuit.

Chapter 5

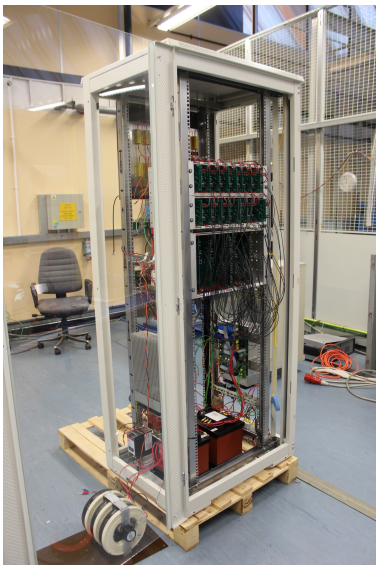
Experimental test platform

A laboratory test platform has been designed and built as a tool to obtain experimental results and to validate the control strategies proposed for each of the DBS circuits investigated in this research work.

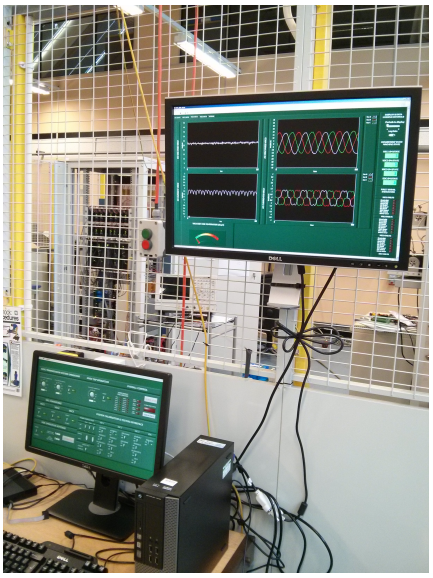
The platform integrates a scaled-down version of a VSC-HVDC connector system plus a reconfigurable converter for the implementation of the four different DBS topologies presented in Chapter 3. A fault emulation mechanism was also included to replicate an AC system fault and recreate the conditions under which a DBS needs to operate while providing fault ride-through capability to the VSC-HVDC connector. A computer based user interface was also implemented which provides remote control over the test platform as well as displaying and logging capability for the signals from all the sensors included in the platform. Fig. 5.1 shows the final laboratory implementation for both the power cubicle and the user interface which integrate the experimental test platform.

5.1 Scaled-down VSC-HVDC system

To emulate the operation environment of a VSC-HVDC connector in offshore wind farm applications, a low-voltage low-power circuit using 2-level 3-phase PWM VSC modules was implemented. The schematic of this scaled-down system is presented in Fig. 5.2. Due to the lack of two independent AC systems in the laboratory, an alternative solution with both VSC stations connected to the same AC system was implemented. In this way, instead of transmitting power between two AC systems, the power is continuously circulated between both VSCs and the AC system only needs to supply the losses. VSC1 operates as the rectifier station, equivalent to the offshore VSC, and VSC2 as the inverter station, equivalent to the onshore VSC. Additionally, a third reconfigurable converter is connected to the DC bus for the implementation of different DBS circuits. The main system parameters are given in Table 5.1.

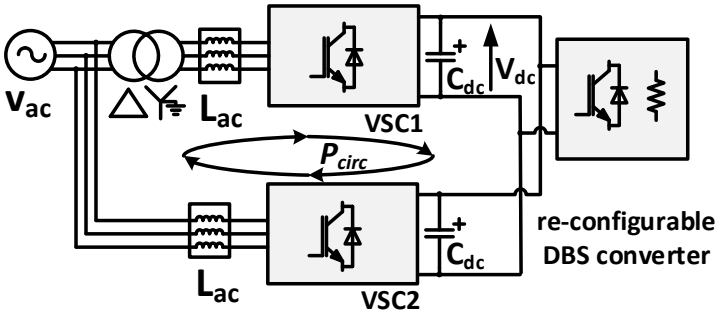


(a) Power cubicle.

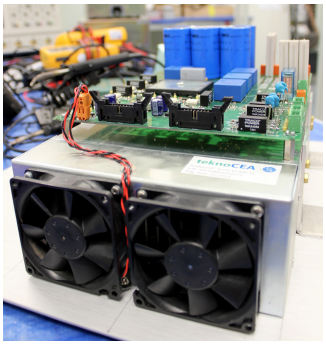


(b) User interface.

Fig. 5.1 Laboratory experimental DBS test platform.



(a)



(b)

Fig. 5.2 (a) Scaled-down model of VSC-HVDC connector and (b) VSC power module.

Table 5.1 Main laboratory test platform parameters.

TEST PLATFORM PARAMETERS		
Parameter	Value	Unit
v_{ac}	220	V
f_{ac}	50	Hz
V_{dc}	400	V
P_n	800	W
Q_n	0	VA
L_{ac}	10.4	mH
C_{dc}	1.02	mF

Table 5.2 Main laboratory test platform components.

TEST PLATFORM COMPONENTS		
Item	Description	Ratings
$T1$	Isolation transformer	1:1, 3.15kVA, 50Hz
$CB1/2/3$	Contactor	3P, NO, 690Vac, 9A, 24Vdc coil
$RPCH$	Pre-charge resistors	3 x 10Ω, 50W
$LAC1/2$	AC inductors	10.4mH, 2A, 50Hz
$PS2$	Power supply	24V, 240W
$SSR1/2$	Contactor	3P, NO, 690Vac, 9A, 24Vdc coil
$RF1$	Fault resistors	3 x 10kΩ, 10W
$RH1$	Fault rheostat	3 x 0-100Ω, 1.5kW
$VSC1/2$	Voltage-source converter	$400V_{ac}$, $800V_{dc}$, 10kVA, 20kHz
$BATT1/2$	Lead-acid battery	12 V, 12Ah
$LUMPED R$	Lumped braking resistor	141/188/235 Ω, in 47Ω segments
$DISTRIB R$	Distributed braking resistor	16 x 22Ω, 100W

Fig. 5.3 shows the detailed electrical diagram of the test platform. A description of the displayed elements is included in Table 5.2.

5.1.1 Isolation transformer

As studied in [97], when two VSC converters are connected in parallel, as it is the case in the test platform, there is a risk of a zero-sequence circulating current to loop around both converters. In order to avoid this problem, an isolation transformer was added to the AC terminals of VSC1 in order to break the path for these circulating currents to flow, avoiding the problem.

5.1.2 DC link pre-charge circuit

A pre-charge circuit for the DC system capacitance was included in the AC terminals of VSC1. During the pre-charge sequence, CB1 and CB2 are open and both VSC1 and VSC2 are blocked. CB3 is then closed and the DC capacitance will charge through resistors RPCH and the diodes in VSC1, which form a 3-phase uncontrolled rectifier. Once the pre-charge sequence is finished and the DC bus has reached the required voltage, CB2 closes and CB3 opens. The controllers of VSC1 and VSC2 are then de-blocked and VSC2 brings the DC voltage up to the nominal value before the power transmission starts.

5.1.3 Fault emulation circuit

The fault emulation mechanism was implemented with contactors SSR1 and SSR2, resistors RF1 and rheostat RH1, connected to the AC terminals of VSC2.

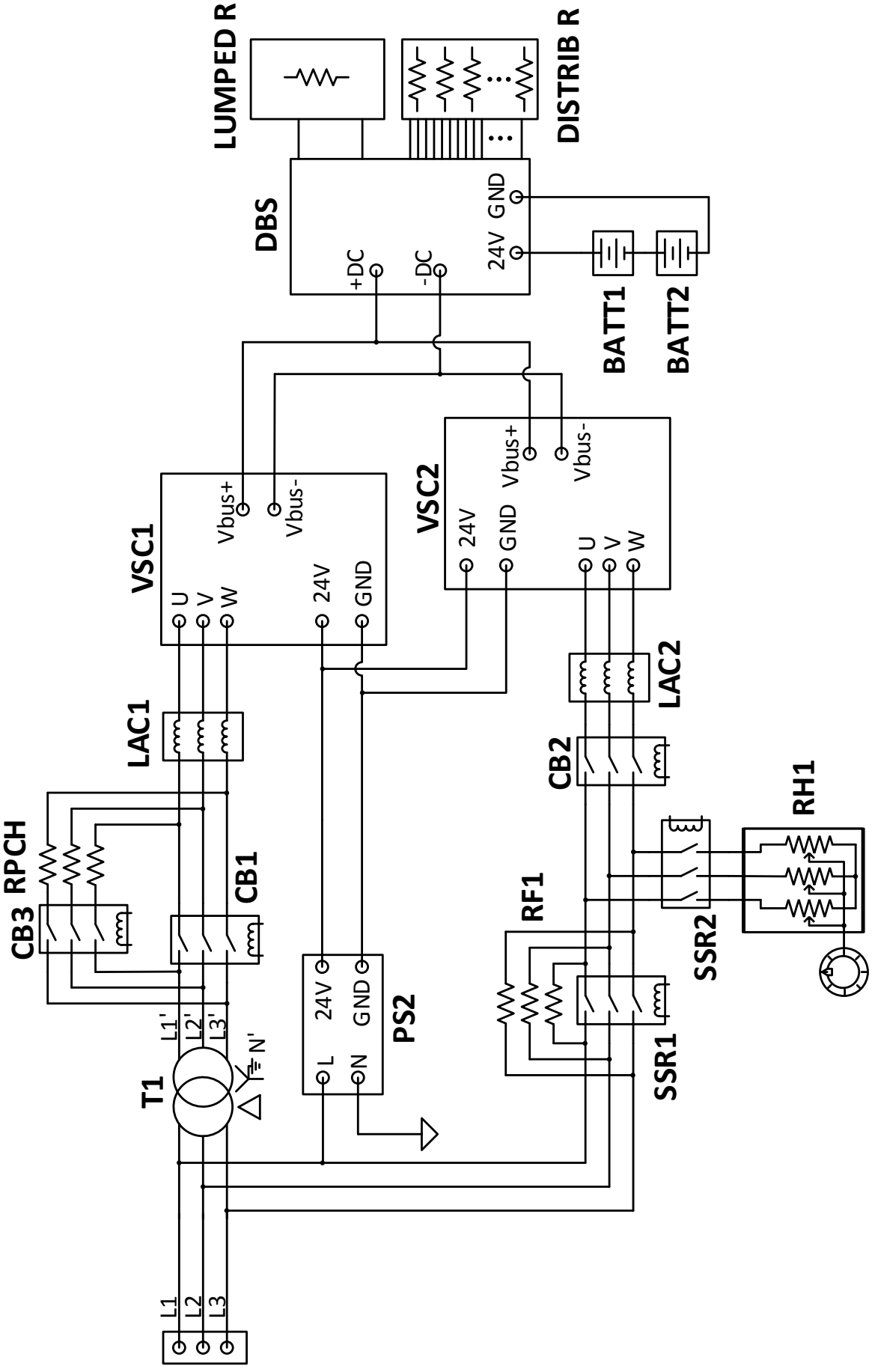


Fig. 5.3 Detailed laboratory test platform electrical diagram.

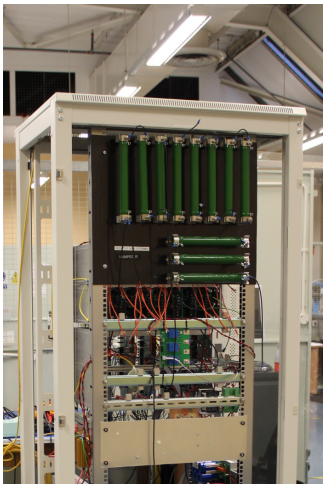
The fault triggering process is later explained in section 5.1.7.

5.1.4 Voltage source converter modules

Fig. 5.2b shows the VSC power module used for the implementation of each VSC station. It integrates a 3-phase IGBT bridge module with anti-parallel diodes mounted on a heat sink and a printed circuit board containing voltage and current sensors on both AC and DC sides. The board also integrates the gate drivers for the 6 IGBTs and the DC bus capacitors, whose value was specified in Table 5.1. The ratings for the module are presented in Table 5.2.

5.1.5 Braking resistors

In order to test the four different DBS circuits studied in this work, a lumped resistive element (LUMPED R) and the distributed resistive elements (DISTRIB R), as presented in Chapter 3, were included in the platform. The values for these resistive elements are specified in Table 5.2. A panel containing individual resistors whose series connection can be reconfigured was used to build the lumped resistive element (Fig. 5.4a). For the distributed elements, single resistors were mounted on a panel, with the capability of individually connecting them to each cell (Fig. 5.4b).



(a) Lumped braking resistor.

(b) Distributed braking resistors.

Fig. 5.4 Braking resistors used in the test platform.

5.1.6 DC voltage supplies

All the electronic circuits inside both VSCs and reconfigurable DBS were designed to be supplied with $24V_{dc}$. PS2 is an AC/DC converter used to supply the

electronics in the VSCs, plus all the control boards presented later in section 5.3. For the supply of the electronics in the power cells utilized in the reconfigurable DBS two 12 V batteries, BATT1 and BATT2, were used. The use of batteries was necessary to minimize the capacitance from each power cell to earth, since this creates a path for current to flow from the DC bus poles to earth which can potentially charge the cells in the DBS multilevel topologies. This could derive in a cell over-voltage situation if the magnitude of this current is large enough. In a real VSC-HVDC scheme, since all the electronics inside a cell is directly supplied from the local capacitor, this effect should not be a concern.

5.1.7 Fault triggering mechanism

The fault ride-through characteristics as specified in different grid codes were presented in Chapter 2. They were also used for simulation in Chapter 4 as a way to exercise the DBS circuits over the whole operation range, from zero to nominal power dissipation. In order to replicate the ramped voltage recovery from these characteristics in the test platform, an electronic power supply connected to the terminals of VSC2, which operates as the onshore rectifier station, could be used. This is however an expensive piece of equipment, so an alternative simple method to emulate AC system faults is proposed here by using the combination of contactors and resistors that was presented in Fig. 5.3.

Starting with the system transmitting power from VSC1 to VSC2 during steady state operation, a fault is triggered using the following sequence:

1. SSR1 opens, inserting the high impedance RF1 between the AC system and the terminals of converter VSC2. CB2 stays always closed during the system operation.
2. A pre-determined time delay is applied to ensure the terminals of SSR1 are open before commutating SSR2.
3. SSR2 closes, connecting the low impedance RH1 to the terminals of VSC2.
4. SSR2 is kept closed for a time equal to the desired fault duration.
5. SSR2 opens.
6. A pre-determined time delay is applied to ensure the terminals of SSR2 are open before commutating SSR1.
7. SSR1 closes, reconnecting VSC2 terminals to the AC system.

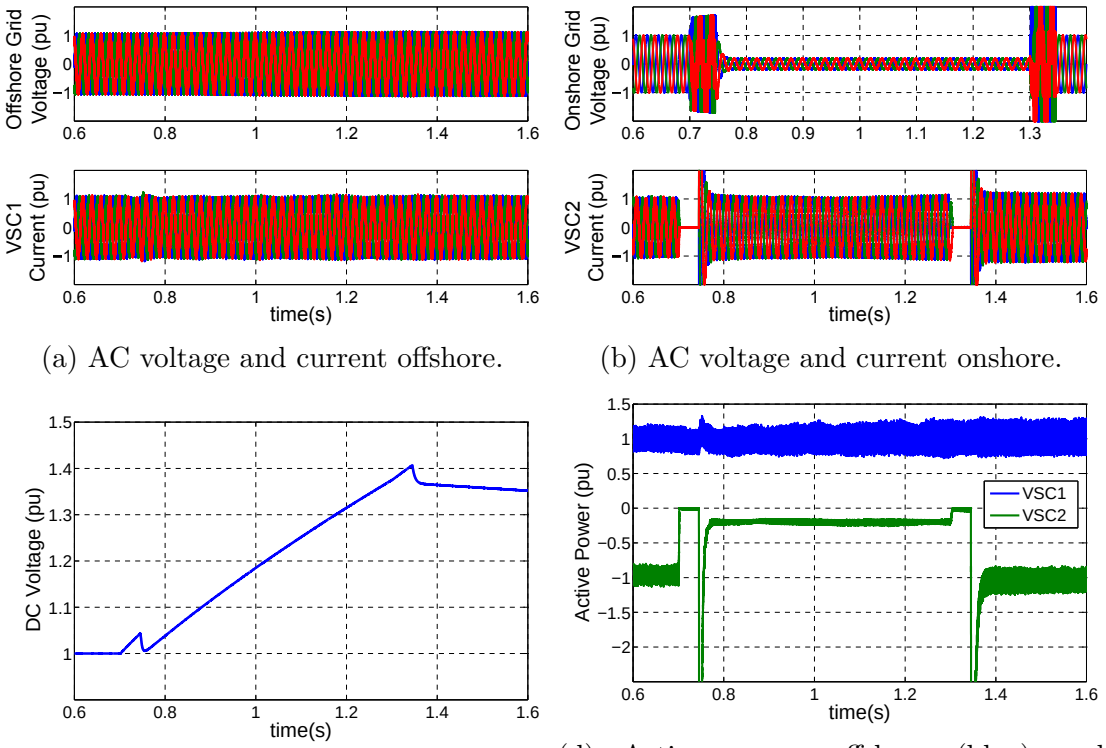
With this mechanism, by adjusting the impedance of the rheostat RH1, faults of different severity are emulated. This allows to test the DBS operation at different levels of power dissipation.

Fig. 5.5 shows the simulation results for the operation of the fault triggering mechanism. A fault is applied at time 0.7 s for a duration of 0.6 s. A delay of 45 ms is used between the operation of the breakers to account for mechanical delays, as previously explained. While no changes are observed in the grid voltage and current for the rectifier station VSC1 in Fig. 5.5a, Fig. 5.5b shows how at time 0.7 s, with the connection of high impedance RF1, the terminals of the inverter station, VSC2, are left in open circuit and the AC current drops to zero. The effect can also be observed in the active power at the AC terminals of VSC2, as shown in Fig. 5.5d, which collapses from -1 pu to 0 pu instantaneously. The situation is maintained for the pre-established delay of 45 ms, after which SSR2 is energised, connecting the low impedance RH1 to the terminals of VSC2. At this time, current starts flowing from VSC2 into impedance RH1, and VSC2 goes into over-current mode. In this case, since the impedance of rheostat RH1 is not set to zero ohms, a voltage appears across it, as observed in Fig. 5.5b and VSC2 is capable of evacuating around 0.2 pu active power as shown in Fig. 5.5d, while VSC1 continues injecting 1 pu power into the DC link. This creates a power unbalance which makes the excess power to be stored in the DC system capacitance, with the subsequent DC voltage increase, as observed in Fig. 5.5c. At time 1.3 s SSR2 is de-energised, and the terminals of VSC2 are again left in open-circuit. After the 45 ms delay, SSR1 is re-energised, reconnecting VSC2 to the AC system and bringing the fault emulation to an end. The power evacuation capability of VSC2 is then restored and the DC voltage starts decreasing. VSC2 control board is in charge of generating the signals to drive SSR1 and SSR2 based on the fault duration command received from the user interface.

In a real HVDC transmission system, when a fault on the AC grid occurs, the terminals of the VSC station are not left in open-circuit as it is the case with the method proposed here for the reduced scale test rig. This leads to the disturbance of the onshore VSC converter operation in the test rig at the instants right after the operation of relays SSR1 and SSR2. Some of the effects can be appreciated when looking at the VSC2 AC current and active power overshoots (Figs. 5.5b and 5.5d) after the closing of SSR2 and SSR1. Some additional disturbances will be seen in the experimental results presented in Chapter 6.

5.2 Reconfigurable DBS power cells

In order to be able to implement the different DBS circuits in the test platform with minimal effort, a flexible power cell printed circuit board (PCB) has been designed. Later, sixteen of these flexible power cells were manufactured to serve as building blocks for the modular DBS topologies. The electrical diagram of this flexible power cell or power module is shown in Fig. 5.6. As seen in the



(a) AC voltage and current offshore.

(b) AC voltage and current onshore.

(c) HVDC link voltage.

(d) Active power offshore (blue) and onshore (green).

Fig. 5.5 Simulation results for the fault emulation mechanism.

figure, screw terminal connectors (SW1 to SW6) were included to allow changing the internal cell components electrical connections. By appropriately setting these connections, all the four DBS circuits presented in Chapter 3 can be implemented, as displayed in Fig. 5.7.

The required connections are indicated with blue wires and the resulting current path in the cell is indicated by the brown highlighted tracks. The values of the main components of the cell power circuit are presented in Table 5.3.

Once the electrical connections to configure each cell are made, the external connections are also made to build the desired DBS circuit and connect it across the DC bus. In Fig. 5.8, the different cell arrangements are displayed. In the case of the multilevel chopper, shown in Fig. 5.8a, only one power cell is used, since the voltage rating of MOSFET T5 is sufficient to withstand the full DC link

Table 5.3 Flexible power cell main components.

Part	Description
T1..T4	N-channel MOSFET, 100V, 144A, 5.5mΩ, FDP054N10
T5	N-channel SiC MOSFET, 1.2kV, 40A, 80mΩ, SCT2080KEC
C_{dc}	electrolytic capacitors, 220μF, 100V each
Current sensor	LEM CAS 6-NP, 6A

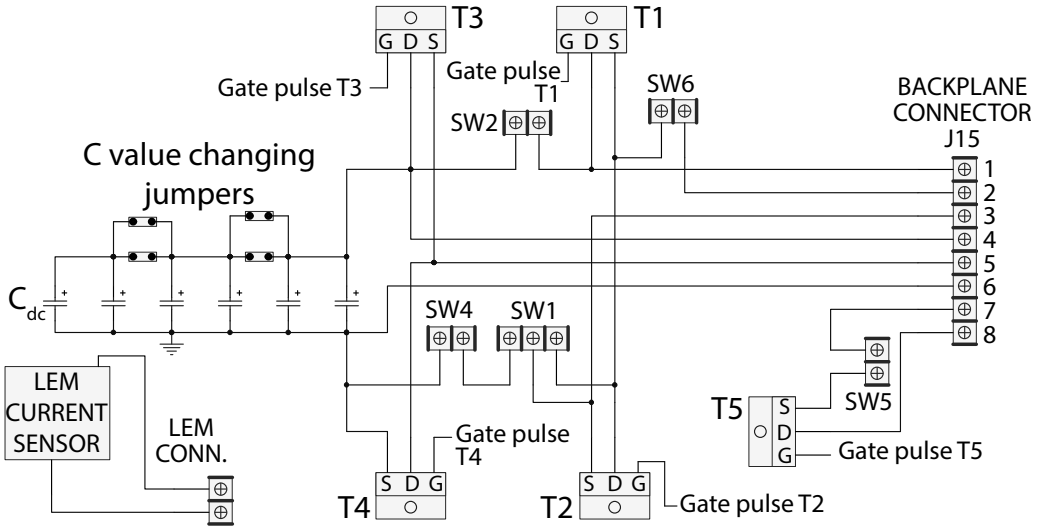


Fig. 5.6 Power circuit diagram of the flexible power cell.

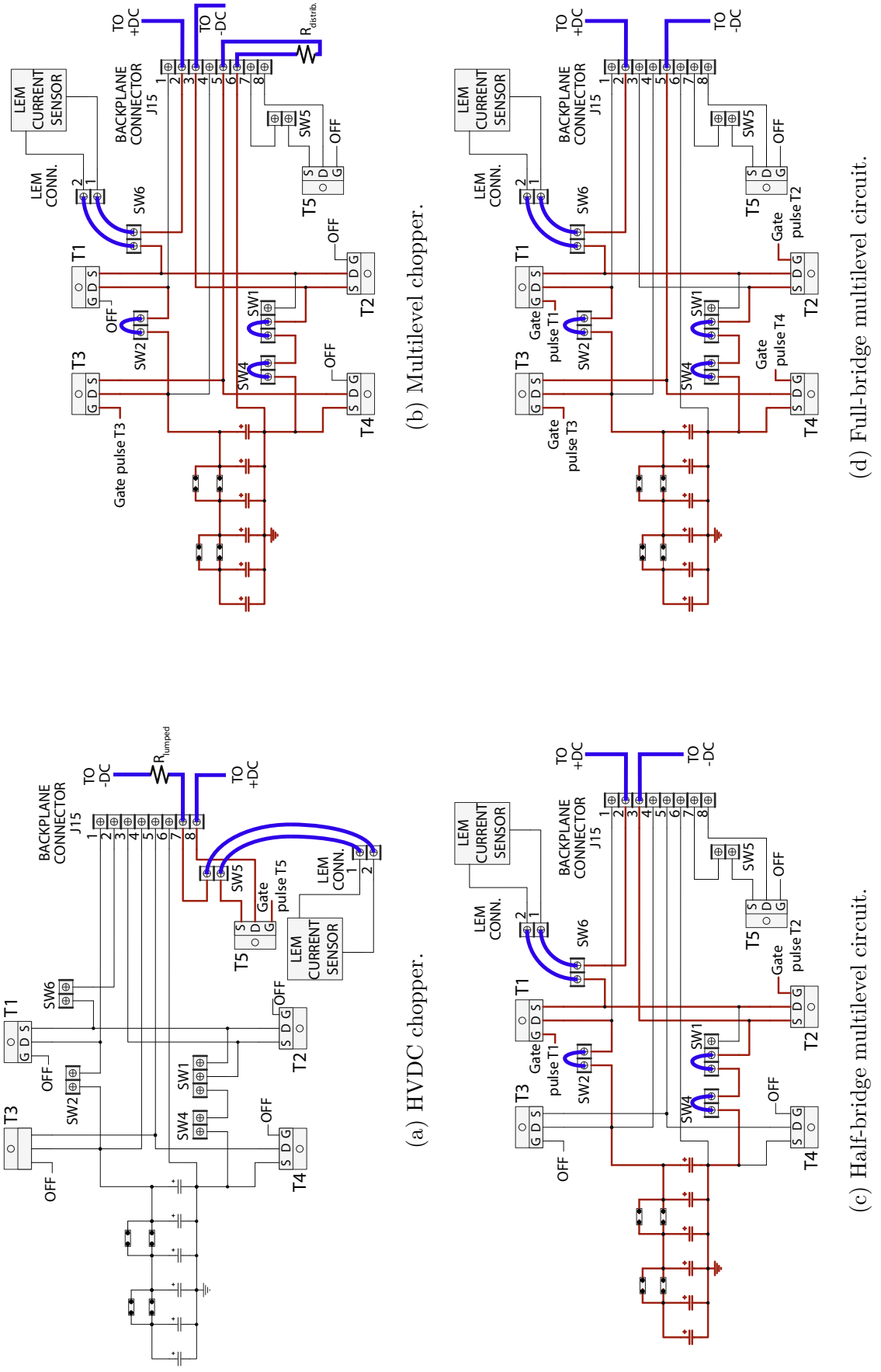
voltage. For the three multilevel topologies however, the sixteen power cells are used as shown in Figs. 5.8b, 5.8c and 5.8d in order to obtain a good resolution in the number of steps generated by the DBS circuit during testing.

In addition to the power circuit, the cell includes the control electronics, with an FPGA as the core of the system. It also includes gate drivers for each of the MOSFETS, 3 analog-to-digital (ADC) converters to measure the cell current, the cell capacitor voltage and the voltage across the distributed braking resistor in case it is present. A fibre optics receiver and transmitter enable communication between the power cell and the DBS converter control board. The detailed schematic for the complete power cell board is included in appendix B. Fig. 5.9 shows one finalised power cell and Fig. 5.10 shows the power cell organization in the DBS converter rack.

5.3 Control boards and user interface

In order to control each converter in the platform and to manage the operation of the complete system during testing, a set of dedicated control boards was designed and built. A computer based user interface was also implemented using the LabVIEW software package.

A communication network based on fibre optics and using custom protocols was also built, which in addition provides the required electrical isolation between the different converters and the control system. Ethernet was used for data transfer between the test platform and the computer running the user interface. FPGAs were used as programmable devices for the implementation of the control algorithms and to manage all the communications.



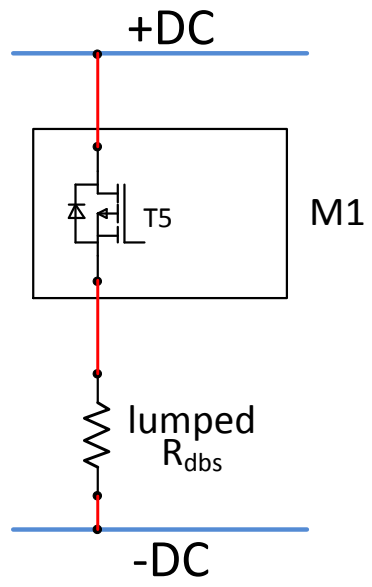
(a) HVDC chopper.

(b) Multilevel chopper.

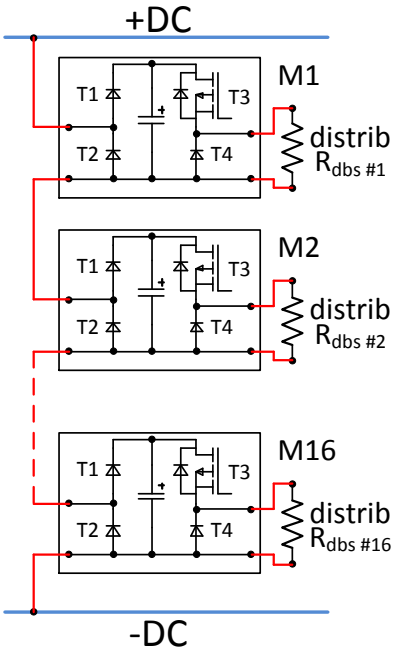
(c) Half-bridge multilevel circuit.

(d) Full-bridge multilevel circuit.

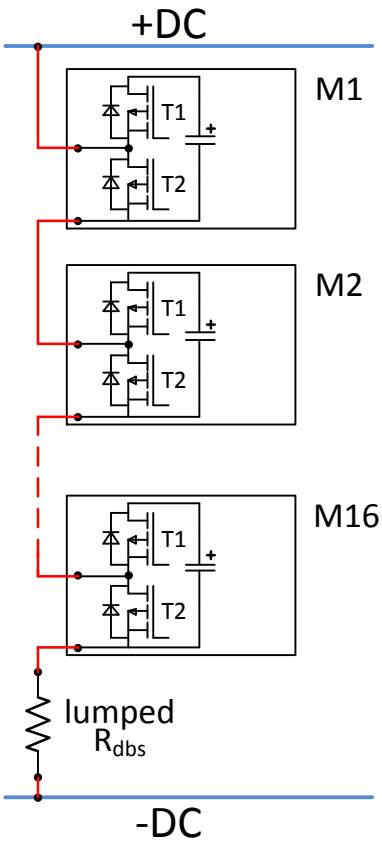
Fig. 5.7 Screw terminal connections in the flexible power cell for the different DBS configurations.



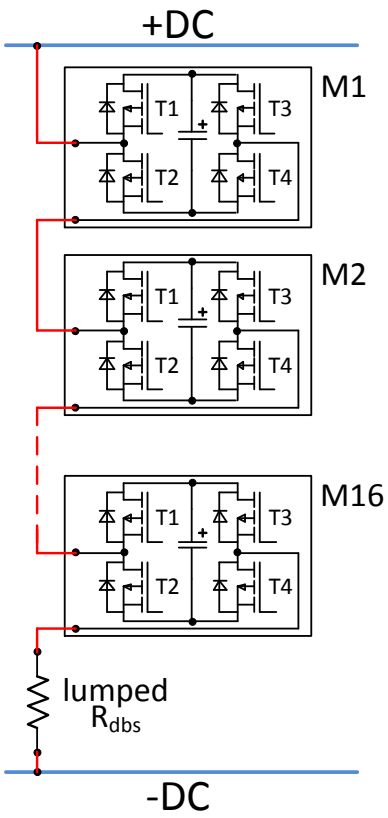
(a) HVDC chopper.



(b) Multilevel chopper.



(c) Half-bridge multilevel circuit.



(d) Full-bridge multilevel circuit.

Fig. 5.8 Configuration of the power cells to build the four DBS circuits.

(a) Front view. (b) Back view.

Fig. 5.9 Flexible power cell.

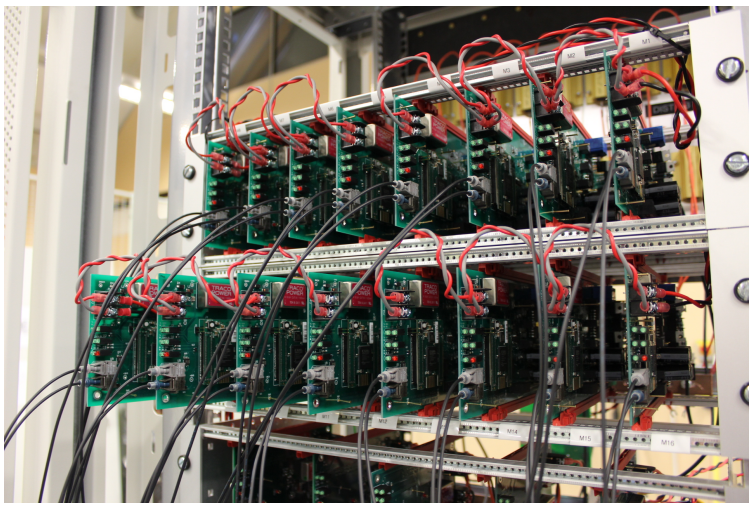


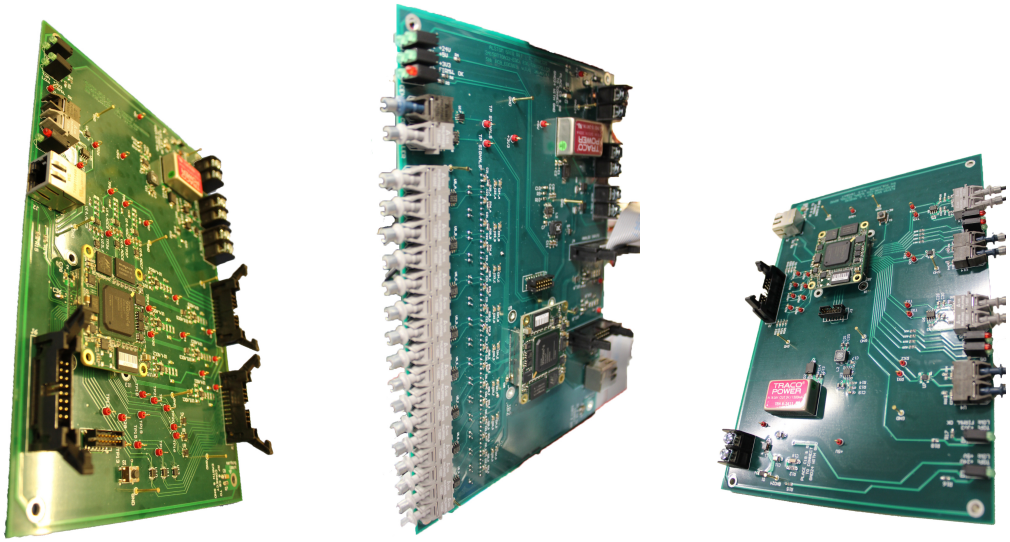
Fig. 5.10 Modular arrangement of the DBS power cells for the DBS circuits implementation.

5.3.1 Control boards

Three different control boards were designed for the test platform. These are:

- VSC controller
- DBS controller
- Global controller

Each control board includes a programmable Xilinx FPGA. This device manages the operation of all the electronics in the board plus the communications, and it is programmed using Verilog-HDL (hardware description language). In the particular case of the converter control loops, these are first tested in simulation in the Matlab-Simulink environment. Later, HDL code is automatically generated from the Simulink block diagrams using Xilinx's System Generator tool. This automatically generated code is then merged with the manually developed code to create the complete firmware to program the FPGAs. Fig. 5.11 shows the finished control boards.



(a) VSC controller. (b) DBS controller. (c) Global controller.

Fig. 5.11 Different control boards in the test platform.

Two units of the VSC control board, shown in Fig. 5.11a, are used in the platform, one for each VSC. They implement the vector control to manage the operation of the HVDC transmission system. VSC1 regulates the active power transfer while VSC2 regulates the DC voltage. The electrical interface between the control board and the VSC module is implemented via two 16-pin IDC connectors (black connectors in the back of the board). One fibre optics link, transmitter and receiver, is also included to allow communication with the global controller.

The DBS control board, shown in Fig. 5.11b, implements the control algorithms presented in Chapter 3 for the operation of the different DBS circuits. 16 fibre optics links (transmitter and receiver) are included for the communication with each of the power cells. An additional fibre optics link is available for communication with the global controller.

The global controller, Fig. 5.11c, is the central node of the communication network. It sends and receives data from all the control boards. It includes four fibre optics links (receivers and transmitters) for interconnection with one DBS control board and with up to three VSC control boards. It also contains an Ethernet transceiver for communication with the computer where the user interface is running. Detailed schematics for each of the three control boards are included in appendix B.

5.3.2 Communication network

Fig. 5.12 presents the diagram of the communication network in the test platform. The communication interfaces included in each board were explained in the previous point. The network transmits commands from the user interface in the PC to the relevant control boards. It also sends the firing pulses from the DBS controller to the semiconductors inside each power cell and from the VSC controllers to the VSC converters. On the opposite direction, this is from the converters to the user interface, the date gathered in the different sensors is first transmitted to the controller boards to be used by the control algorithms and also transmitted back to the user interface in the computer for displaying and logging purposes. A global fault management structure is also implemented in the control boards, so that in case a fault is detected in any of the converters, a fault flag is passed to all the other control boards to halt the system operation. There are three different communication interfaces:

- Electrical interface: using copper cable between the VSCs and controllers. No communication protocol needed.
- Fibre optics interface: between DBS power cells and controller; between the VSC and DBS controller boards and the global controller board. A custom communication protocol is implemented.
- Gigabit Ethernet interface: between the global controller and the computer running the user interface. UDP is used as the communication protocol.

Fig. 5.13 shows both the fibre optics and Ethernet interfaces as implemented in the laboratory. A description of each of the data packets used in the platform is included in appendix C. The signals from the sensors in the platform are

digitized using the ADCs inside the power cells and the control boards. Once in digital format, the signals are grouped in data packets to be sent through the communication network.

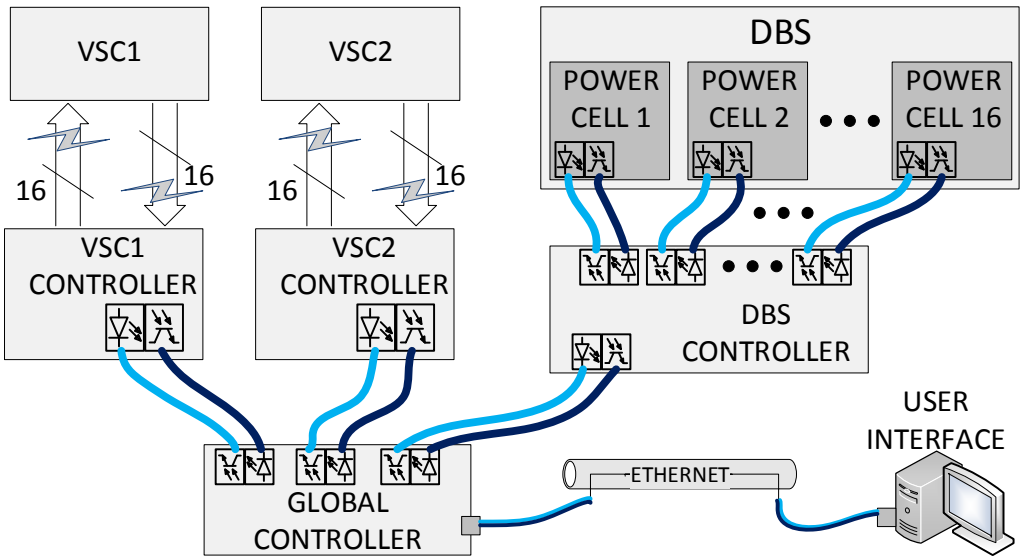


Fig. 5.12 Test platform communication network detail.

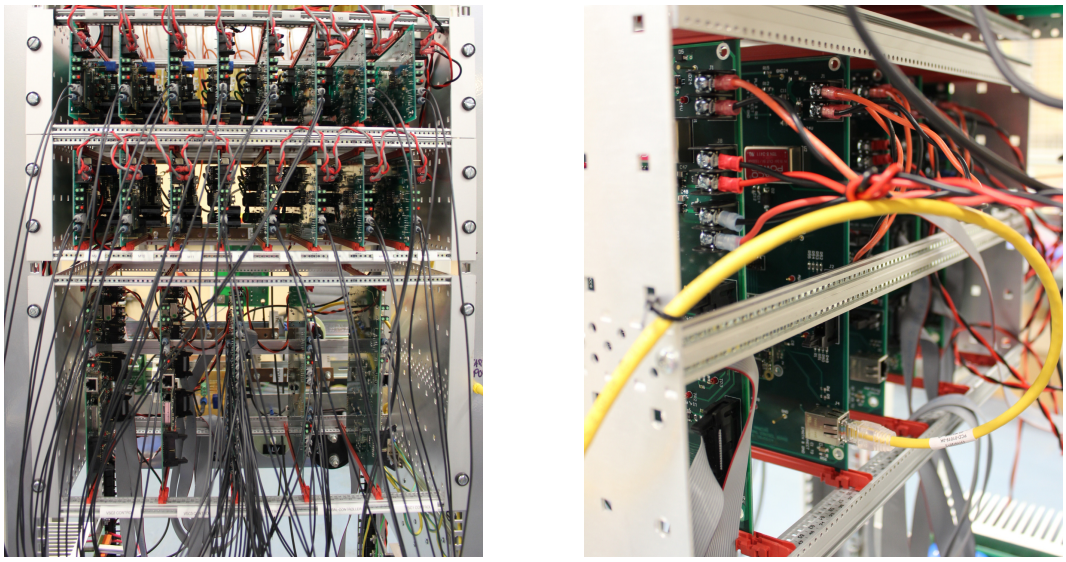
As mentioned, all the data gathered in the different sensors is collected and sent back to the computer. Table 5.4 lists all the measurements performed in the test platform.

Data sampling and transmission rates

Table 5.4 also shows on the right column the resolution and sampling frequency for each digitized measured signals. The controller boards provide data to the control algorithms at the sampling rates shown in the table. Each of the control boards, in addition, re-samples the data at 4 kHz for transmission to the global control board, and back to the computer. Based on this, the required transmission bandwidths for different sections of the communication network are calculated and presented in Table 5.5. The two external sensor boards needed for the DBS converter operation are displayed in Fig. 5.14. The output of these two sensors is sent to the ADCs in the DBS control board to be digitized.

5.3.3 User interface

The two screens for the user interface developed using LabVIEW are shown in Fig. 5.15. Fig. 5.15a shows the control panel from which the user can give the commands to manage the operation of the different converters in the platform. There are several subsections in the panel:



(a) Fibre optics. (b) Ethernet.

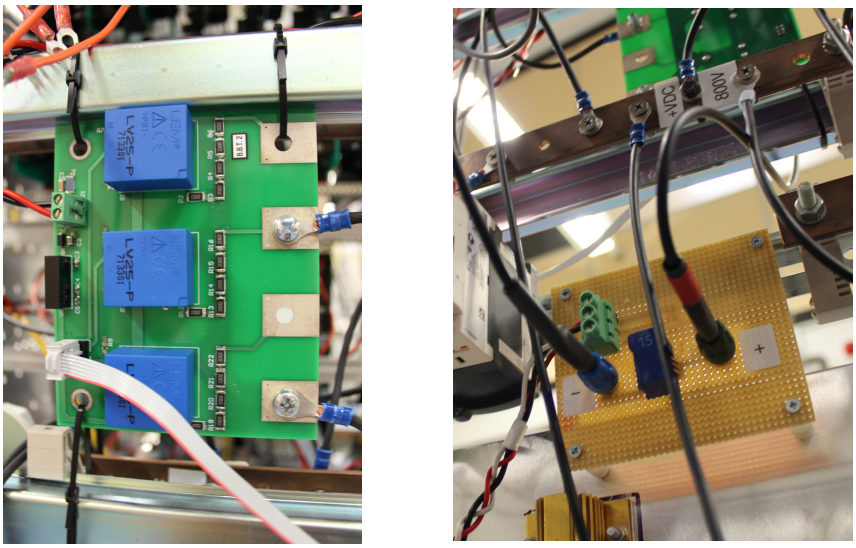
Fig. 5.13 View of the different communication interfaces.

Table 5.4 Laboratory test platform measurements detail.

VSC1 and VSC2 (each containing)		
Measurement	Sensor	Digitized signal
3x AC voltages	R divider + ACPL-C79B chip	16-bit (@ 30.3kHz)
3x AC currents	LEM LA 25-NP	16-bit (@ 30.3kHz)
1x DC voltage	R divider + ACPL-C87B chip	16-bit (@ 30.3kHz)
1x DC current	LEM LA 25-NP	16-bit (@ 30.3kHz)
1x IGBT module temp.	Module internal PTC	16-bit (@ 30.3kHz)
DBS power cells (each containing)		
Measurement	Sensor	Digitized signal
1x capacitor voltage	R divider	12-bit (@ 16kHz)
1x distributed R voltage	R divider	12-bit (@ 16kHz)
1x cell current	LEM CAS 6-NP	12-bit (@ 16kHz)
DBS - External		
Measurement	Sensor	Digitized signal
1x DC bus voltage	LEM LV 25-P	16-bit (@ 30.3kHz)
1x DBS current	LEM CAS 15-NP	16-bit (@ 30.3kHz)

Table 5.5 Data transmission bandwidths in the communication network.

From	To	Interface	Bandwidth
VSC controller	Global controller	Fibre	562.5 kbps
DBS power cell	DBS controller	Fibre	562.5 kbps
DBS controller	Global controller	Fibre	2.2 Mbps
Global controller	PC	Ethernet	3.3 Mbps



(a) DC bus voltage sensor. (b) DBS current sensor.

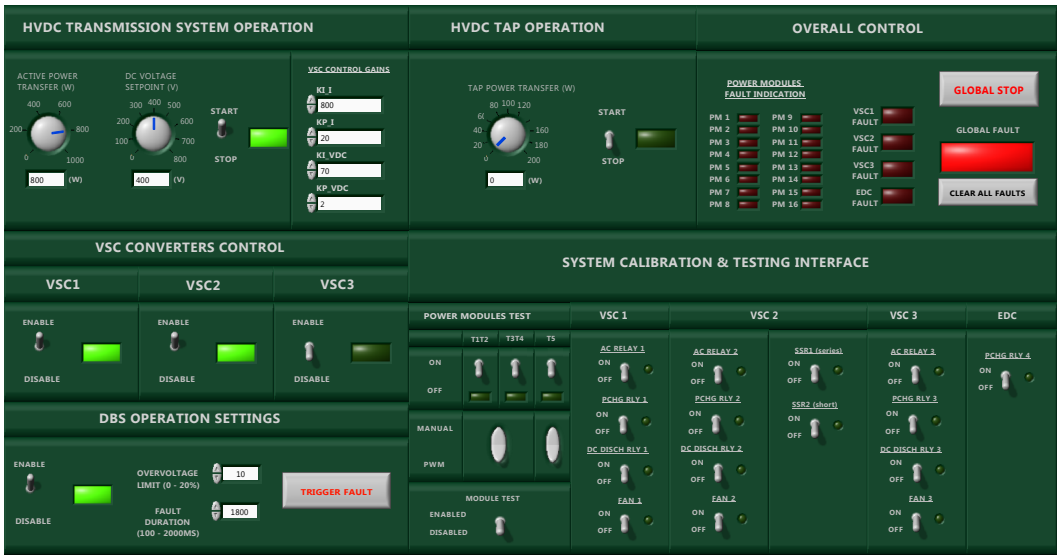
Fig. 5.14 External sensor boards in the DBS converter.

- **HVDC transmission system operation:** In this section the user can set the DC voltage and active power demand for the HVDC equivalent system. The proportional and integral gains for both active power and DC voltage regulators in VSC1 and VSC2 can be defined and the start/stop of the converters can also be controlled. When the user moves the switch to the start position, VSC1 and VSC2 start executing the start-up sequence to pre-charge the DC link voltage, bring the voltage up to the specified set point and start transmitting the required active power.

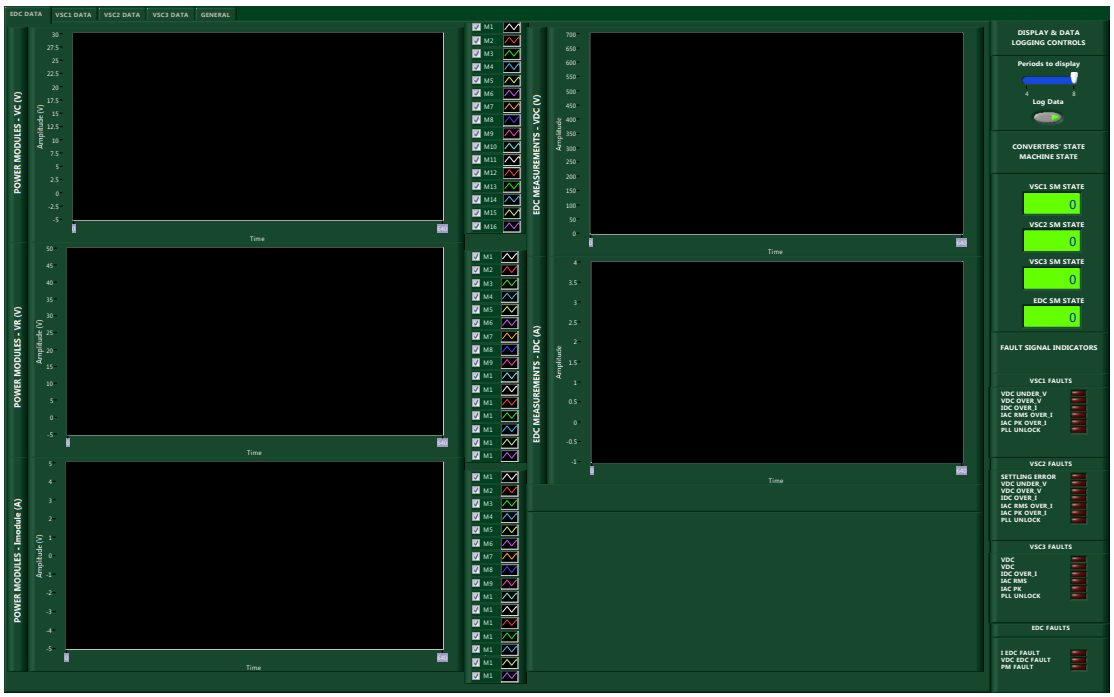
- **VSC converters control:** Here the operation of each VSC can be enabled/disabled by manipulating the provided switches. If a VSC converter is disabled it does not respond to the commands sent from other sections in the control panel.

- **DBS operation settings:** This section contains the controls for the DBS converters operation. The operation of the DBS converter can be enabled/disabled and the allowed over-voltage limit can be set. The fault duration value can be specified in milliseconds, from zero up to two seconds. A button is also provided for the user to trigger the AC fault event in the terminals of VSC2.

- **Overall control:** Here the user receives the feedback on the faults that may occur in the test platform. In the event of a fault, an LED indicates its origin, showing in which converter or in which power cell the fault occurred. The test platform implements a locking mechanisms where each controller board goes into a blocked state when a fault is detected. In order to restart



(a) Control panel window.



(b) Scopes and data logging window.

Fig. 5.15 User interface implemented in LabVIEW.

operation the user needs to manually reset the system using the *"CLEAR ALL FAULTS"* button. An additional button to stop the operation of the whole user interface is also available here.

- **System calibration & testing interface:** This section is added for debugging purposes during the platform commissioning or in case malfunction of any component is suspected. It allows the user to manually control all the relays in the test platform and to send firing pulses to the MOSFET switches inside each of the power cells.

Fig. 5.15b on the other hand shows the data display and data logging window which includes scopes to display in real-time all the data captured by the test platform sensors presented in Table 5.4, which as already mentioned, has been re-sampled at 4 kHz while keeping the same bit resolution specified in the table. As observed, several tabs are provided on the top-left part of the screen which allow the user to display the scopes related to either the DBS or each VSC converters. On the right hand side of the window, section *"Display & data logging controls"* allows the user to choose when to start logging the data from all the scopes into the PC's hard drive, and also select the number of fundamental frequency (50 Hz) periods to be displayed in the scopes. Just below, the *"Converters' state machine state"* section, shows the current state of the state machine implemented inside each control board to sequence the operation of each converter and it is useful to detect potential problems during the platform's power-up or power-down events. Last, the right-bottom area of the screen is dedicated to provide additional information to the user concerning a fault event in the VSC or the DBS converters. LED's are used to display which of the considered fault conditions, for example over-currents or over-voltages was detected by the control board of the relevant converter.

5.4 Summary of the chapter

A flexible laboratory test platform has been designed and built to validate the control strategies for each DBS circuit proposed in this research work. The test platform integrates a scaled down model of a VSC-HVDC connector system, plus a reconfigurable DBS converter, which by making use of a flexible power cell design allows building each of the four DBS circuits presented in Chapter 3. A user interface to manage the operation of the platform during the tests has been developed and implemented using a PC. A communication network to permit data exchange between all the control boards in the platform has also been integrated. The chapter has presented the details of the design and implementation of each of the hardware and software parts required for building

and operating the experimental test platform. Additional information concerning the platform design has been included in appendices B and C.

Chapter 6

Experimental evaluation of DBS circuits

In Chapter 5 the platform built to carry out the experimental studies was explained. In this chapter, the results of these experimental studies are presented. The main aim is to prove the validity of the control systems developed for each of the four DBS circuits.

6.1 Test platform configuration for the tests

The test platform diagram described in Chapter 5 is shown in Fig. 6.1. The set of parameters to configure the test platform and DBS operation for the tests is displayed in Table 6.1. An autotransformer is used between the laboratory 3-phase 400 V AC power supply and the AC input to the platform in order to provide the required 400V/220V reduction. The controller gains that have been used in the experimental platform for the VSC stations are displayed in Table 6.2 and for the DBS converters in Table 6.3.

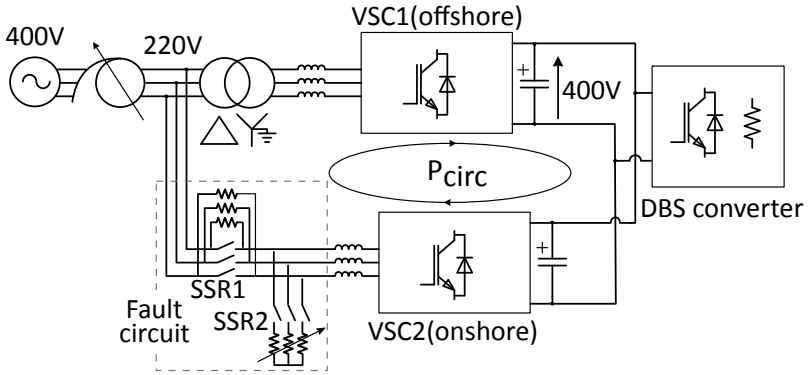


Fig. 6.1 Reminder of the experimental test platform diagram.

In Fig. 6.2 the operation of both VSC stations during quasi steady-state power transmission is shown, which validates the correct operation of the HVDC

Table 6.1 Test platform set-up parameters for the tests.

GENERIC TEST PARAMETERS	
V_{ac}	220 V
V_{DCn}	400 V
P_{DCn}	800W
$UOVL$	1.1 pu
$LOVL$	1.05 pu
T_{fault}	1.8s
T_{delay}	15 ms

Table 6.2 PI controller gains for the VSC stations in the test platform.

VSC controller gains			
DC link voltage PI		AC current PI	
k_p	0.05	k_p	22
k_i	2	k_i	3850

inter-connector in normal (non-faulted) mode. The distortion in the AC current is due to insufficient filtering of the harmonics introduced by the pulse width modulation of the VSC converter AC voltage. However this does not affect the DBS functionality being tested. The start-up sequence, as described in Chapter 5, is observed during the first 4 seconds of operation.

The DC bus is pre-charged through VSC1, and once the threshold voltage is reached, VSC2 is de-blocked to bring the DC voltage to 1 pu (400 V). Initially, VSC1 controls the transmitted power to 1 pu and later the power demand is reduced in steps to test the power regulation. It is observed how both VSC stations achieve the correct regulation of both active power and DC voltage parameters respectively.

Regarding the fault circuit operation, as presented in Table 6.1, a fault duration (T_{fault}) of 1.8 s is set as a standard for all tests. This is the maximum

Table 6.3 P and PI controller gains for DBS converters in the test platform.

DBS converter controller gains				
	DBS#1	DBS#2	DBS#3	DBS#4
V_{DC} open loop controller gain				
k_p	20	320	20	20
Valve energy controller gains				
k_p	-	-	5e-4	2e-4
k_i	-	-	1e-4	9e-5

operation time expected from the DBS in the Dolwin 3 offshore wind farm interconnection project specification, and therefore it has been adopted here. The time delay between contactor operations to avoid short-circuiting of the AC supply is set to 15 ms. In Fig. 6.3 the experimental results for a fault event triggered in the platform using a fault impedance of zero ohms and with no DBS in operation are presented.

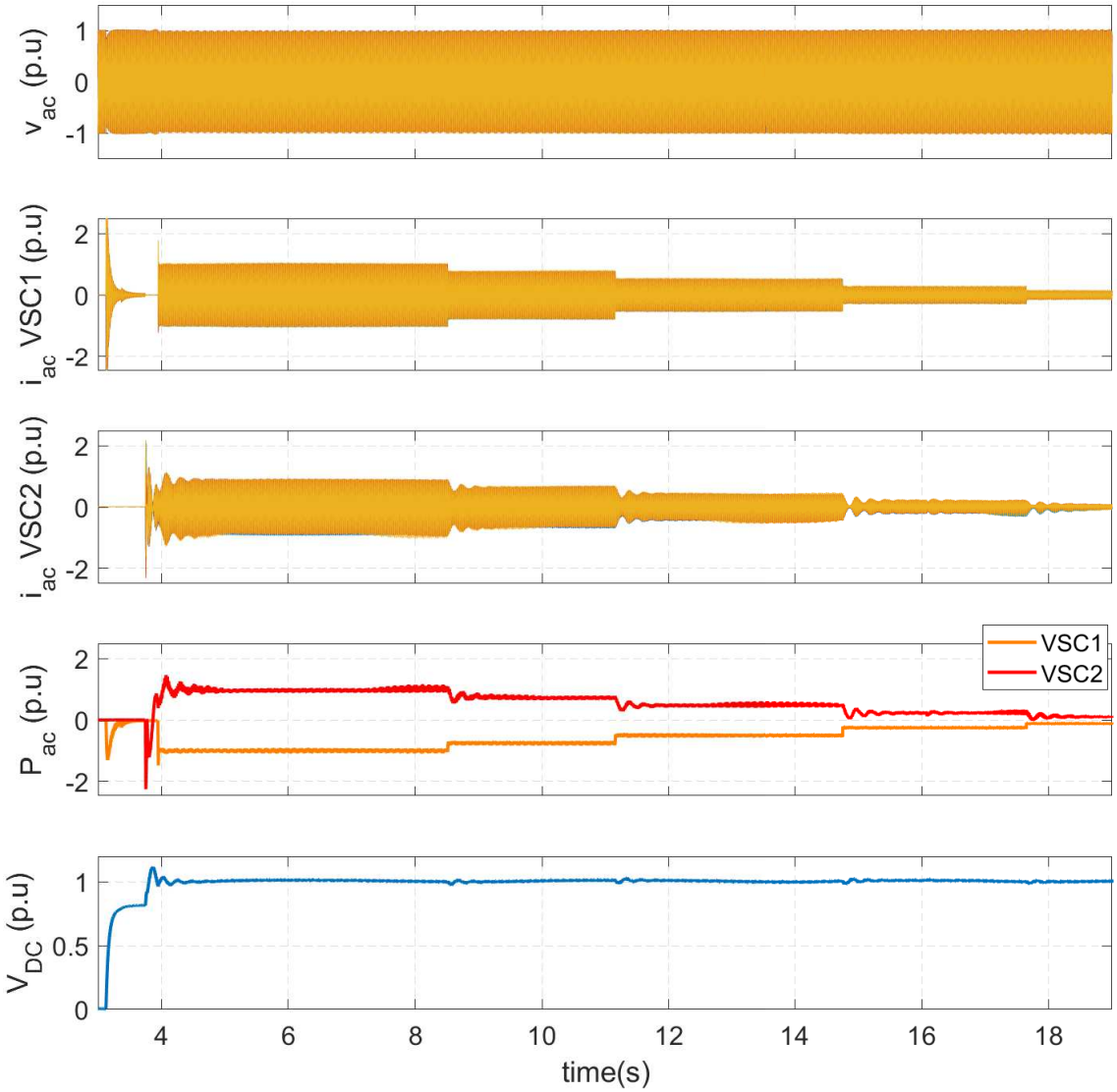


Fig. 6.2 Start-up sequence and power demand variation in the test platform.

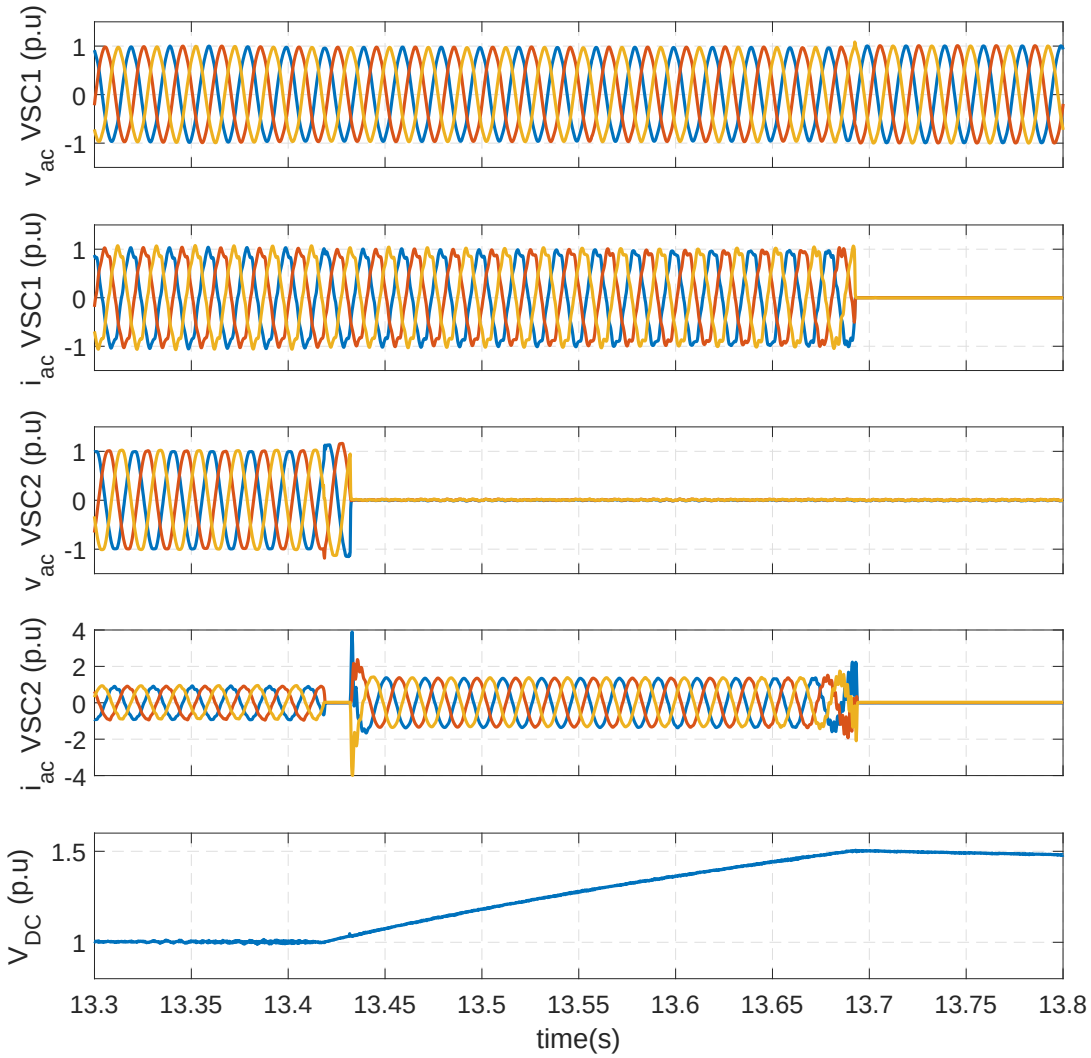


Fig. 6.3 AC fault in the test platform with DBS disabled.

Initially the system is in quasi steady-state circulating the nominal power. At time 13.42 s the fault is triggered. As explained in section 5.1.7, during the predefined delay, in this case 15 ms, the de-energisation of relay SSR1 leaves the terminals of VSC2 in open circuit, which is corroborated by the drop of AC current in VSC2 to zero. After this delay, relay SSR2 is closed connecting the fault impedance, in the case of the figure set to a zero ohms value, which causes a solid short-circuit on the VSC2 terminals. This causes the AC voltage to collapse to zero and VSC2 to lose all active power injection capability. The station's current controller goes into current limit mode which is set to limit the AC current to 1.4 pu. Meanwhile VSC1 station continues injecting 1 pu active power into the DC system, with all the resulting energy being stored in the DC capacitance, and the voltage starts increasing as seen in the DC voltage graph. The figure shows how once the voltage reaches 1.5 pu the operation of the VSC converters stops. This is equivalent to the DC over-voltage protection implemented in the HVDC transmission system.

In the following sections, experimental results for fault events using different fault impedance levels are presented for each of the four DBS circuits under study. In order to avoid repetition, Figs. 6.4, 6.5 and 6.6 show the AC waveforms for both VSC stations during successful fault ride-through events with different fault impedances. The lower the fault impedance, the lower will be the power that VSC2 can extract from the DC link and inject in the AC grid. Therefore the lower the fault impedance the larger the power dissipation in the DBS. In particular, the fault impedance is set to reduce the power injection capability of VSC2 down to 0%, 30% and 60% respectively. It can be noticed how, as the power injection capability increases, the AC voltage in VSC2 terminals during the fault is also larger, since the fault impedance is larger while the fault current limitation is kept constant. For all three fault events both VSC stations successfully ride through the fault as a DBS circuit absorbs the excess power in the DC link. In the following sections, only the DC system and DBS waveforms are therefore shown, acknowledging that the AC waveforms will be similar to the ones just presented.

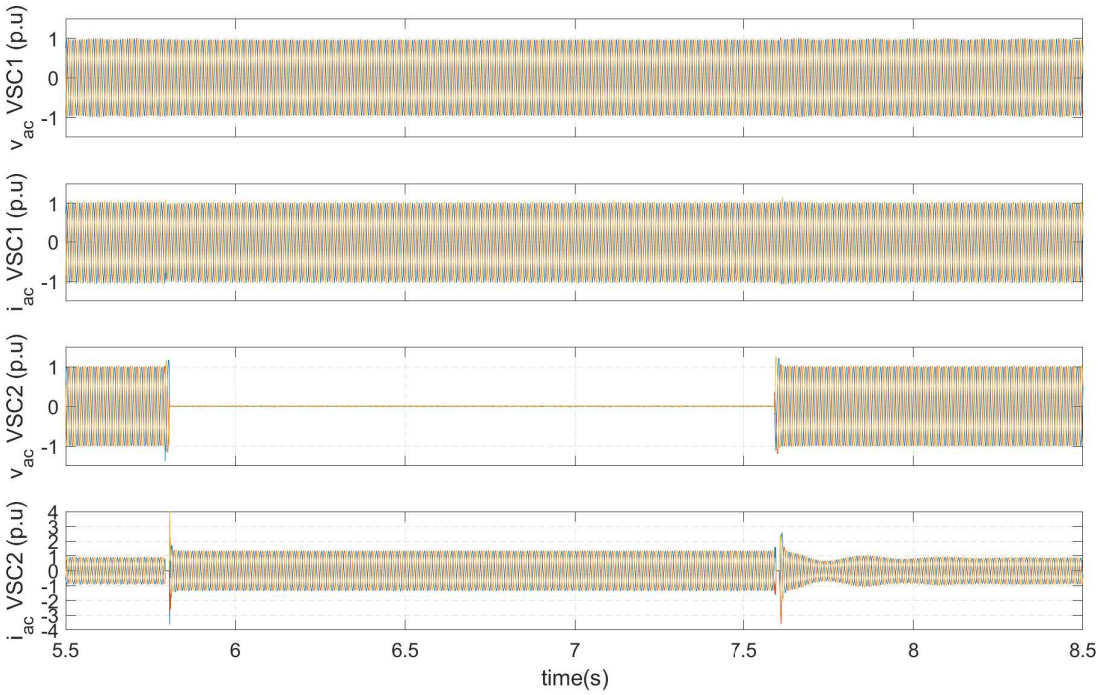


Fig. 6.4 VSC1 and VSC2 AC waveforms for successful fault ride-through with VSC2's P injection capability reduced to 0%.

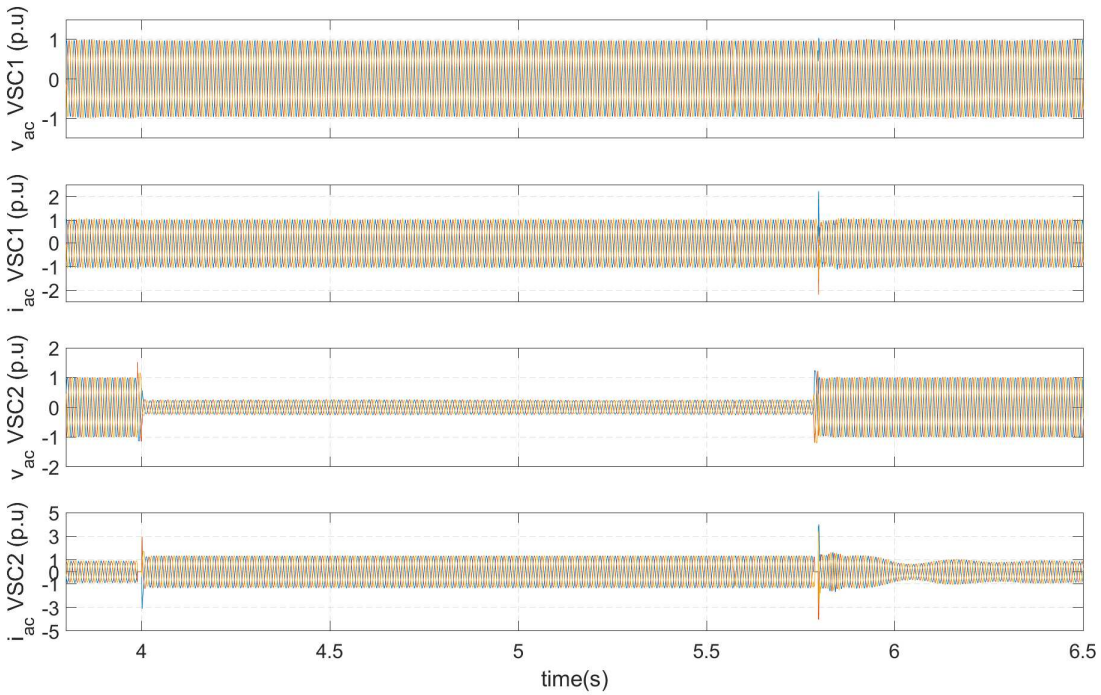


Fig. 6.5 VSC1 and VSC2 AC waveforms for successful fault ride-through with VSC2's P injection capability reduced to 30%.

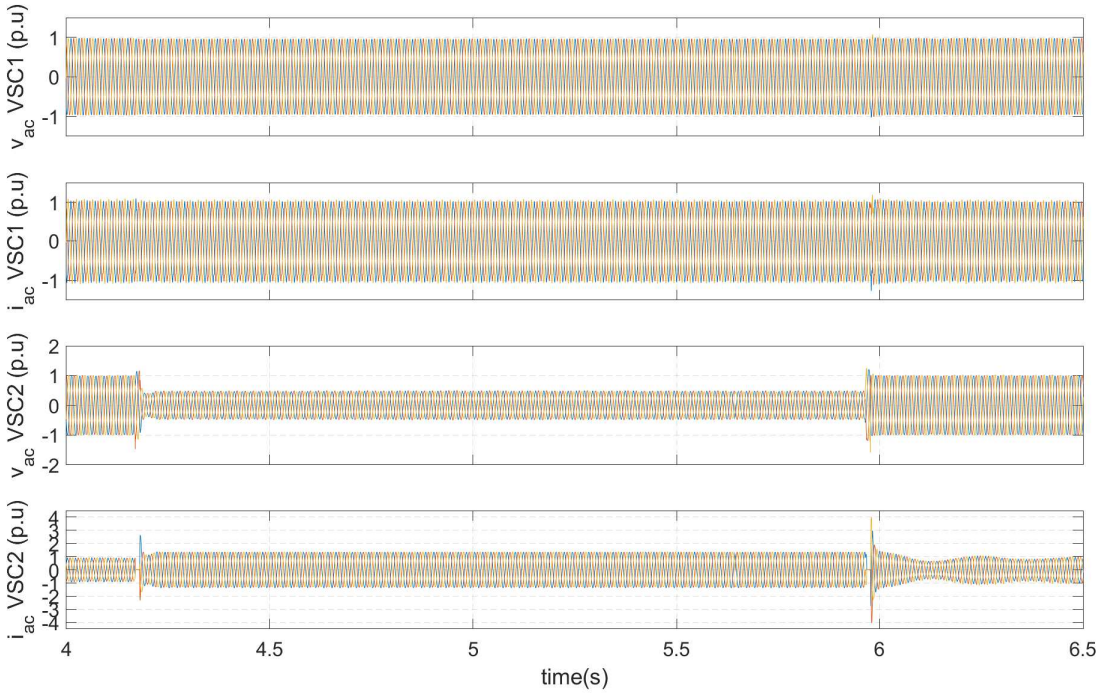


Fig. 6.6 VSC1 and VSC2 AC waveforms for successful fault ride-through with VSC2's P injection capability reduced to 60%.

6.1.1 Malfunction during operation of the fault triggering circuit affecting VSC2

During the testing stage with the experimental platform it was found that the commutation of the contactors from the fault circuit induce a malfunction in

converter VSC2, which eventually leads to a DC over-voltage situation even when a DBS converter is in operation. The analysis of this malfunction is presented here in order to draw some conclusion that will help with the validation of the DBS converter operation.

Fig. 6.7 shows the DC voltage and the active power flow in both VSC stations together with the power dissipation in the DBS during a test with the experimental platform where the 1.8s fault is applied and the DBS circuit is active in order to limit the maximum DC over-voltage to the predefined UOVL value. The operation of the fault circuit contactors SSR1 and SSR2 (Fig. 6.1) leaves momentarily the AC terminals of VSC2 in open circuit before the fault impedance is applied at the start of the fault (around time time=4 s) or after it is disconnected at the end of the fault (time=5.8 s).

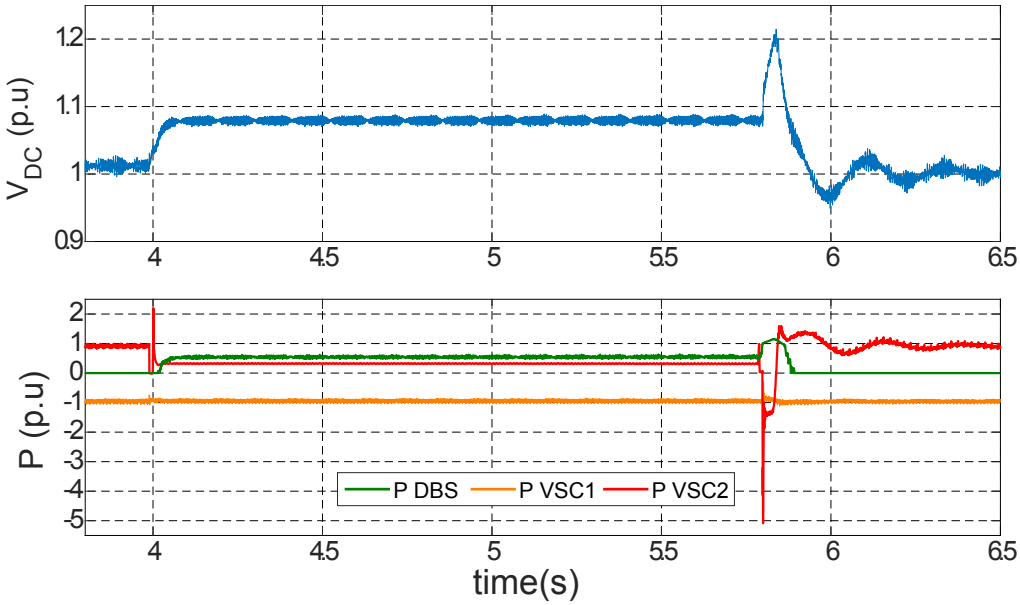


Fig. 6.7 VSC2 malfunction during commutation of the fault circuit contactors.

As observed in the power plot, before the fault, VSC1 is injecting 1 pu power into the DC link and VSC2 is extracting 1 pu power from the DC link, while no power is dissipated in the DBS. When the fault starts the contactors operate and when VSC2 is connected to the fault impedance a peak power of 2 pu is observed before the power extraction capability of VSC2 is reduced as a consequence of the fault. Simultaneously the DC voltage starts increasing and the DBS circuit start to operate dissipating power in order to successfully limit the DC link over-voltage to a value below 1.1 pu. At time=5.8 s the fault event finishes and the fault contactors operate, leaving the AC terminals of VSC2 again in open circuit, and after the 15ms delay, the second contactor reconnects VSC2 terminals to the AC grid. It is at this time that the malfunction in VSC2 occurs, and the converter starts injecting power into the DC link instead of extracting it as would be the normal behaviour, since VSC2 is in charge of regulating the DC link voltage to

1 pu permanently. After a short spike of -5 pu, VSC2 injects a bit more that 1 pu into the DC link for a time period of around 40 ms. The result is that both VSC1 and VSC inject simultaneously a total active power of more than 2 pu into the DC link. As observed, even if the DBS reacts correctly and goes into full power dissipation mode, since the circuit and the resistor are only dimensioned to dissipate a maximum power of 1 pu, the consequence is that the DC voltage starts rising and exceeds the 1.1 pu maximum over-voltage level the DBS is supposed to ensure. Eventually, after those 40 ms the VSC2 voltage controller recovers and reverses the power flow, helping the DBS to bring down the DC link voltage back to its nominal value. As observed for the complete fault duration, the DBS adjusts its power dissipation level correctly to the DC over-voltage level and it only stops power dissipation once the voltage falls below the LOVL value at 1.05 pu. It is only because the power injected in the DC link exceeds its maximum power dissipation capability that it does not manage to avoid the over-voltage situation. In order to clarify the origin of the VSC malfunction, in Fig. 6.8, both the AC voltage and current at the converter terminals are displayed, as well as the detail of the active power flow through VSC2 and the instantaneous power dissipation in the DBS circuit.

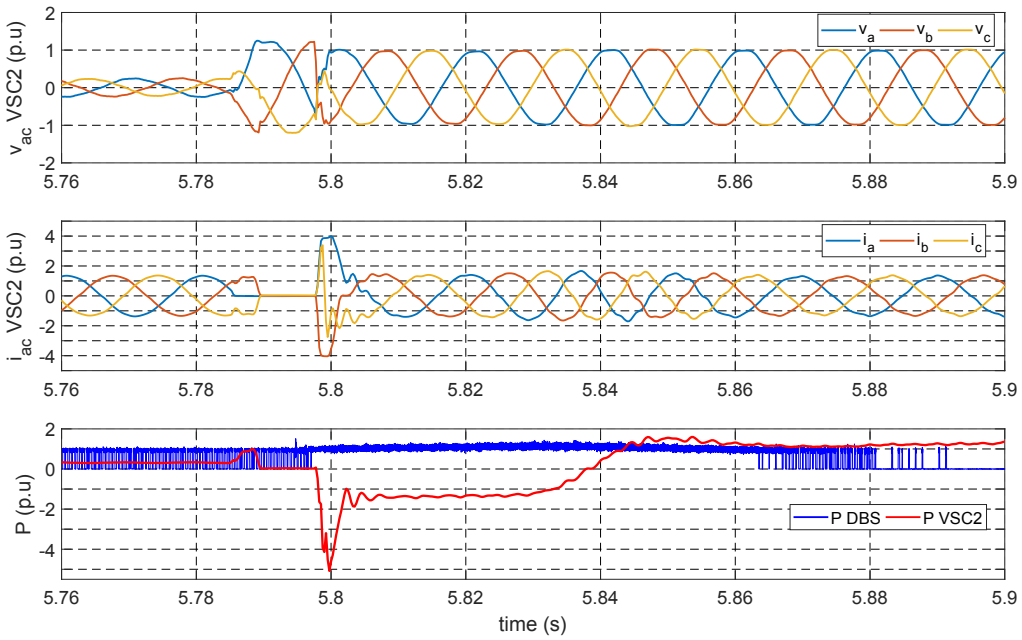


Fig. 6.8 Detailed view of relevant waveforms during the fault circuit commutation that generates the DC over-voltage.

The AC voltage sensors are placed between VSC2's AC inductors and the fault circuit. It can be observed in both the AC voltage and current how the opening of the contactor SSR2 at time=5.785s causes a disturbance in the AC voltage while the AC current drops to zero. 15 ms after, contactor SSR1 closes, reconnecting the AC grid voltage to the VSC2 terminals, and as a consequence

a big jump in the AC voltage phase of around 180 degrees is observed. As a result, after the closing of SSR1, the PLL of VSC2 has lost track of the right AC voltage phase angle, and the generated AC currents are 180 degrees phase shifted with respect to the correct phase they should have. The result is that for the transient of around two AC cycles (40 ms) that it takes for the PLL to regain the correct tracking of the AC voltage phase angle, VSC2 injects 1 pu power into the DC link instead of extracting it, and the result is the already discussed DC over-voltage. In the curve of the power dissipated by the DBS it can be seen how almost instantaneously when the malfunction occurs, the DBS starts dissipating 1 pu power, which demonstrates its correct operation for the complete duration of the fault.

This analysis has found the reason behind the DC over-voltage which is observed at the end of the fault event in some of the experimental results with the DBS circuits. It has also proven that the DBS operates correctly for the complete duration of the fault event, and it is only the physical limitation to dissipate a maximum of 1 pu power which does not allow it to successfully limit the over-voltage during the malfunction of VSC2. On this basis, the over-voltage at the end of the fault event will be ignored when judging the correct operation of the four different DBS circuits during the experimental results presented next.

6.2 Evaluation of the HVDC chopper circuit: DBS#1

The parameters used for testing the operation of this circuit with four different fault impedances are shown in Table 6.4. The value of the braking resistance is the closest approximation that can be obtained to the value of 242Ω calculated with expression (3.6) when using the 47 Ω sections available in the test platform. The fault impedances R_{rheo} in the table are chosen for the power injection capability in VSC2 to reduce to 0%, 30%, 60% and 75% of its nominal value P_{DC}. The waveforms captured for each case are presented in Figs. 6.9, 6.10, 6.11 and 6.12 respectively. Three graphs are shown in each figure:

- DC bus voltage.
- Power dissipation in the DBS.
- DBS current.

As the DBS has a pulsed power characteristic, for clarity only the filtered average power curve is included in the active power graph. Comparing the DC voltage evolution from the four figures with the results from Fig. 6.3, it can be seen that the operation of the DBS successfully limits the maximum DC bus

Table 6.4 Parameters used with the DBS#1 circuit during the tests.

DBS #1 TEST PARAMETERS	
VSC transmitted power (P_{DC})	800 W
Braking resistance (R_{dbs})	235Ω
Fault impedance (R_{rheo})	0/10/20/25 Ω
DBS operation frequency ($f_{carrier} = 1/T_{carrier}$)	2 kHz

over-voltage to the desired level of 1.1 pu for all faults during the complete fault duration, apart from the transient event at the end of the fault caused by the malfunction of VSC2 due to the commutation of the fault circuit.

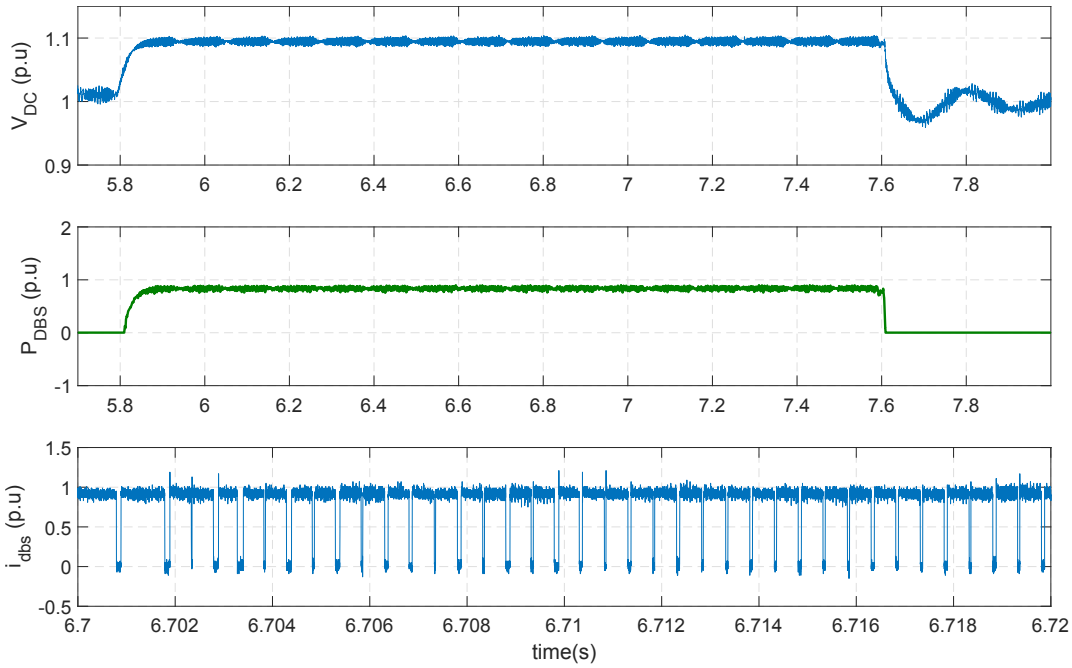


Fig. 6.9 Fault with 0% VSC2 P injection capability and the HVDC chopper DBS in operation.

A 2 kHz carrier, commonly used with power IGBTs, is used by the controller's PWM function as observed in the graph of the DBS current. The duty cycle reduction is also observed as the VSC2 injection capability increases. For the 75% injection capability case, it is observed that the DBS does not dissipate power in the braking resistor during some of the PWM periods. This is due to the imposition of a minimum 10% duty cycle to limit the minimum voltage pulse width to 50 μs, which is the minimum turn on/off time for the semiconductor switches implemented in the gate drive circuit. Ideally the average power dissipated by the DBS equals the difference between the power injected in the DC bus by VSC1 and the power extracted by VSC2, which changes according to the applied fault impedance. In reality, the system power losses, mainly in the VSC converter stations, also need to be subtracted from this quantity to obtain

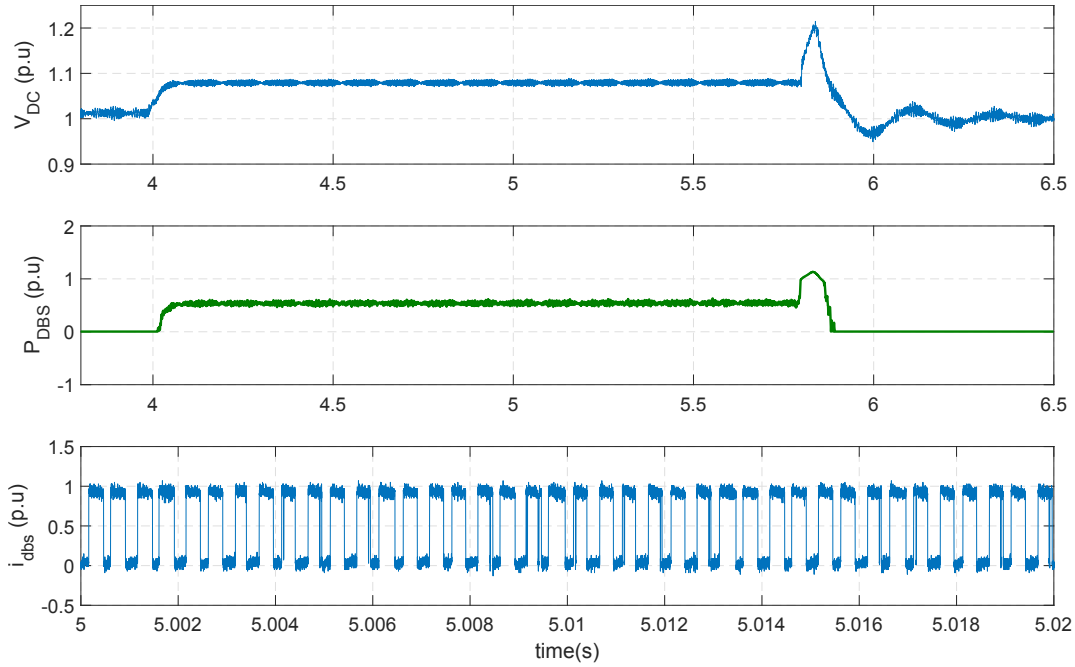


Fig. 6.10 Fault with 30% VSC2 P injection capability and the HVDC chopper DBS in operation.

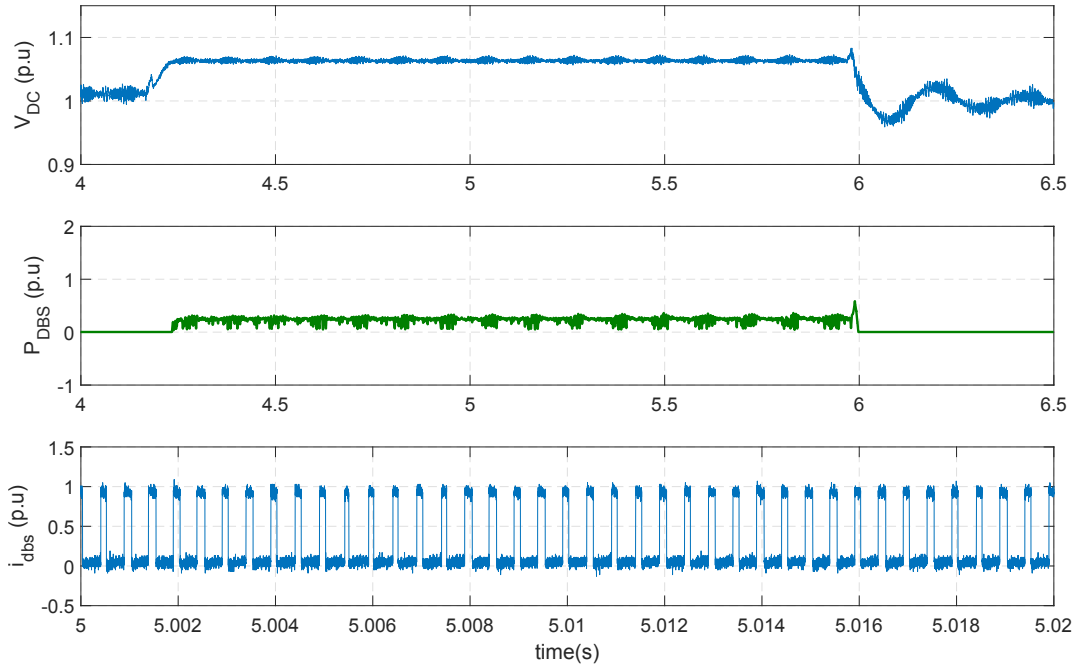


Fig. 6.11 Fault with 60% VSC2 P injection capability and the HVDC chopper DBS in operation.

the power to be dissipated by the DBS. Power losses in the experimental test platform are in the region of 10%. Hence the required average power dissipation in the DBS circuit during the four fault cases under study is of 90%, 60%, 30% and 15% of the nominal power respectively.

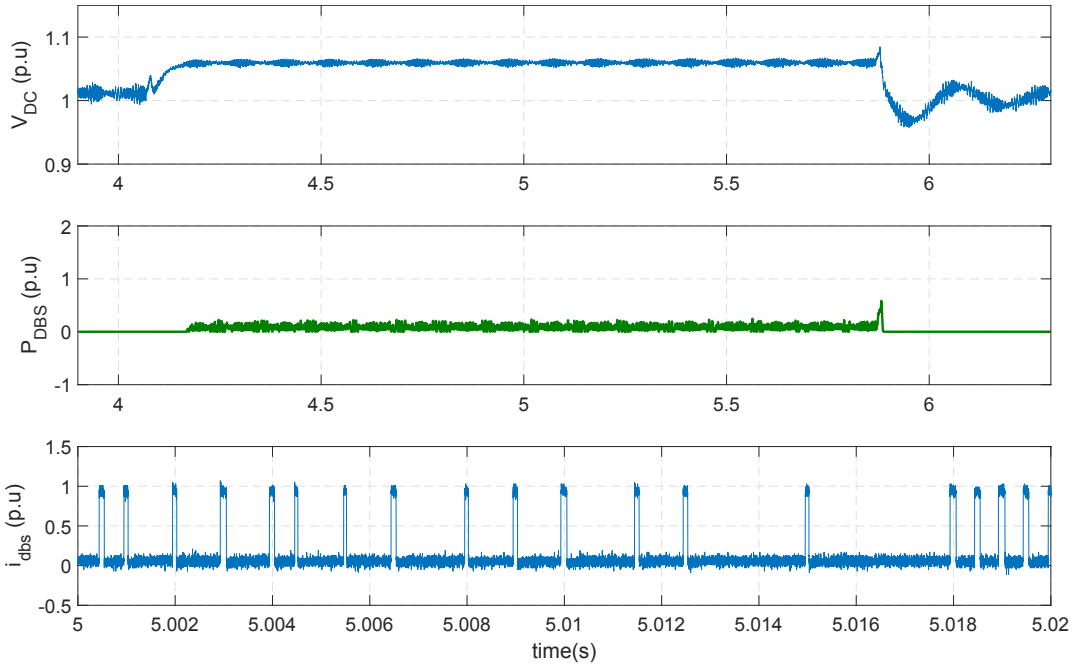


Fig. 6.12 Fault with 75% VSC2 P injection capability and the HVDC chopper DBS in operation.

6.3 Evaluation of the multilevel chopper circuit: DBS#2

Table 6.5 shows the parameters used to configure the multilevel chopper DBS during experimental testing. Figs. 6.13, 6.14, 6.15 and 6.16 show the experimental results for the operation of the circuit when the four different fault impedances are applied. Five graphs are shown in each figure, with the addition of the cell capacitor voltages. In this case, due the use of distributed braking resistors, the voltage across the resistor in one cell, in this case cell M9, is shown as an example.

Table 6.5 Parameters used with the DBS#2 circuit during the tests.

DBS #2 TEST PARAMETERS	
VSC transmitted power (P_{DC})	550 W
DBS cell capacitance (C_{cell})	440 μF
Braking resistance (R_{dbs})	22 Ω
Fault impedance (R_{rheo})	0/6.8/13.5/17 Ω
DBS balancing frequency ($f_{balancing} = 1/T_{balancing}$)	2 kHz

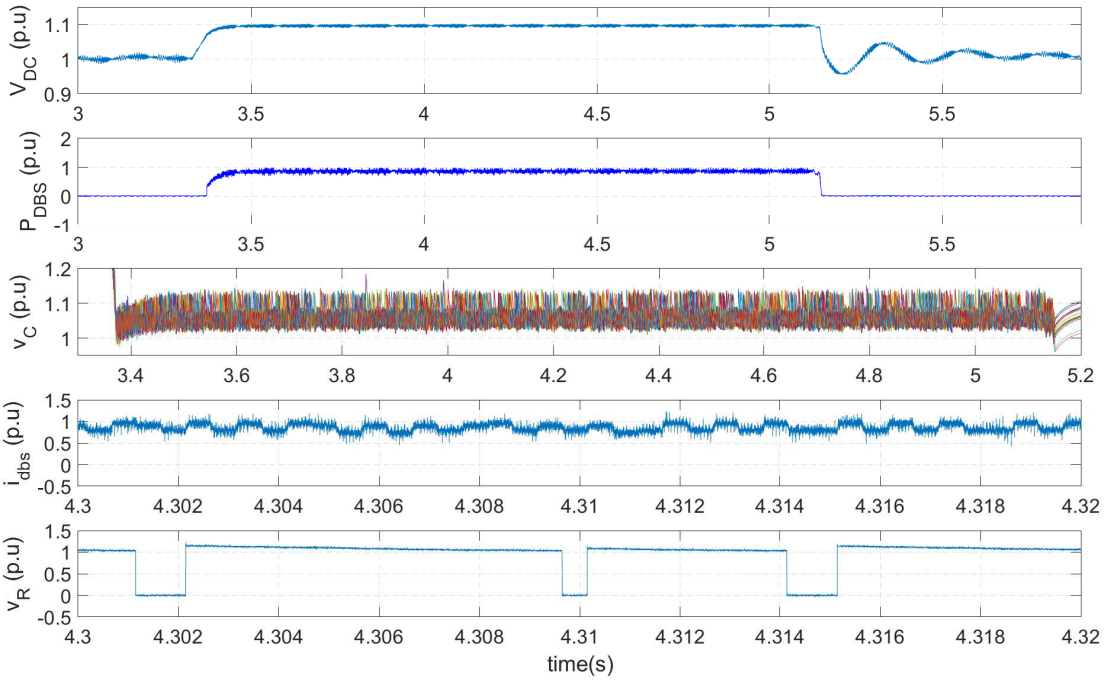


Fig. 6.13 Fault with 0% VSC2 P injection capability and the multilevel chopper DBS in operation.

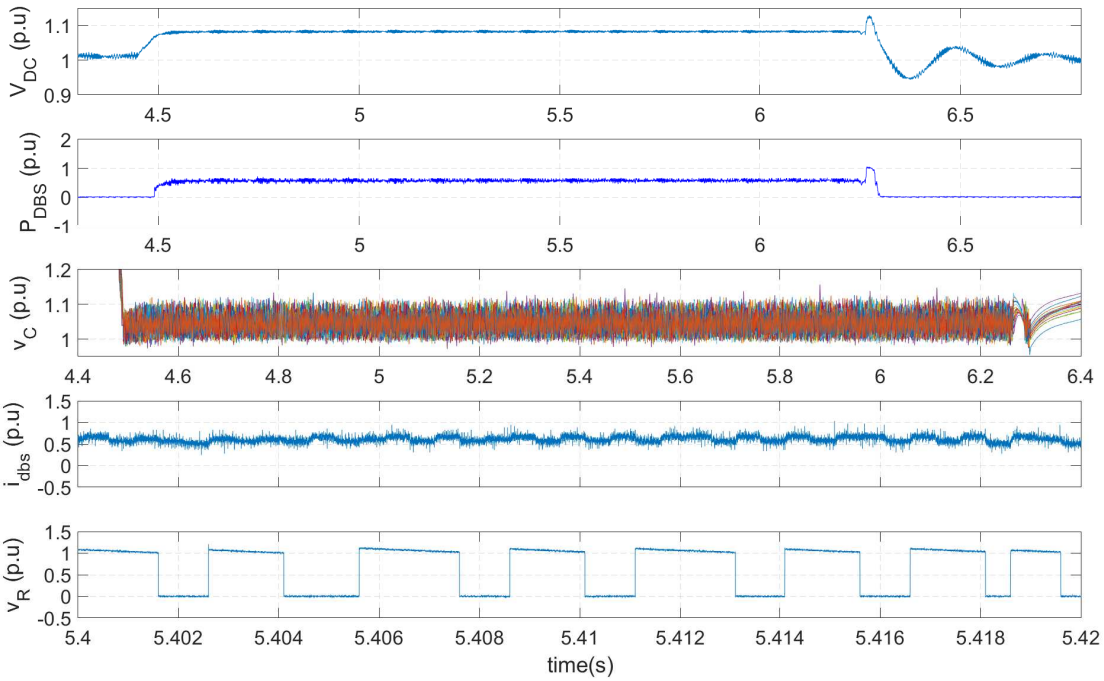


Fig. 6.14 Fault with 30% VSC2 P injection capability and the multilevel chopper DBS in operation.

The DC bus voltage curves in each of the four figures corroborate the correct operation of the proposed control strategy to operate the DBS circuit and limit the DC over-voltage to the desired value of 1.1 pu with the four different fault impedances. The DBS power and current curves display the already mentioned

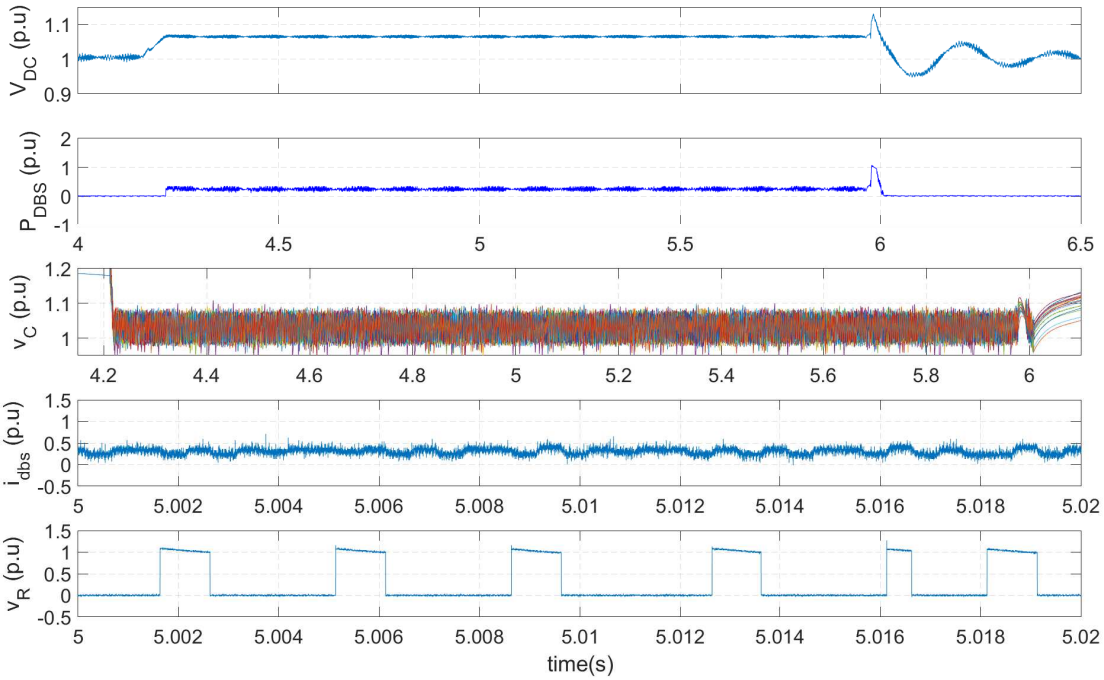


Fig. 6.15 Fault with 60% VSC2 P injection capability and the multilevel chopper DBS in operation.

characteristic of having a DC component with a small superimposed ripple as opposed to the pulsed characteristic of the other three circuits, which makes this the best performing circuit with respect to radiated EMI.

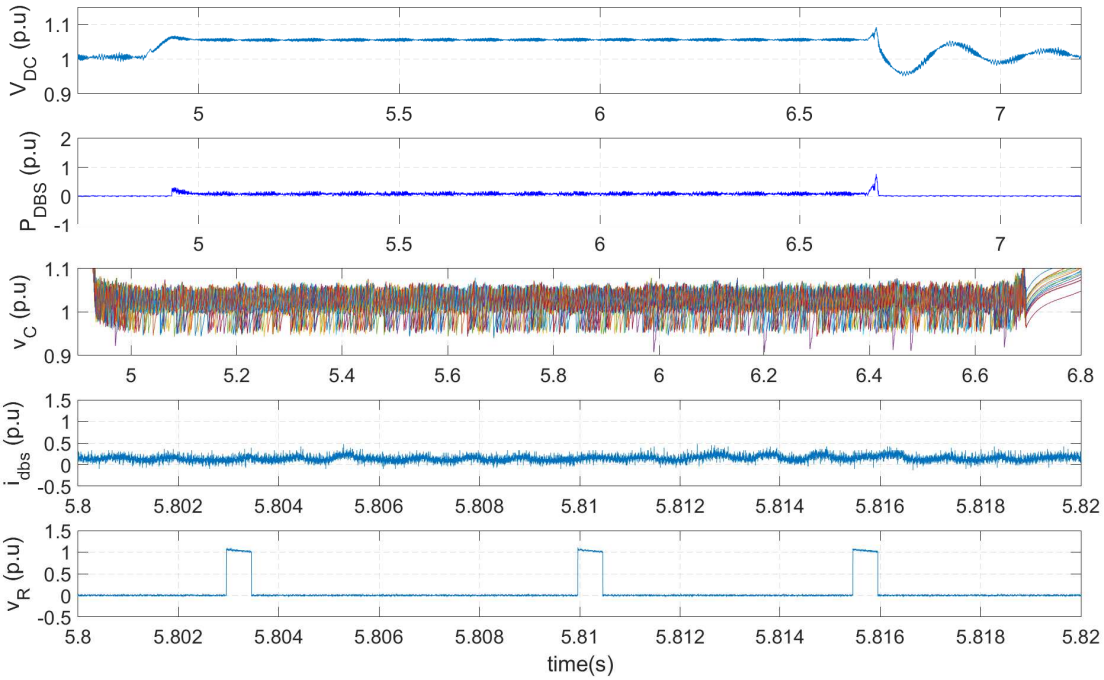


Fig. 6.16 Fault with 75% VSC2 P injection capability and the multilevel chopper DBS in operation.

The graph displaying the cell capacitor voltages validates the satisfactory operation of the balancing function in keeping the total arm energy well distributed among the cells. A balancing frequency of 2 kHz is chosen for the circuit. In modular circuits like the multilevel chopper DBS arm, the effective switching frequency of each cell is lower than the frequency of execution of the balancing algorithm, since only a few cells change their commutation state in order to modify their energy level every time the algorithm is executed. Taking into account the already stated 10% power losses in the VSC stations, the DBS dissipates 90%, 60%, 30% and 15% in Figs. 6.13, 6.14, 6.15 and 6.16 respectively. The braking resistor voltage curve shows how the cell switching frequency is minimum for the 90% and 15% power dissipation case, and maximum for the 60% case, in line with what was presented in Chapter 3 and illustrated in Fig. 3.14. An effective cell switching frequency in the region of 150-400 Hz can be measured from these experimental results. There is a compensation effect between the variation in switching frequency and average DBS current which makes the cell voltage ripple to stay constant for the entire circuit operation band, from 0 to 100% power dissipation. This is validated with the experimental results, where a ripple in the 0.1 pu region is observed in the four different cases.

6.4 Evaluation of the half-bridge multilevel circuit: DBS#3

Table 6.6 shows the parameters used for testing the half-bridge multilevel DBS circuit. The values $f_{balancing}$ and dv/dt are chosen to achieve a good resolution in terms of voltage steps to generate the trapezoidal voltage ramps when using 16 cells. A ramp from 0 to 1.1 pu voltage generated by the DBS then contains a minimum of 8 voltage steps, which as observed in the R_{dbs} voltage graph from Fig. 6.17, gives a good approximation to an ideal ramp. The selected value for voltage V_A implies that the stack of cells is capable of generating a voltage 25% larger than the DC bus voltage. In a commercial project, with the power cells designed to operate close to their maximum voltage limit, this extra voltage generation capability would be achieved by adding 25% extra cells. In the test platform, for simplicity and since the cells are designed with enough voltage margin, the average cell voltage is increased by 25% instead. The value of the lumped resistance is the closest possible approximation using 47 Ω sections to the value of 150Ω calculated with expression (3.23). The fault impedances for the tests are also shown in the table. A trapezoidal modulation period (T_m) of 4 ms is chosen. This is approximately 10 times smaller than the value calculated with expression (3.46) which would be the maximum acceptable period to correclty track the required power demand and to avoid exceeding the desired maximum

DC over-voltage. As can be observed in Fig. 3.40 from Chapter 3, where 48 ms was the maximum modulation period, a period 10 times smaller than this maximum, in that case 5 ms, achieves a smoother regulation of V_{DC} for the duration of the fault as well as a smoother power dissipation the DBS. This has therefore been the criteria followed here.

Table 6.6 Parameters used with the DBS#3 circuit during the tests.

DBS #3 TEST PARAMETERS	
VSC transmitted power (P_{DC})	800 W
Braking resistance (R_{dbs})	141 Ω
Fault impedance (R_{rheo})	0/10/20/25 Ω
DBS cell capacitance (C_{cell})	440 μF
Trapezoidal modulation period (T_m)	4 ms
DBS balancing frequency ($f_{balancing} = 1/T_{balancing}$)	20 kHz
Voltage derivative (dv/dt)	1.05 V/μs
Voltage amplitude V_A	$V_{DC}/4$ V
Voltage amplitude V'_A	$V_B/4$ V

By observing the DC bus voltage evolution during the fault event in Figs. 6.17, 6.18, 6.19 and 6.20, it can be concluded that the proposed controller and circuit configuration succeeds in limiting the DC over-voltage to the desired 1.1 pu value, with the four different fault impedances. The cell capacitor voltages graph also shows how the energy balancing is correctly achieved by the proposed modulation strategy.

The DBS valve current graph for each of the four tests shows how the modulation strategy changes the shape of the trapezoidal voltage pulse to adapt the average power dissipation to the required amount according to the fault impedance. As already mentioned, the DBS circuit dissipates 90%, 60%, 30% and 15% of the nominal power respectively during each of the four tests. Since the crossover point, the power dissipation level for which the change from the time modulation region to the amplitude modulation region occurs, is in this case is situated at around 10% of the nominal power, the circuit operates in the time modulation region for all the four cases. It can be observed how the duration of subinterval T_2, during which the DBS valve generates zero voltage (hence applying V_{DC} across R_{dbs}), is progressively reduced as the fault impedance is increased. In the particular case of Fig. 6.20, with the DBS operating around the 15% power dissipation region, it can be observed how during one of the commutation cycles the circuit enters the amplitude modulation region. This is due to the ripple present in the DC voltage, which enters the control system and introduces a small variation in the operation point for each successive commutation cycle, which does not have an impact on the average power dissipation value.

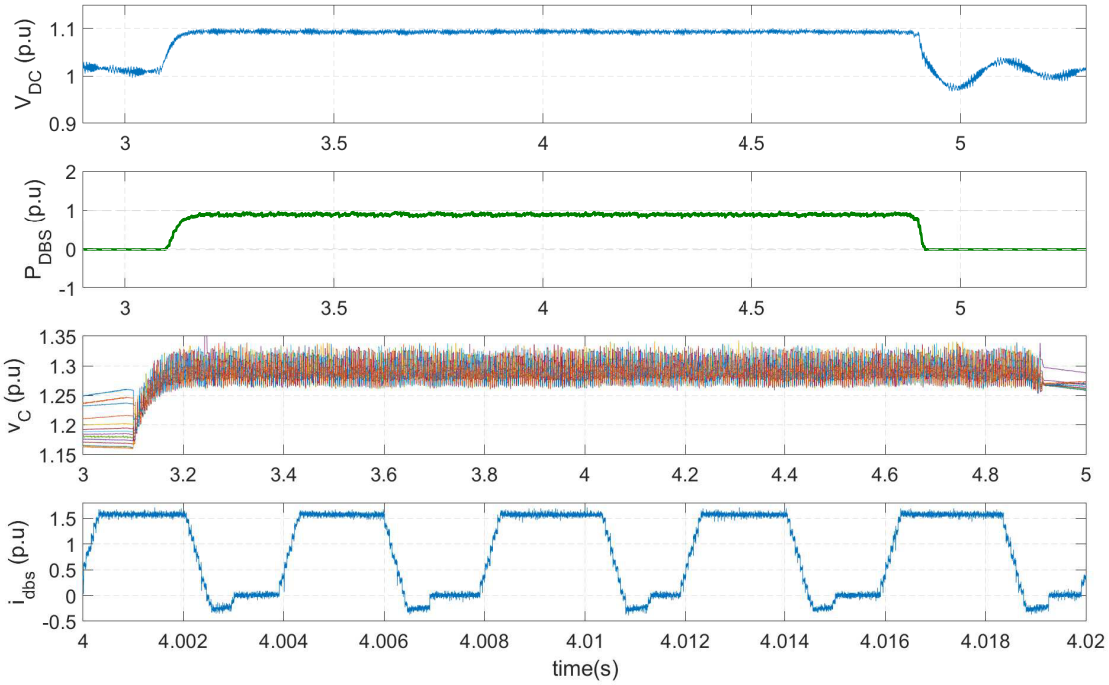


Fig. 6.17 Fault with 0% VSC2 P injection capability and the half-bridge multilevel DBS in operation.

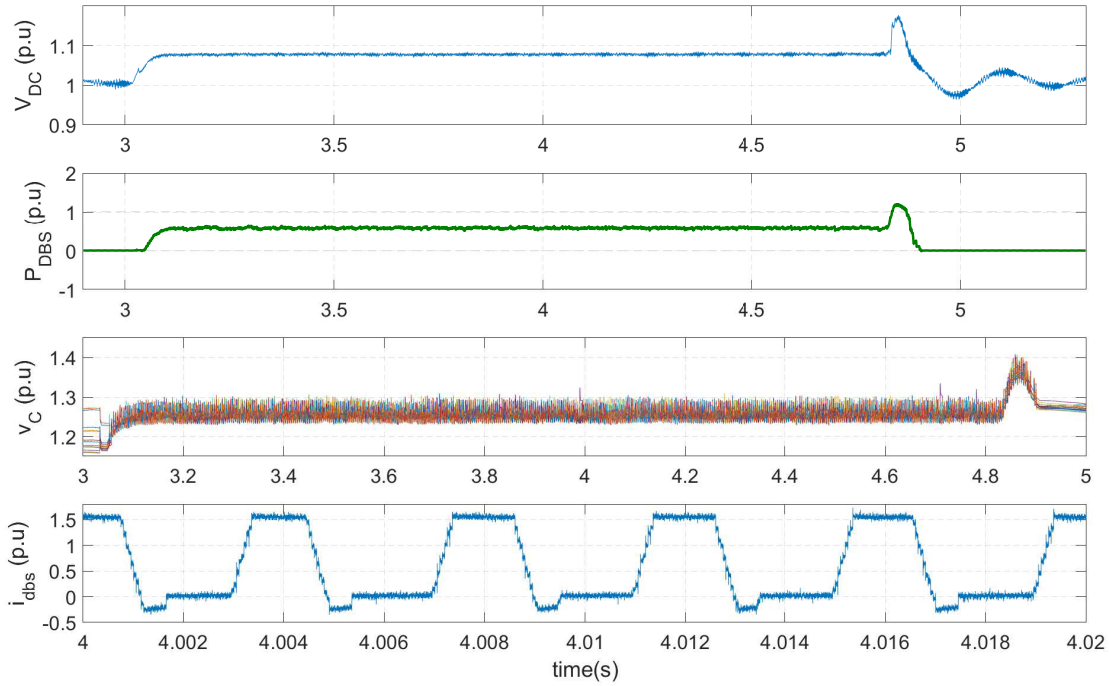


Fig. 6.18 Fault with 30% VSC2 P injection capability and the half-bridge multilevel DBS in operation.

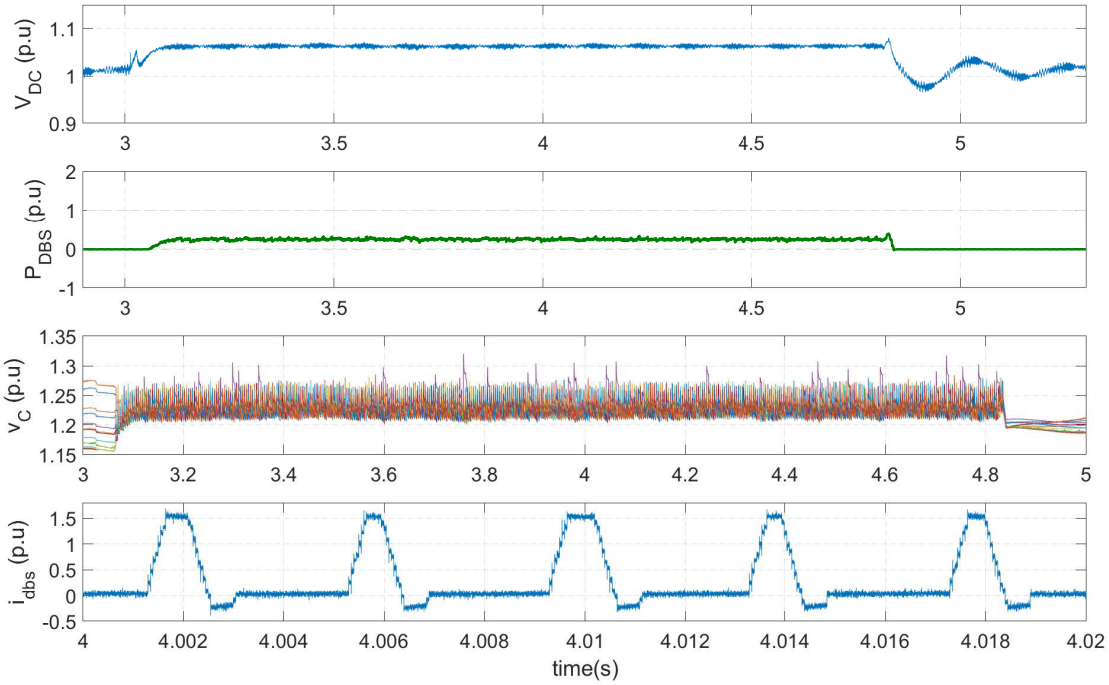


Fig. 6.19 Fault with 60% VSC2 P injection capability and the half-bridge multilevel DBS in operation.

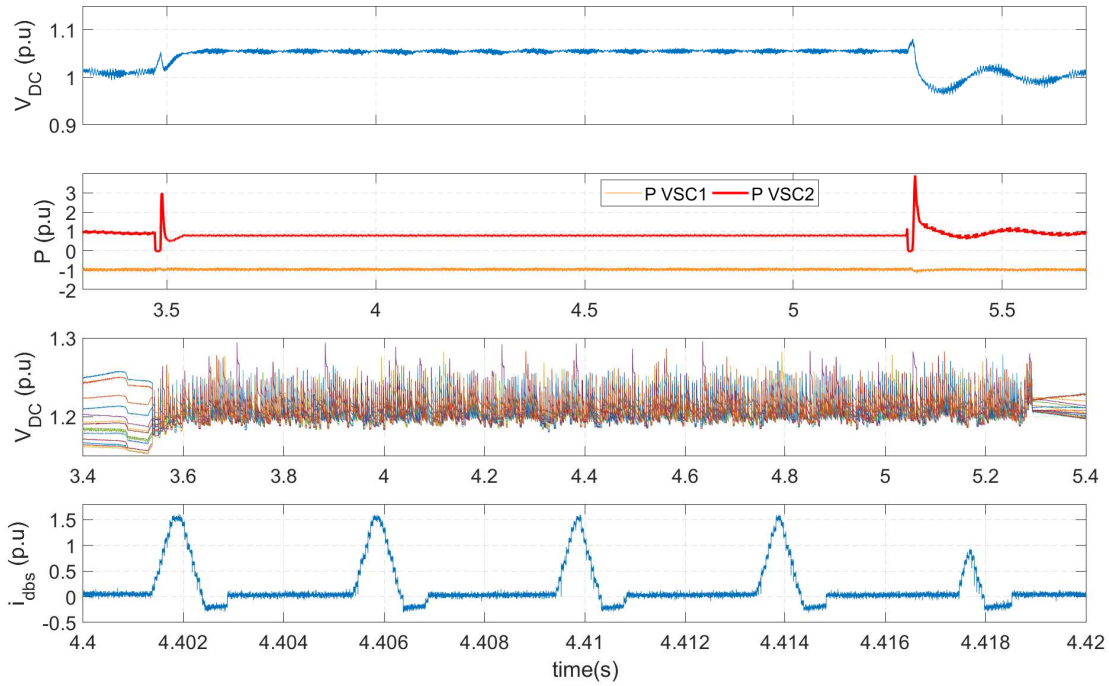


Fig. 6.20 Fault with 75% VSC2 P injection capability and the half-bridge multilevel DBS in operation.

6.5 Evaluation of the full-bridge multilevel circuit: DBS#4

Table 6.7 shows the parameters used to configure the experimental tests with this circuit. The braking resistor value is the closest approximation to the value 187Ω obtained with expression (3.43) when using the 47Ω sections available in the platform. In general, all the parameters are kept the same as used for testing the half-bridge multilevel circuit, with the exception of the value of the braking resistor and the voltage amplitude V_A. The latter is used to discharge the DBS arm energy, as was explained in Chapter 3. With the half-bridge circuit, power dissipation during subinterval T_5 of the trapezoidal pulse (voltage amplitude $V_{DC}+V_A$ is applied) is very low. Therefore, to minimize the subinterval duration in order to achieve the required average power dissipation, a larger value of V_A is used. For the same reason, a smaller braking resistance is also used in the half-bridge circuit, which increases the instantaneous power dissipation during the whole modulation period.

The results in Figs. 6.21, 6.22, 6.23 and 6.24, show that the trapezoidal modulation and controller operation achieve a correct DC over-voltage limitation to the defined 1.1 pu value. The graphs of the cell capacitor voltages validate the correct operation of the modulation strategy and the capacitor energy balancing to achieve the energy balance in the arm. The graph also shows how with the full-bridge circuit no extra cells or an increase in the average cell voltage is needed, as opposed to the half-bridge based circuit. The energy discharge subinterval, during which the negative valve voltage is generated, is well appreciated towards the end of the trapezoidal pulse in the DBS arm current from Fig. 6.21, identified as the subinterval where the peak current occurs.

Table 6.7 Parameters used with the DBS#4 circuit during the tests.

DBS #4 TEST PARAMETERS	
VSC transmitted power (P_{DC})	800 W
Braking resistance (R_{dbs})	188 Ω
Fault impedance (R_{rheo})	0/10/20/25 Ω
DBS cell capacitance (C_{cell})	440 μF
Trapezoidal modulation period T_m	4 ms
DBS balancing frequency $f_{balancing} = 1/T_{balancing}$	20 kHz
Voltage derivative (dv/dt)	1.05 V/μs
Voltage amplitude V_A	V_{DC}/8 V

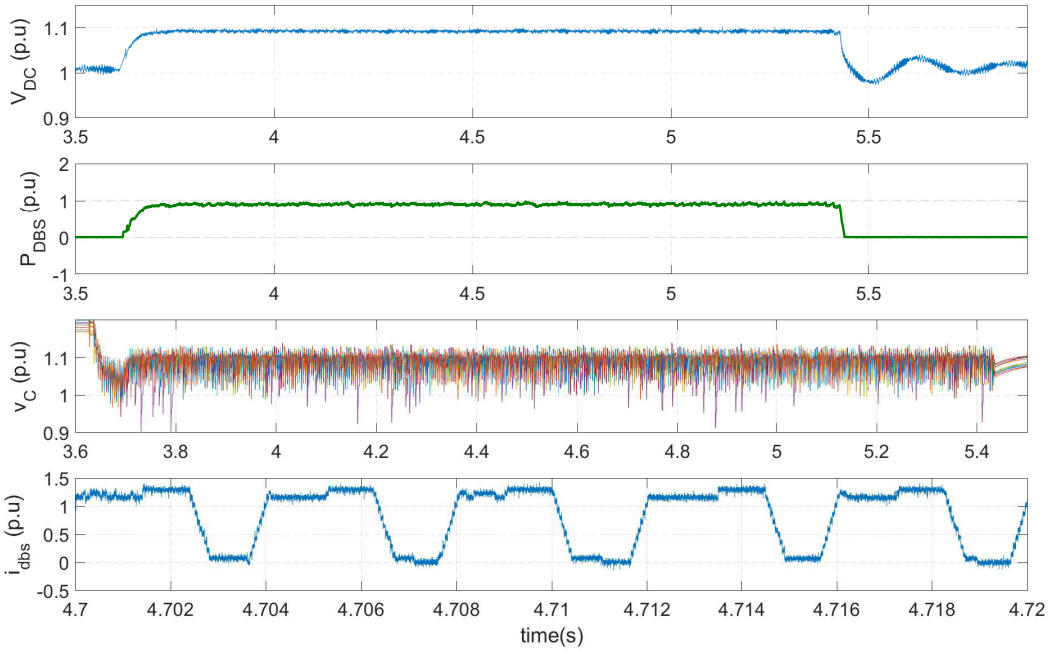


Fig. 6.21 Fault with 0% VSC2 P injection capability and the full-bridge multilevel DBS in operation.

For the DBS parameters being used, the crossover point that marks the transition between the first and the second modulation regions, as presented in section 3.5.2, is situated at 36% of the nominal power dissipation. During the second modulation region, a variable voltage derivative is used in the trapezoidal ramps to adjust the power dissipation and achieve the energy balance. The operation in the variable dv/dt region produces almost square pulses for power dissipation levels in the region of 1% to 5% which might impose more severe EMC mitigation requirements in a real scheme implementation. It was therefore decided to limit the operation of the DBS circuit to the first modulation region. The average power dissipation per trapezoidal pulse is therefore limited to values between 36% and 100% of the nominal value, but as described next, the DBS can still adjust the average power dissipation for the duration of the fault to values down to 0%.

Comparing the DBS current plots from the four tests, the evolution of the modulation strategy is appreciated. Between Figs. 6.21 and 6.22, a reduction in the duration of subinterval T_2 is observed. This reduces the average power dissipation from 90% down to 60%. A new trapezoidal pulse is applied every 4 ms, in line with the selected modulation period T_m. In Fig. 6.23, the power dissipation in the DBS is reduced to 30%, which is below the crossover point for both modulation regions. Since the operation in the second modulation region is not allowed, a trapezoidal with a T_2 duration of zero is now applied, which represents an average power dissipation of 36%, the minimum within the first modulation region. The excess in power dissipation is compensated by further spacing the

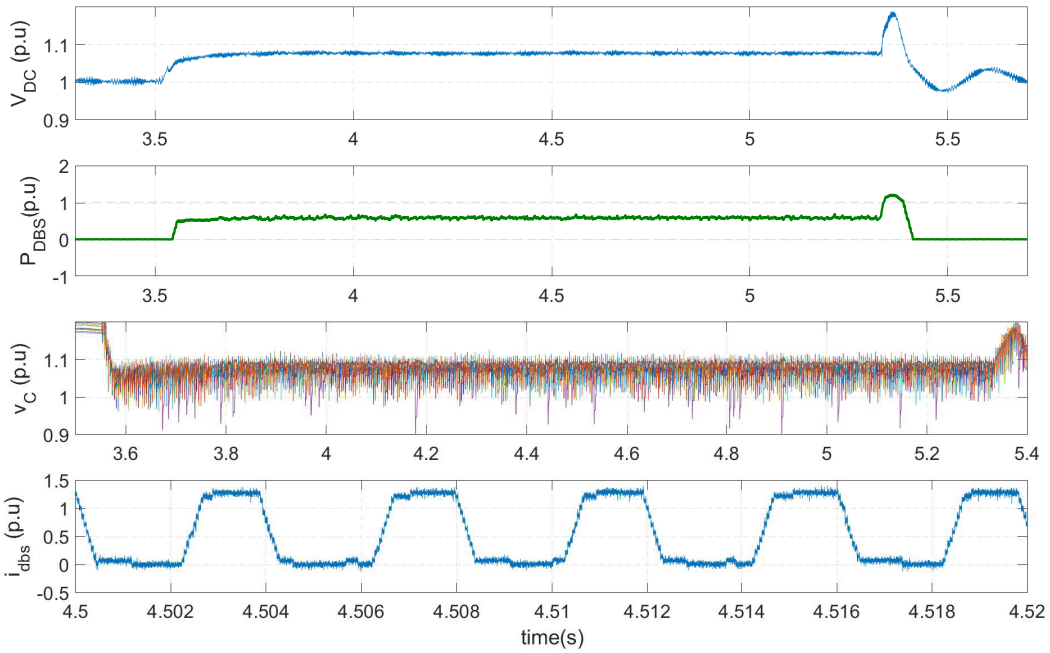


Fig. 6.22 Fault with 30% VSC2 P injection capability and the full-bridge multilevel DBS in operation.

trapezoidal pulses as also observed in Fig. 6.23. This effectively reduces the DBS average power dissipation to the required level without entering the second modulation region. Fig. 6.24 shows the results for a 15% power dissipation in the DBS. Here, the trapezoidal pulses are even further spaced to achieve the required additional average power reduction. These results demonstrate how the successful operation of the DBS#4 is possible without the need to enter the variable dv/dt modulation region. This avoids a degradation in the EMC performance of the DBS circuit while being easier to implement by the DBS controller.

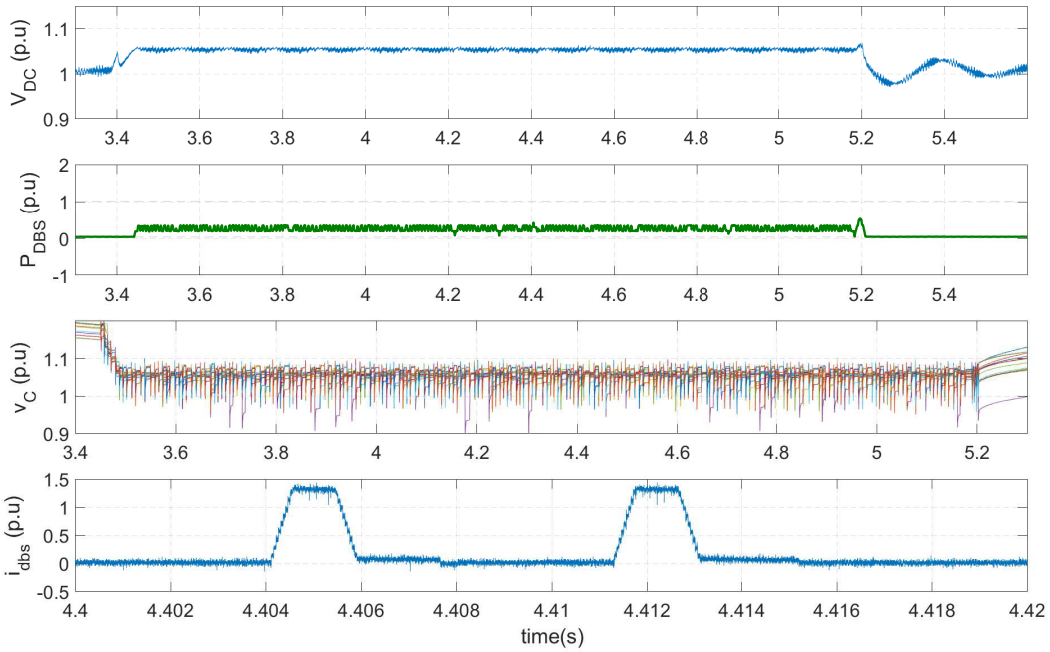


Fig. 6.23 Fault with 60% VSC2 P injection capability and the full-bridge multilevel DBS in operation.

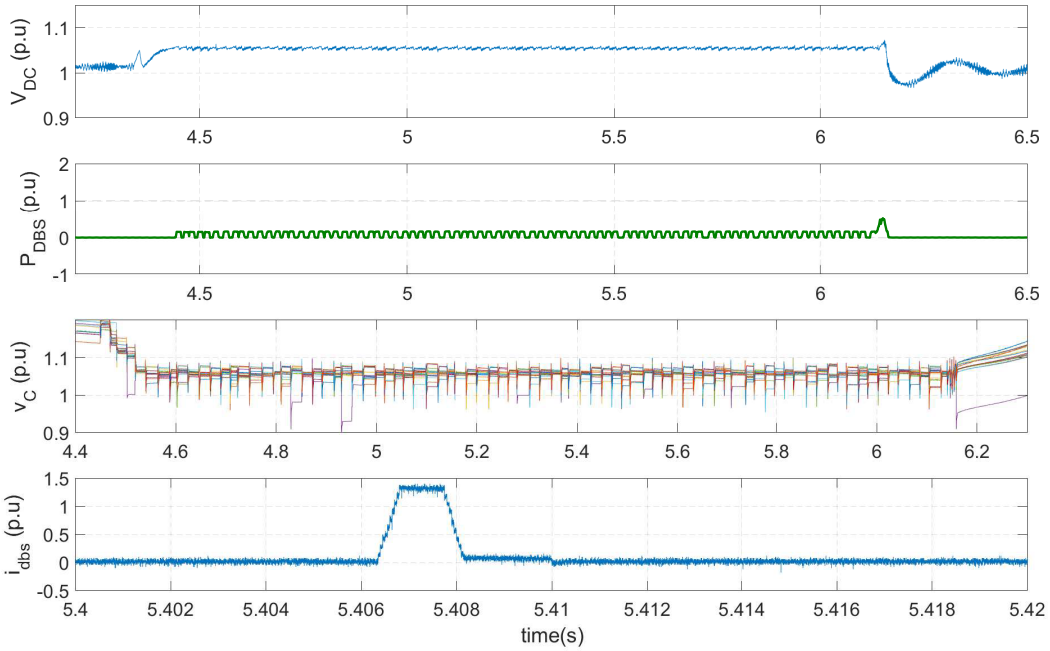


Fig. 6.24 Fault with 75% VSC2 P injection capability and the full-bridge multilevel DBS in operation.

6.6 Summary of the chapter

In this chapter the experimental results obtained from the laboratory test platform for each of the four DBS circuits under study have been analysed. The objective of the tests is to validate the operation of the proposed control strategies for each circuit in a real hardware environment. To achieve this, the fault triggering circuit included in the test platform has been used to perform four tests with each circuit. A different fault impedance has been applied at the terminals of VSC2 station, forcing the DBS circuits to operate at different points of their dissipation capability curve.

The reason behind the transient over-voltage occurring at the end of the fault for some of the experimental results with the DBS converters was found to be the disturbance on the AC voltage phase angle at the terminals of VSC2 when the fault circuit commutates as analysed in section 6.1.1. This analysis has also proved that the DBS circuits operate as expected even during these transient over-voltages. Based on these conclusions, the experimental results have been successful for the four DBS circuits, and have validated the control strategies developed in Chapter 3.

In the particular case of the full-bridge multilevel DBS the experimental results have shown that the circuit operates successfully without the need to enter the second modulation region, where the dv/dt of the trapezoidal voltage pulses is varied and can reach very high values. Even if the trapezoidal modulation operation is limited to the first modulation region, the circuit can still deliver the required average power dissipation down to zero and the drawbacks of increased EMI and stress on converter components due to a high dv/dt are eliminated.

The experimental results also highlighted the problems with the fault circuit that was selected for the test platform. In the future it would be recommended to replace this circuit by an electronic AC power supply which would allow to reduce the AC voltage to the desired level for a period of time in order to emulate the same fault events that have been presented here.

Chapter 7

An Energy Diverting Converter: added functionality to the DBS circuit

The high-voltage blocking requirements of a dynamic braking system (DBS) translate into a significant cost which accounts for some millions of euros. Even though the addition of such DBS is usually a requirement from the transmission system operator (TSO), as part of this research project, the option of adding extra functionality to the DBS in order to better justify the economic investment is explored. In the context of an offshore wind-farm interconnection, a DBS spends most of its lifespan inactive. Only when a fault occurs on the onshore AC grid, it enters operation for a few seconds to protect the HVDC link from an over-voltage situation. They are these extended periods of inactivity that may be used for the converter to perform some additional tasks.

The HVDC tapping application has been targeted in this thesis and it is studied in section 7.1. In section 7.2 the concept of merging a DBS and HVDC tap into a single converter is investigated.

7.1 HVDC tapping

The Dynamic Braking Systems studied so far absorb (divert) energy from a DC network to comply with the grid codes (ie. FRT requirements). The diverted energy is then dissipated as heat in the braking resistor. An alternative solution consists of diverting energy into a secondary electrical network. In HVDC, a converter which diverts a small fraction of the link nominal power is known as an *HVDC Tap* [98].

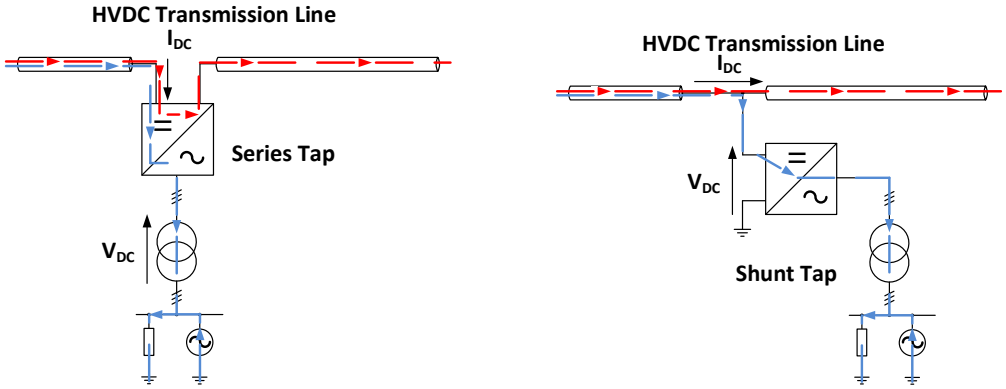
The extracted power, typically below 10% of the HVDC rated power [99], can be used to supply small and isolated rural or urban communities or industrial

areas in the vicinity of existing HVDC transmission systems. In countries such as Canada, Brazil or in regions like central and southern Africa, large amounts of hydro power are transmitted using HVDC schemes. There is great potential to supply communities currently serviced with diesel generation or with no access to electricity at all by tapping small amounts of DC power [100]. This would generate both human and economic benefits, especially for rural areas in developing countries.

Most proposed solutions for the implementation of HVDC taps fall within one of two main groups [98] : series connected or shunt/parallel connected taps (Fig. 7.1). An alternative way of classifying tap circuits is based on the converter type, either line-commutated or self-commutated converters [100].

In series taps (Fig. 7.1a), the HVDC system current (in red) traverses the tap converter itself, and a transformer is used to transfer the energy to the low voltage side. This transformer needs to be isolated to withstand full HVDC voltage. As the main advantage, the voltage blocking requirements for the power electronics are greatly reduced. The main disadvantage is that since the active devices conduct full HVDC current, high losses can be generated, and more important, in case of a fault in the tap the complete HVDC transmission could be disrupted.

Shunt connected taps on the other hand rely on power electronic devices to block the HVDC voltage. Only the tap current flows through the converter in this case, as displayed in Fig. 7.1b.



(a) Series connection. (b) Shunt connection.

Fig. 7.1 Different HVDC tap configurations.

The block diagram of the solution developed in this thesis is presented in Fig. 7.2. It belongs to the group of shunt connected self-commutated taps, and it is based on the same DC/DC plus DC/AC converter arrangement proposed in [99]. A DC/DC circuit performs the required voltage reduction. A low-voltage low-power voltage source converter (VSC) provides the interface with the local AC grid. Only the DC/DC converter needs to withstand full HVDC voltage and

an industrial medium-voltage, low to medium power VSC, can be used. The use of VSC technology allows to supply networks where AC generation from synchronous machines is not present. This configuration also avoids the need for complex transformer arrangements proposed by others, like in [101], [102] or [103]. The transformer in Fig. 7.2 matches the output voltage of the VSC to the local AC grid requirements and provides galvanic isolation if needed [34]. The main advantage of this proposal with respect to previous HVDC taps based on VSC converters, like those of [100] and [104], is that in this case the high voltage VSC is replaced by a DC/DC converter with a reduced number of components. Since the VSC is directly connected on the low voltage side and referenced to ground, its isolation requirements are greatly reduced with respect to previous solutions [105].

An innovative DC transformer circuit, originally proposed for railway applications in [106] has been studied and adapted for this application. In the following subsectionsthe circuit is studied and a suitable control strategy is developed. The analytical study is complemented by simulation studies.

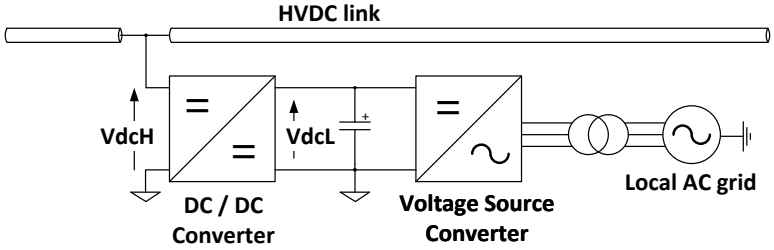


Fig. 7.2 Overall structure of DC/DC converter based HVDC tap.

7.1.1 The cascaded resonant DC transformer circuit

The proposed DC transformer structure is depicted in Fig. 7.3. It relies on the *Marx* generator concept, where a stack of capacitors is sequentially connected in parallel and in series to obtain a voltage multiplication effect [107]. The circuit presents a modular structure. The principal components are a high-voltage valve, *HV valve*, containing series connected self-commutated switches, and a cascaded cell structure. Each of the N cells contains three switches (S_1, S_2 and S_3) plus a capacitor (C_{cell}). The N^{th} cell inside the arm presents a different switch arrangement as shown in Fig. 7.3 to provide the required bi-directional current blocking capability. Integrated in the HVDC tap, the DC transformer performs a voltage reduction from V_{DCH} to V_{DCL}. The converter presents a fixed voltage transformation ratio. Only by increasing or decreasing the number of cells in the arm the ratio can be modified. This relation between the terminal voltages and

the number of cells N is expressed in (7.1):

$$V_{DCL} = \frac{V_{DCH}}{N} \tag{7.1}$$

Where,

- V_{DCL}: DC voltage on the low voltage DC bus (V)
- V_{DCH}: DC voltage on the high voltage DC bus (V)
- N: Number of cells in the DC transformer circuit ($-$)

V_{DCL} presents the same amplitude as the voltage in each individual cell. It is therefore limited by the voltage rating of the cell semiconductors and capacitor. In the tap configuration, the DC/DC converter regulates V_{DCL} by imposing the fixed conversion ratio (7.1) and the VSC converter regulates the active power exchange. Due to its inability to regulate power flow and its fixed voltage ratio, the DC/DC circuit can be identified as the DC equivalent of an AC transformer.

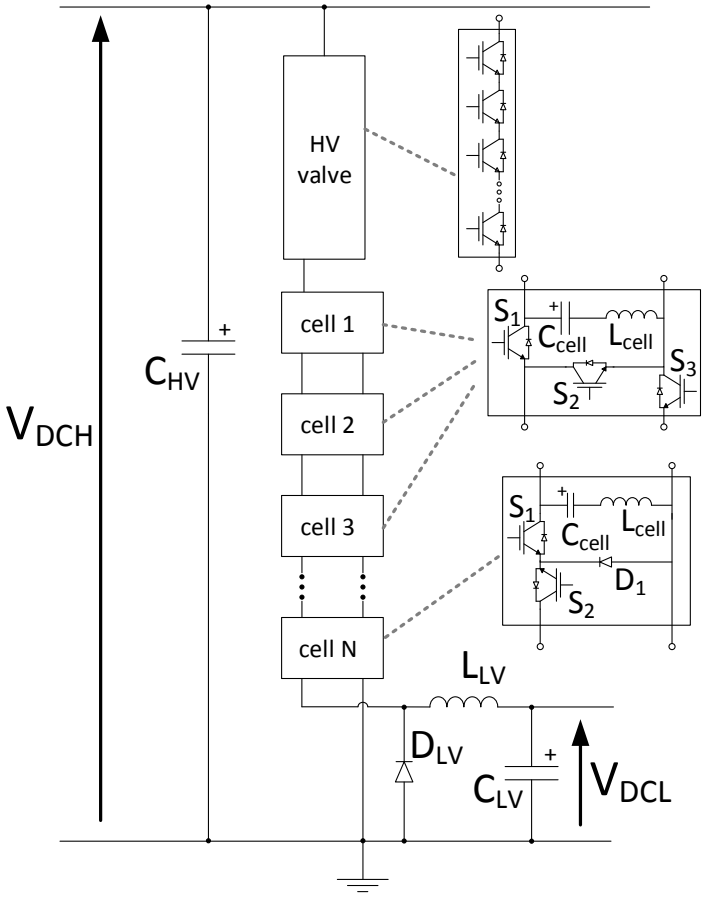
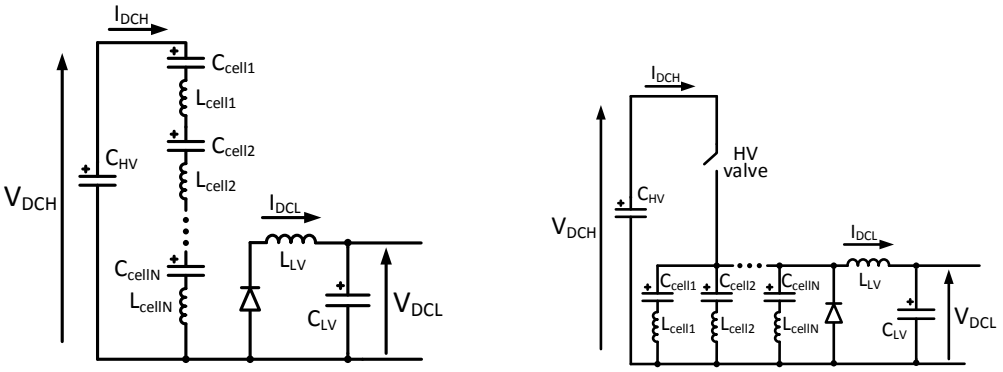


Fig. 7.3 Cascaded resonant DC/DC converter in monopole configuration.

Principle of operation

The two basic switching states of the DC/DC converter are shown in Fig. 7.4. During the first subinterval (Fig. 7.4a), all the cell capacitors are connected in series across the high voltage terminals V_{DCH} and the low voltage terminals are isolated from the main circuit. An energy transfer takes place between the HVDC system and the cell capacitors. During the second subinterval (Fig. 7.4b) the cell capacitors are connected in parallel with the low voltage terminals, and the circuit is isolated from the high voltage terminals by the operation of the *HV valve*. An energy transfer occurs between the cell capacitors and the low voltage capacitance (C_{LV}). Any voltage unbalance in the cell capacitors is naturally equalized with the paralleling during the second subinterval. As described in the following, the DC/DC converter operates in a resonant manner. During the series connection subinterval the cell inductors (L_{cell}) and capacitors (C_{cell}) form a resonant network with the high voltage capacitor (C_{HV}). A second resonant network is formed between the cell inductors and capacitors and low voltage capacitor (C_{LV}) and inductor (L_{LV}) during the parallel connection subinterval. This resonant operation allows for zero current switching (ZCS) of all the semiconductors, minimizing switching losses, hence the overall converter losses.



(a) Series connection of capacitors. (b) Parallel connection of capacitors.

Fig. 7.4 Different HVDC tap configurations.

The circuit switching pattern

For the control of the DC/DC converter, the fixed switching pattern displayed in Fig. 7.5 is used. The two switching subintervals, i.e. series (T_{ser}) and parallel (T_{par}), are sequentially applied during the global switching period T_{sw}. A short duration intermediate state (T_{ZVS}) is added between the two subintervals to achieve zero voltage switching (ZVS) of the HV valve. The summary of each switch commutation state during each subinterval is presented in Table 7.1.

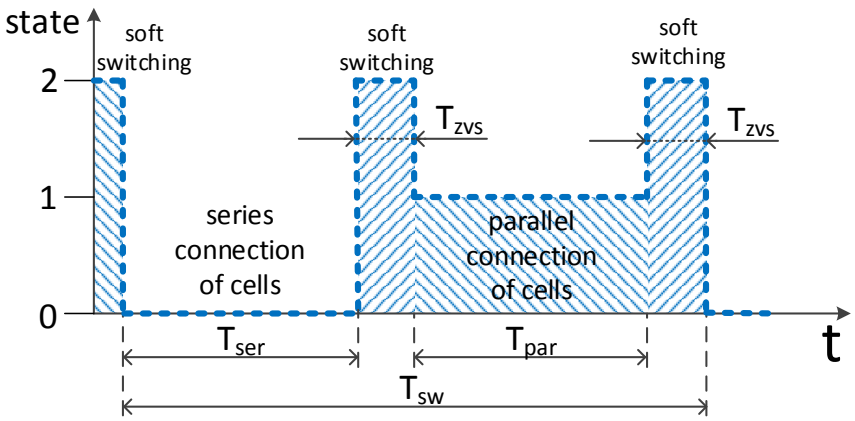


Fig. 7.5 Switching sequence of the DC/DC converter.

Table 7.1 Switching states of the circuit switches.

Subinterval	HV valve	Cells 1..N-1			Cell N	
		S1	S2	S3	S1	S2
T_{ser}	ON	OFF	ON	OFF	OFF	OFF
T_{par}	OFF	ON	OFF	ON	ON	ON
T_{ZVS}	OFF	OFF	ON	OFF	OFF	OFF

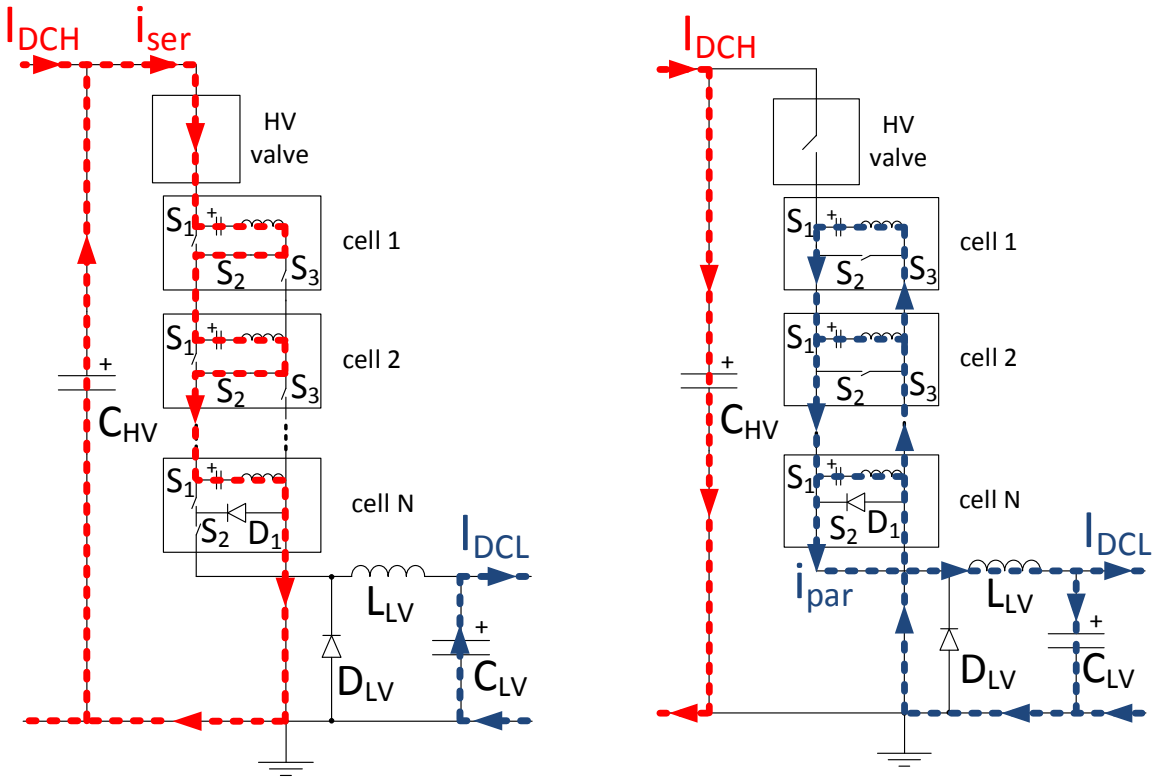
Fig. 7.6a shows the current flow in the circuit during the series subinterval. S_1/S_3 are OFF and S_2 is ON inside cells 1 to N-1. Switches S_1/S_2 in cell N are OFF, isolating the low voltage terminals from the stack of cells. Fig. 7.6b shows the current flow during the parallel subinterval. S_2 is OFF and S_1/S_3 are ON, connecting the cell capacitors in parallel. In cell N, S_1/S_2 are ON, allowing the current flow between the parallel cells and the low voltage DC terminals.

The resonant circuit operation is influenced by the DC currents I_{DCH} and I_{DCL}, which add an offset that modifies the zero current crossing point. The equivalent circuit diagrams for each subinterval are displayed in Fig. 7.7. The equivalent inductance and capacitance values displayed in the diagram are expressed in (7.2), (7.3), (7.4) and (7.5) and the resulting differential equations are presented in (7.6) and (7.7).

$$L_{ser} = N\, L_{cell} \tag{7.2}$$

$$C_{ser} = \frac{C_{cell}}{N} \tag{7.3}$$

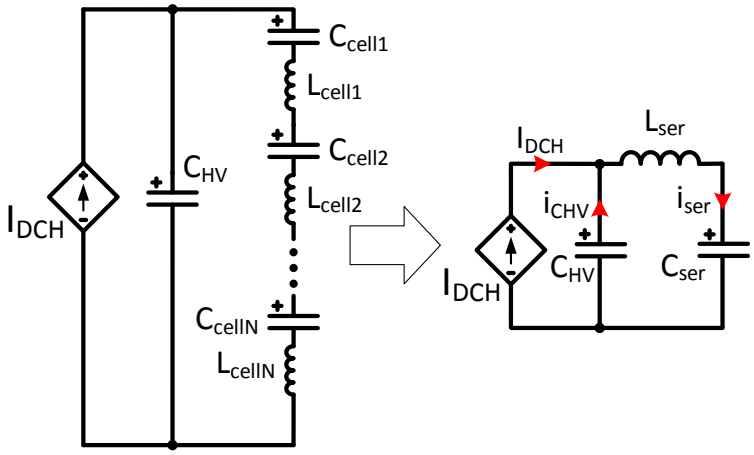
$$L_{par} = \frac{L_{cell}}{N} + L_{LV} \tag{7.4}$$



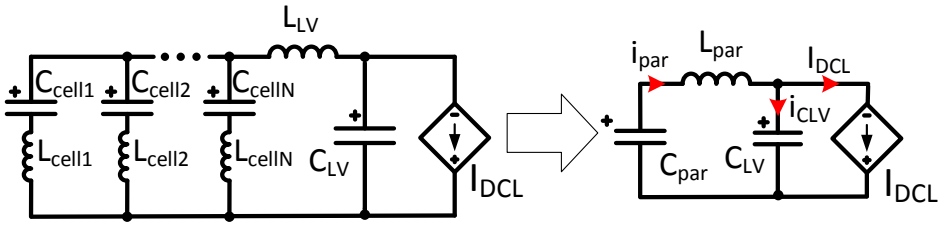
(a) Series connection of cells.

(b) Parallel connection of cells.

Fig. 7.6 Circulation of the currents during the two switching subintervals.



(a) Series connection subinterval.



(b) Parallel connection subinterval.

Fig. 7.7 Equivalent circuits considering effect of DC bus currents.

$$C_{par} = N\, C_{cell} \tag{7.5}$$

$$\frac{d^2\, i_{ser}(t)}{dt^2} + \frac{1}{L_{ser}} \left(\frac{1}{C_{HV}} + \frac{1}{C_{ser}}\right) i_{ser}(t) - \frac{I_{DCH}}{C_{HV}\, L_{ser}} = 0 \tag{7.6}$$

$$\frac{d^2\, i_{par}(t)}{dt^2} + \frac{1}{L_{par}} \left(\frac{1}{C_{LV}} + \frac{1}{C_{par}}\right) i_{par}(t) - \frac{I_{DCL}}{C_{LV}\, L_{par}} = 0 \tag{7.7}$$

Where,

- L_{cell}: Inductance of an individual circuit cell (H)
- L_{ser}: Equivalent inductance during the series connection subinterval (H)
- L_{par}: Equivalent inductance during the parallel connection subinterval (H)
- C_{cell}: Capacitance of an individual circuit cell (F)
- C_{ser}: Equivalent capacitance during the series connection subinterval (F)
- C_{par}: Equivalent capacitance during the parallel connection subinterval (F)
- C_{HV}: Capacitance connected across the high-voltage terminals of the converter (F)
- C_{LV}: Capacitance connected across the low-voltage terminals of the converter (F)
- I_{DCH}: High-voltage DC bus current (A)
- I_{DCL}: Low-voltage DC bus current (A)
- i_{ser}: Resonant current through the cells during the series connection (A)
- i_{par}: Resonant current through the cells during the parallel connection (A)

The resonant current expressions after solving equations (7.6) and (7.7) are shown in (7.8) and (7.9). By properly dimensioning the values of capacitors and inductors in the circuit, the desired resonant periods can be obtained in order to commutate all switches under ZCS.

$$i_{ser}(t) = A_s\, \sin(\omega_{0ser}\, t) + B_s\, \cos(\omega_{0ser}\, t) + C_s \tag{7.8}$$

$$i_{par}(t) = A_p\, \sin(\omega_{0par}\, t) + B_p\, \cos(\omega_{0par}\, t) + C_p \tag{7.9}$$

With:

$$A_s = \sqrt{\frac{C_{HV}\, C_{ser}}{(C_{HV} + C_{ser})\; L_{ser}}}\; (V_{C_{HV0}} - V_{C_{ser0}}) \tag{7.10}$$

$$B_s = -\frac{I_{DCH}\, C_{ser}}{C_{HV} + C_{ser}} \tag{7.11}$$

$$C_s = \frac{I_{DCH}\, C_{ser}}{C_{HV} + C_{ser}} \tag{7.12}$$

$$\omega_{0ser} = \sqrt{\frac{C_{HV} + C_{ser}}{C_{HV}\, C_{ser}\, L_{ser}}} \tag{7.13}$$

$$A_p = \sqrt{\frac{C_{LV}\, C_{par}}{(C_{LV} + C_{par})\; L_{par}}}\; \left(V_{C_{par0}} - V_{C_{LV0}}\right) \tag{7.14}$$

$$B_p = -\frac{I_{DCL}\, C_{par}}{C_{LV} + C_{par}} \tag{7.15}$$

$$C_p = \frac{I_{DCL}\, C_{par}}{C_{LV} + C_{par}} \tag{7.16}$$

$$\omega_{0par} = \sqrt{\frac{C_{LV} + C_{par}}{C_{LV}\, C_{par}\, L_{par}}} \tag{7.17}$$

Where,

- ω_{0ser}: natural frequency of the current during series connection (rad/s)
- ω_{0par}: natural frequency of the current during parallel connection (rad/s)
- $V_{C_{HV0}}$: Initial voltage value for C_{HV} (V)
- $V_{C_{LV0}}$: Initial voltage value for C_{LV} (V)
- $V_{C_{ser0}}$: Initial voltage value for C_{ser} (V)
- V_{Cpar0}: Initial voltage value for C_{par} (V)

In Fig. 7.8 the characteristic resonant current waveforms through the switches are presented. Fig. 7.6a shows how during the series subinterval the same current flows through the HV valve switches and S_2 switches inside the cells. This current is displayed in Fig. 7.8 during T_{ser}. No current flows during the ZVS subintervals (T_{ZVS}), and the commutation of the switches is achieved under ZCS conditions. During the parallel subinterval (T_{par}) on the other hand, switches S_1/S_3 (S_1/S_2 in cell N), are in conduction. Fig. 7.6b shows how the switches in cell 1 conduct the current of their associated cell capacitor. However, the switches from cells

positioned lower in the arm, conduct the current from their associated capacitor but also that of all the modules situated upper in the arm. This is appreciated in Fig. 7.8 during T_{par}, where switches in cell 1 withstand a peak current of amplitude I_{pk}, whereas those in cell N withstand N-times this amplitude . This uneven current rating of the cell switches and a high peak current, particularly in switches situated in the arm lower positions, appear as the main drawbacks of the circuit.

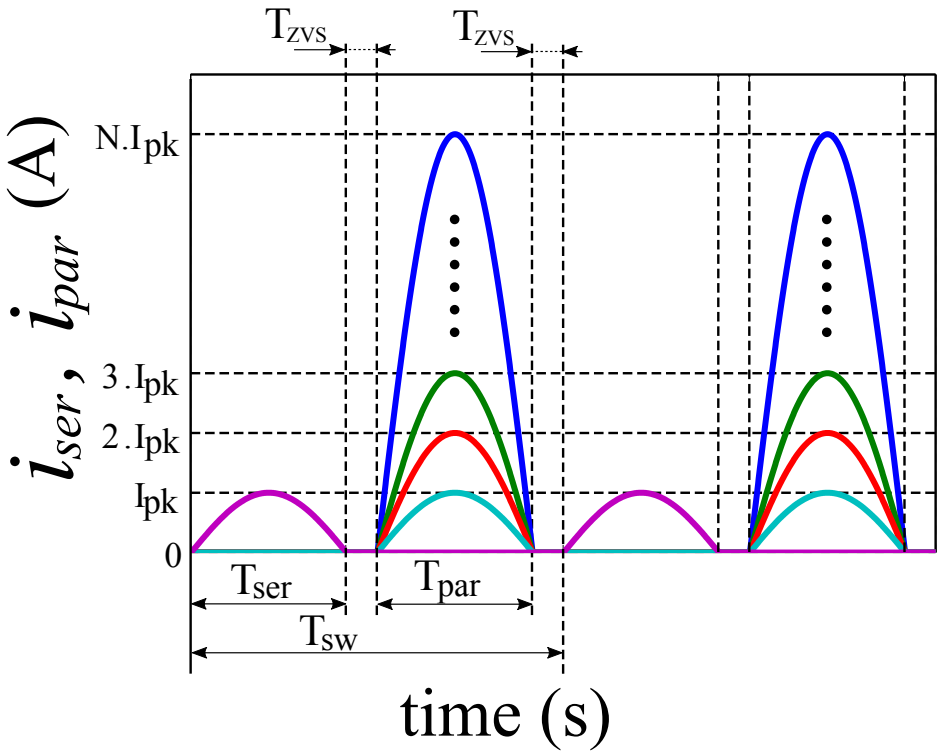


Fig. 7.8 Characteristic of ideal switch currents during the series/parallel subintervals.

Circuit dimensioning

The dimensioning of the circuit components starts by calculating the required values of capacitance for a desired maximum peak to peak voltage ripple. The maximum ripple occurs when the converter is transmitting nominal power (P_{DCn}). The resulting expressions are displayed in (7.18), (7.19) and (7.20):

$$C_{cell} = \frac{P_n\, T_{sw}}{N\, V_{celln}\, \Delta V_{C_{cell}}} \tag{7.18}$$

$$C_{HV} = \frac{P_n\, (T_{sw} - T_{ser})}{V_{DCHn}\, \Delta V_{C_{HV}}} \tag{7.19}$$

$$C_{LV} = \frac{P_n\, (T_{sw} - T_{par})}{V_{DCLn}\, \Delta V_{C_{LV}}} \tag{7.20}$$

Where,

- P_n: Nominal power rating of the converter (W)
- T_{sw}: Switching period of the DC transformer (s)
- T_{ser}: Series connection subinterval of T_{sw} (s)
- T_{par}: Parallel connection subinterval of T_{sw} (s)
- V_{DCHn}: Nominal voltage of the high-voltage DC bus (V)
- V_{DCLn}: Nominal voltage of the low-voltage DC bus (V)
- $\Delta V_{C_{cell}}$: Desired peak-to-peak voltage ripple in C_{cell} (V)
- $\Delta V_{C_{HV}}$: Desired peak-to-peak voltage ripple in C_{HV} (V)
- $\Delta V_{C_{LV}}$: Desired peak-to-peak voltage ripple in C_{LV} (V)

With the capacitors dimensioned, the required cell and low voltage inductor values are calculated to obtain the resonant frequencies that match the desired switching subintervals (T_{ser}/T_{par}). The DC bus currents (I_{DCL}, I_{DCH}) introduce a DC offset in the resonant current expressions (7.8) and (7.9) to be considered when dimensioning the inductors to operate at ZCS. Fig. 7.9 shows this offset. The same problem affects both i_{ser} and i_{par}. In red the ideal resonant current, without accounting for the DC current component, is displayed. In yellow, the real resonant current, when the DC component is considered, is represented. It is observed how the resulting offset delays the current zero crossing point. Therefore expressions (7.13) and (7.17) cannot be directly used to dimension the inductors since the circuit would be operated with $T_{ser/par}$ ideal from Fig. 7.9, whilst i_{real} circulates, causing the circuit to commutate before the resonant current reaches the zero crossing point.

An iterative design process has been used to calculate the required inductor values instead. The initial values of L_{ser} and L_{par} are set using (7.21) and (7.22), obtained from (7.13) and (7.17) for the target values T_{ser}, T_{par}. The iterative process steps are:

1. Refine the value of L_{ser} until i_{ser} from (7.8) at $t = T_{ser}$ is zero.
2. The required cell inductor L_{cell} is then calculated from (7.2).
3. Refine the value of L_{par} until i_{par} from (7.9) at $t = T_{par}$ is zero.
4. The required of inductor L_{LV} is then calculated from (7.4).

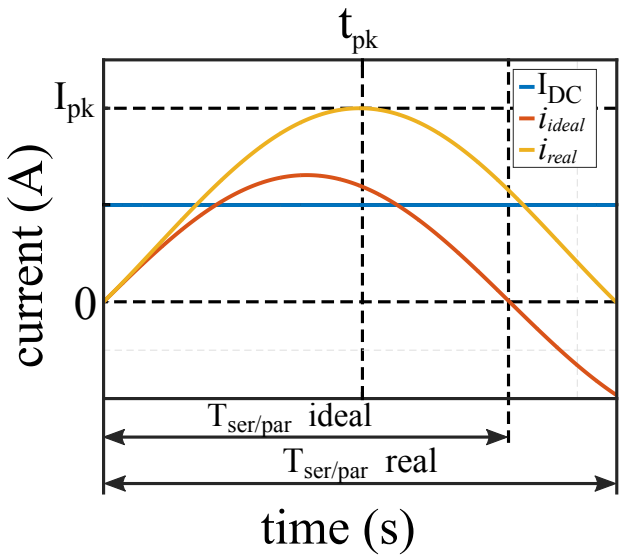


Fig. 7.9 Variation in the resonant subinterval duration introduced by the DC bus current component.

$$L_{ser0} = \frac{T_{ser}^2 \left(N\, C_{HV} + C_{cell}\right)}{4\pi^2\, C_{HV}\, C_{cell}} \tag{7.21}$$

$$L_{par0} = \frac{T_{par}^2 \left(C_{LV} + N\, C_{cell}\right)}{4\pi^2\, N\, C_{LV}\, C_{par}} \tag{7.22}$$

The peak value of the current occurs at time t_{pk} as displayed in Fig. 7.9 which is calculated as:

$$t_{pk,ser} = \frac{1}{\omega_{0ser}} \left(\arctan\left(\frac{A_s}{B_s}\right) + \pi\right) \tag{7.23}$$

$$t_{pk,par} = \frac{1}{\omega_{0par}} \left(\arctan\left(\frac{A_p}{B_p}\right) + \pi\right) \tag{7.24}$$

And replacing time instants (7.23) and (7.24) in (7.8) and (7.9) respectively, the peak amplitudes of the resonant currents during each subinterval ($I_{pk,ser}/I_{pk,par}$) can be calculated.

Zero voltage switching of the HV valve

As seen in Fig. 7.3, the HV valve is made of series connected self commutated switches, typically IGBTs. As expressed in (7.25) the valve withstands almost full HVDC voltage during the parallel subinterval.

$$\hat{V}_{HV_{valve}} = V_{DCH} - v_{cell} \tag{7.25}$$

Where,

- $\hat{V}_{HV_{valve}}$: Peak voltage withstood by HV valve in the DC transformer (V)
- v_{cell}: voltage of a single cell in the DC transformer (V)

Therefore, in a full scale system, the valve is composed of hundreds of switches. Balanced static voltage sharing can be achieved by snubber circuits and grading resistors across each device. However, in order to avoid dynamic voltage sharing problems and complex active gate driving solutions, ZVS of the valve is beneficial. For this reason, as already seen in the circuit switching pattern, intermediate short duration subintervals T_{ZVS} are used. The capability of the cells to modulate the voltage across the HV valve is used to accomplish this task.

Fig. 7.10 illustrates the ZVS process of the valve. In the figure, the values of voltage across the valve (v_{valve}), valve current (i_{valve}) and the gate pulse applied to the valve (S_{gate}) are represented. Starting at T_{par}, with all the cells in parallel connection, the valve gate pulse is low (OFF) and the voltage across the HV valve equals it maximum value expressed in (7.25). At the beginning of the first T_{ZVS} period after T_{par}, the cells are reconfigured into a series connection in preparation for the series subinterval. This immediately reduces the voltage across the valve to a value below v_{cell}, within the voltage rating of an individual switch of the HV valve. At the beginning of T_{ser} the valve is turned ON at this reduced voltage level, avoiding any uneven dynamic voltage distribution.

At the end of T_{ser}, the HV valve is turned OFF while the cells are kept in series connection. In this way, the valve voltage during the turning off process is again kept below the rating of a single switch. The same process is sequentially repeated during each commutation of the HV valve in subsequent switching cycles T_{sw}. The reason why the voltage during both ZVS intervals differs slightly lies in the fact that the state of charge of the cell capacitors differs at the end of each subinterval due to the charging/discharging process.

Control of the HVDC tap

The control structure developed for the tap converters is presented in Fig. 7.11. The DC transformer is unable to regulate the power flow between the two interconnected DC systems as mentioned. Therefore, in the HVDC tap this task is performed by the VSC, together with the regulation of the AC voltage or provision of reactive power support to the local AC grid in case of need. An overall supervisory controller generates the active and reactive power or AC voltage demands (P^*, Q^*/V_{ac}^*) for the VSC controller. The latter can be implemented using the well known synchronous reference frame (d-q) control strategy [108], where the AC current direct and quadrature components are used to decouple the control of active power and reactive power/AC voltage. Standard proportional-integral (PI) controllers can then be used to regulate each of them

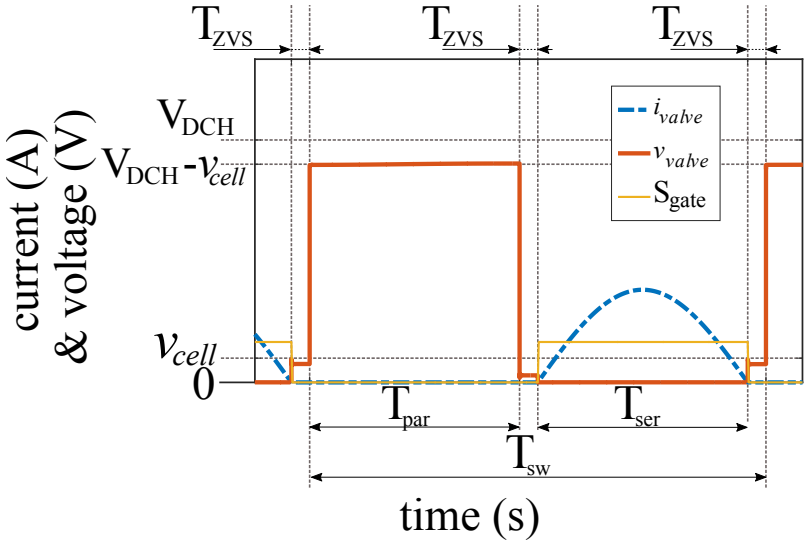


Fig. 7.10 Zero voltage switching of HV valve.

individually. It also generates the references for the switching period (T^*_{sw}) and duration of each subinterval (T^*_{ser},T^*_{par}) for the block implementing the fixed switching pattern described in previous subsections. Communication between the supervisory controller and the HVDC stations and other elements of the AC grid can also be implemented. This might be needed to synchronize the operation of the HVDC tap with the HVDC link during start-up/shut down sequences or the implementation of fault protection strategies.

Simulation studies

The model of the system presented in Fig. 7.12 is used to validate the analytical study of the DC transformer circuit. The values of the circuit components and controller parameters are specified in Table 7.2. Capacitors C_{HV} and C_{LV} are dimensioned for a 3 % peak-to-peak voltage ripple using (7.19) and (7.20). The cell capacitor is dimensioned for a 10 % ripple instead using (7.18). By using the proposed iterative method L_{cell} and L_{LV} values are refined to obtain ZCS at the end of the proposed subintervals T_{ser} and T_{par}.

The low voltage side current source emulates a VSC station and starts ramping up the power at t=0 seconds until 2 MW of power are transmitted from the high-voltage into the low-voltage DC bus. At t=0.5 seconds, the power flow is reversed. In Fig. 7.13c the power measured in both low and high voltage DC terminals is displayed. As observed, even if the DC transformer circuit does not have direct control over the transferred power, the successive series/parallel reconfiguration of the circuit allows to track correctly the power flow imposed by the VSC station (P LV port). In Figs. 7.13a and 7.13b the zoomed view of voltage and current at the tap DC terminals are displayed in order to appreciate the ripple. The voltage ripple in C_{HV} and C_{LV} corresponds to the desired 3%

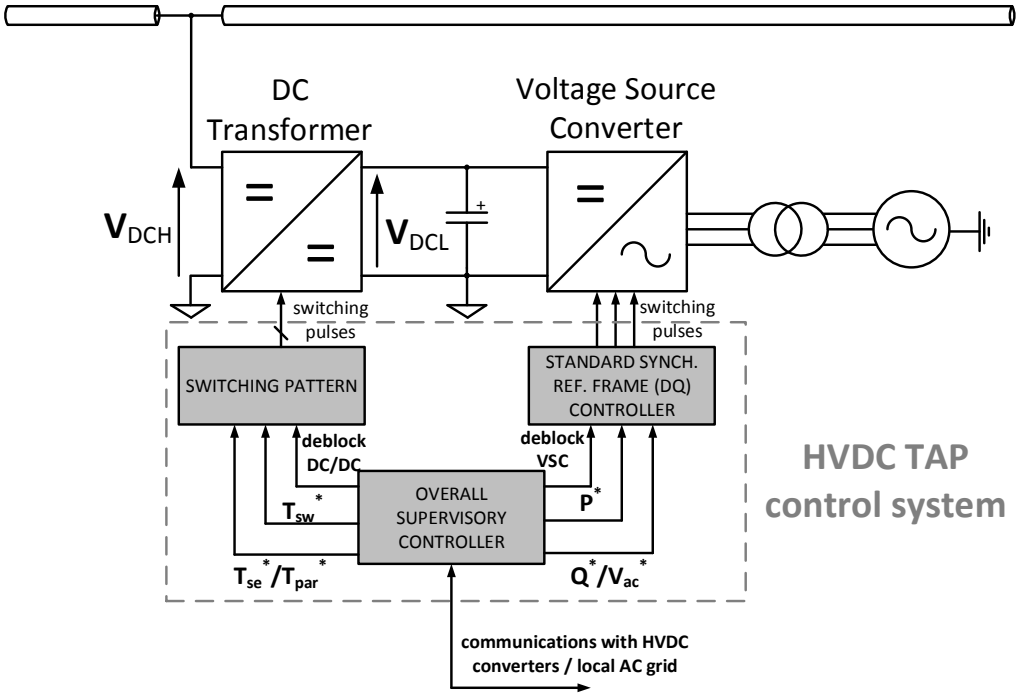


Fig. 7.11 Controller structure for the HVDC tap.

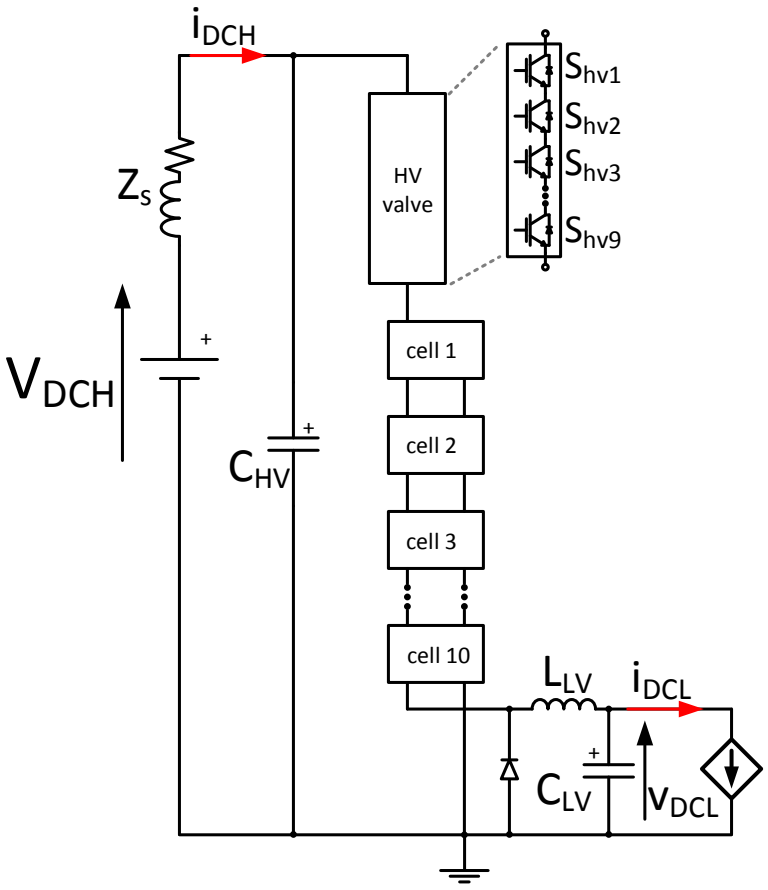


Fig. 7.12 HVDC tap simulation model.

Table 7.2 System parameters for the HVDC tap simulation model.

Parameter	Symbol	Value
Nominal tap power	P_n	2 MW
HVDC bus voltage	V_{DCH}	30 kV
LVDC bus voltage	V_{DCL}	3 kV
Number of cells	N	10
Number of HV valve switches	N_{HV}	9
Cell capacitance	C_{cell}	122 μF
HV capacitance	C_{HV}	25.9 μF
LV capacitance	C_{LV}	1.85 mF
Cell inductance	L_{cell}	44.2 μH
LV inductance	L_{LV}	5.8 μH
Global switching period	T_{sw}	550 μs
Series subinterval	T_{ser}	200 μs
Parallel subinterval	T_{par}	300 μs
ZVS subinterval	T_{ZVS}	25 μs

value. The naturally achieved balance of the cell capacitor voltages is observed in Fig. 7.13d. The desired 10% ripple used for dimensioning is also achieved. In Fig. 7.13e, the detail of the resonant currents during the series (top plot) and parallel (bottom plot) subintervals are displayed. The results validate the proposed iterative method for dimensioning the cell and low voltage inductors to achieve ZCS at the end of both series and parallel subintervals.

7.2 The HVDC tap with dynamic braking capability

The circuit presented in section 7.1 for the implementation of an HVDC tap has a limited capability to divert power from the DC link. The main limiting factor is the magnitude of the currents circulating through the DC transformer, particularly during the parallel connection subinterval, which exceed the ratings of available semiconductor devices when the power is increased beyond a few megawatts. Such tap converter is useful to supply remote and isolated loads but lacks the high power rating required for the implementation of dynamic braking systems to provide fault ride-through capability to big HVDC connected wind farms. But even if the circuit currents could be kept down to levels manageable by the semiconductors, and such tap converter with high power diverting capability could be built, a second problem resides in the low voltage system. Dimensioning the receiving low voltage end (AC grid, energy storage system, etc) for an instantaneous power rating of hundreds of megawatts but to absorb a relatively small amount of energy during the rather infrequent fault ride-through events,

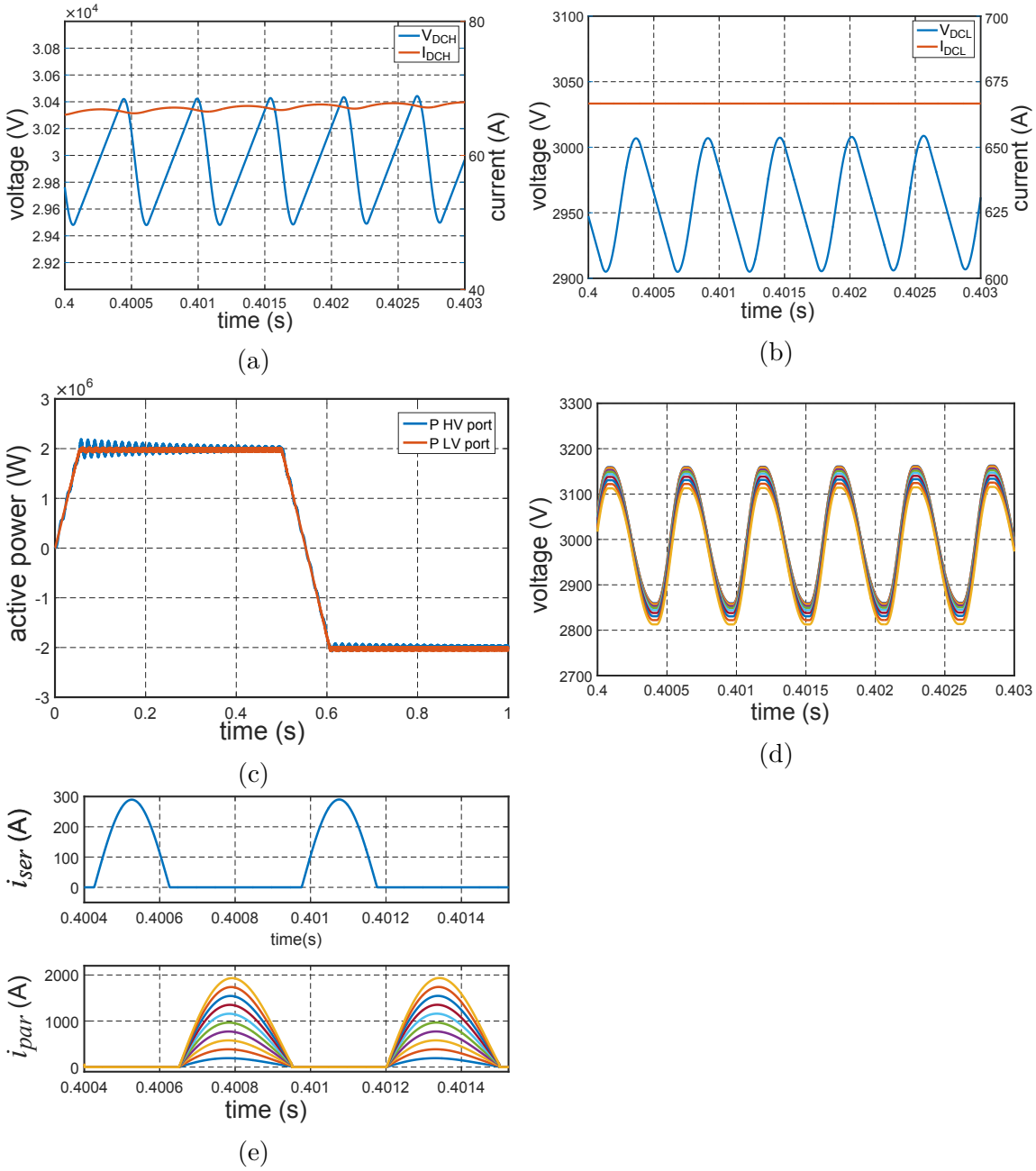


Fig. 7.13 Simulation results for the resonant DC transformer in monopole configuration.

would be both technically challenging and economically unattractive. In this section a solution to merge both the DC transformer functionality with the dynamic braking capability is studied.

7.2.1 The modified cascaded resonant DC transformer circuit

Fig. 7.14 presents a modification of the DC transformer circuit which adds the missing capability to operate as a dynamic braking system. Re-using the *multilevel chopper DBS* circuit concept presented in Chapter 3, a distributed braking resistor (R_{dbs}) in series with a switch (S_4) is added to each of the cells of the DC transformer. This distributed chopper circuit is connected across the capacitor inside each cell (C_{cell}).

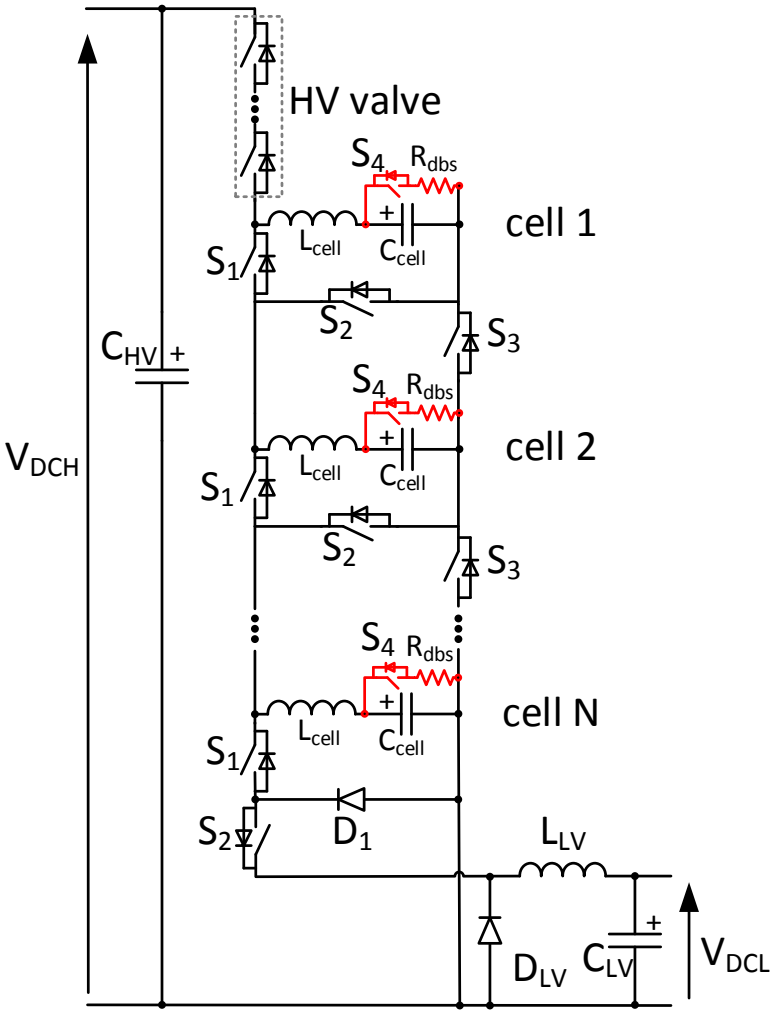


Fig. 7.14 Cascaded resonant DC transformer integrating dynamic braking functionality.

The circuit can operate as a DC/DC converter during normal operation of the

tap system, and switch to the energy dissipation mode when required. The low voltage DC grid or interconnected AC grid are in this way supplied from the tap converter under normal operation, without having to be dimensioned to absorb a large amount of power during a dynamic braking event.

The circuit dimensioning follows the same principles presented in section 7.2.1. The required value of the distributed braking resistor, as derived in section 3.3.2, is:

$$R_{dbs} = \frac{(V_{DCH}\, UOVL)^2}{P_{DCn}\, N} \tag{7.26}$$

Where,

- $UOVL$: Upper over-voltage limit defined in Chapter 3 (pu)
- P_{DCn}: Nominal power of the HVDC system (W)

The single required addition to the control structure of the DC transformer circuit (Fig. 7.11) is the block diagram displayed in Fig. 7.15. This structure generates the switching pulses to control the chopper circuit switches (S_4) inside each cell when the energy dissipation mode is entered in the event of an over-voltage in V_{DCH}.

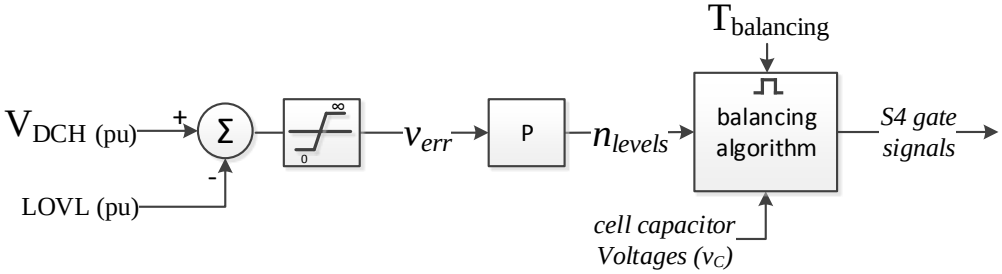


Fig. 7.15 Additional control function for the DC transformer integrating dynamic braking.

The gain value for the proportional controller is:

$$k_p = \frac{N}{UOVL - LOVL} \tag{7.27}$$

Simulation studies

To validate the operation of the proposed HVDC tap integrating dynamic braking functionality a simulation model was built reusing the system parameters from Table 7.2. The circuit power ratings, distributed resistance value and DBS operation voltage thresholds are displayed in Table 7.3.

The simulation results are displayed in Fig. 7.16. The circuit starts operation as an HVDC tap, transferring 2 megawatts of power. At t=0.4 seconds V_{DCH}

Table 7.3 Additional parameters for the HVDC tap+DBS simulation model.

Parameter	Symbol	Value
Nominal power for tap operation	P_n	2 MW
Nominal HVDC system power	P_{DCn}	30 MW
Distributed braking resistance	R_{dbs}	3.63 Ω
Lower over-voltage limit	$LOVL$	1.05 pu
Upper over-voltage limit	$UOVL$	1.1 pu

starts raising as the result of a fault ride-through event. Once the voltage crosses the LOVL threshold (31.5 kV), the operation in tap mode is halted, the power transferred to the low voltage DC terminals falls to zero and the distributed choppers enter operation to start dissipating power. Fig. 7.16c displays the evolution of the DC power measured at both tap circuit terminals. Fig. 7.16d shows the total power dissipation in the distributed braking resistors. As observed, the circuit operates correctly from the moment LOVL is crossed until UOVL is reached (33 kV), gradually increasing the power dissipation in the braking resistors until the power dissipation reaches 30 MW. Figs. 7.16a and 7.16b display the evolution of voltage and current in both DC ports during tap and dynamic braking operation. The cell capacitor voltages are plotted in Fig. 7.16e and the semiconductor currents during both series and parallel subintervals are displayed in Fig. 7.16f. The top graph shows the current during the series subinterval (i_{ser}) which flows through the HV valve and switch S2 inside each cell. As observed, during the DBS operation i_{ser} reaches the value of the HVDC system current ($P_{DCn}/V_{DCH} = 30MW/33kV = 910A$) . In a full scale system (900 MW, 640 kV) this value will stay below 1.5 kA, well within the capability of existing IGBTs, and therefore the integration of the DBS functionality in the HVDC tap circuit would not pose any major challenge.

These results validate the feasibility of a hybrid circuit combining both HVDC tapping functionality for supplying remote loads in the vicinity of HVDC transmission systems, with dynamic braking (DBS) capability to support the HVDC system during fault events.

7.3 Summary of the chapter

The DBS circuits presented in Chapter 3 are needed in HVDC connections when FRT capability is to be provided within the DC link. Although the integration of a DBS solution is usually requested by the TSOs, it represents a significant investment for a converter which spends a large part of the time inactive. With the objective of better justifying the investment in such converter, this chapter explores the integration of additional functionality, which can be performed by

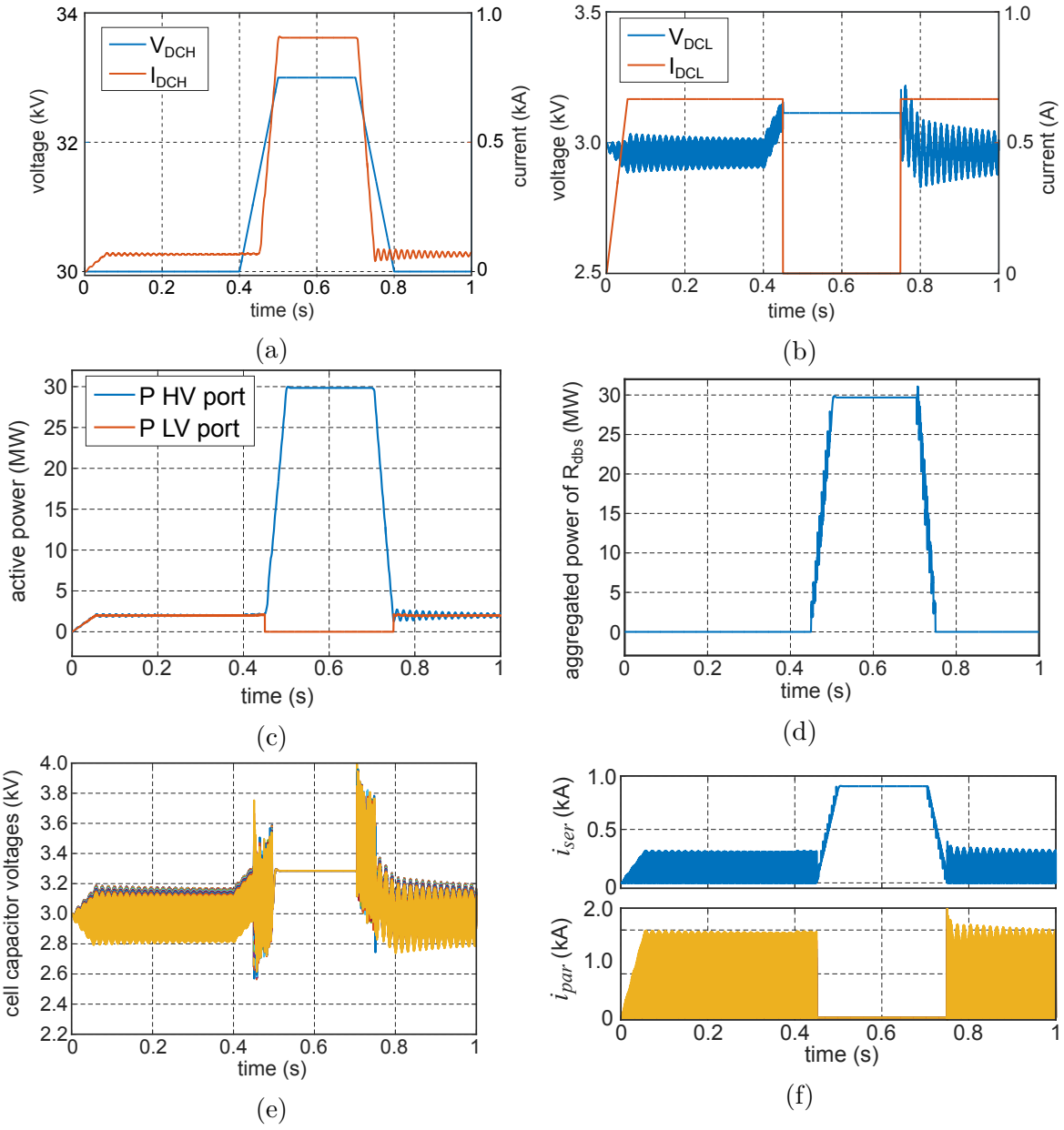


Fig. 7.16 Simulation results for the resonant DC transformer in monopole configuration.

the converter during those long inactivity periods.

The concept of HVDC tapping has been explored in this chapter. These converters are capable of diverting a small fraction of the HVDC link power into a secondary grid, load or energy storage system. The cascaded resonant DC transformer circuit studied in section 7.1 performs a DC/DC conversion to step-down the HVDC voltage to LVDC or MVDC levels, whereas an AC/DC converter of VSC type provides the interface with the secondary grid or energy storage system. The main limitation of the circuit is its relatively small power rating when compared to the nominal power of the HVDC link due the high currents flowing through the semiconductor switching during the circuit operation.

A solution to this limitation is developed in section 7.2 with a modification of the DC transformer circuit. The energy diverting capability of the HVDC taps is combined with resistive power dissipation like in a DBS by adding a distributed chopper circuit inside each cell of the DC transformer. This permits to boost the circuit's power absorption capability without affecting the current rating of the semiconductors, in order to make it suitable for dissipation of nominal HVDC link power during a fault ride-through event.

The validity of the control principle and component sizing proposed for the two converters has been validated with the simulation results presented.

Chapter 8

Conclusions and recommendations for further work

8.1 Conclusions

The review of fault ride-through methods for HVDC connected offshore wind farms revealed that despite some alternatives proposed in literature, onshore energy dissipation circuits, know as Dynamic Braking Systems (DBS), are widely accepted as the most robust solution and mostly a requirement from grid operators. A lack of published research dealing with their practical implementation and control systems was also observed. Most publications consider the DBS as an ideal high-level function that absorbs power as required to mitigate the DC over-voltage, and the major drawback commonly associated with them is the cost. Based on this the research was organized around two main areas: the detailed study of different implementations of DBS circuits and the development of energy diverting converters (EDC) to help justifying the DBS cost by adding extra functionality.

In the thesis four alternative DBS circuits are studied. The first two circuits are based on the conventional braking chopper concept as used in motor drives whereas the other two circuits are implemented as controlled voltage sources with modular multilevel converter (MMC) type cells. The expressions for the sizing of passive components are derived and a dedicated control scheme is developed for each circuit. The simulation and experimental results conclude that the four circuits can reliably provide fault ride-through capability by keeping the DC over-voltage within desired limits. The method to emulate the AC faults in the experimental platform based on contactors and resistors has been found to affect the operation of the VSC converters, resulting in DC overvoltages occurring at

the end of the fault when the contactors operate, despite the correct operation of the DBS circuits. To eliminate this problem it would be recommended to replace the current circuit arrangement by an electronic power supply which can be controlled to reduce the amplitude of the AC grid voltage at the terminals of the onshore VSC station in order to emulate faults of different magnitudes. Despite this problem, the experimental platform also shows that a hardware implementation of the control algorithms is successful and the energy balancing functions perform correctly under the non-linearities and quantization effects introduced by the digital controllers and the tolerances of real passive components and semiconductors. While the HVDC chopper and the multilevel chopper provide a straightforward way of controlling the power dissipation by employing high frequency square voltage pulses across the braking resistors, the modular circuits based on MMC cells require a more complex modulation to regulate the power. The two developed trapezoidal modulations have proven successful in achieving a fine power regulation while naturally keeping the energy balance in the cells. The use of trapezoidal pulses with a controlled voltage derivative offers better EMC performance with respect to the HVDC chopper. However it also increases the voltage and current rating of the semiconductors and the braking resistor. Together with the larger required number of semiconductors makes both MMC cell based circuits the least attractive solution for the implementation of DBS circuits. The multilevel chopper presents the best operational performance thanks to the very low ripple in the current absorbed from the HVDC link, which also produces the lowest voltage ripple in the HVDC link of all the four circuits. In terms of required number of semiconductors, it is the second best alternative behind the multilevel chopper, but it also achieves the lowest switching frequency. Together with the HVDC chopper, it offers the best performance in terms of required current rating of semiconductor switches and braking resistors. On the whole the multi-level chopper represents the best solution for the implementation of a DBS function.

The driving force to explore MMC cell based circuits was the benefit of sharing the same building block for both VSC stations and DBS circuits and presents additional advantages. For example, the full-bridge circuit, thanks to its capability to generate an arm voltage of either polarity, is the only solution that can be implemented straightforward in LCC type HVDC schemes.

The second area of interest for this work was the implementation of extra functionality in DBS circuits, where the combination of the HVDC tapping with the DBS functionality was investigated. An innovative DC-DC converter concept based on the Marx generator principle is developed for the implementation of an HVDC tap and a suitable control principle is developed. In view of the simulation results, the main drawback with the proposed topology is an uneven current rating

of the different cells, which limits the maximum power rating of the tap converter to values below 10 MW. With the addition of a local chopper inside each of the DC-DC converter cells the converter can behave like a multilevel chopper DBS for energy dissipation during the fault. In this way the desired multi-functionality with a DBS circuit is obtained. It is therefore demonstrated that with this EDC it is possible to permanently divert a small fraction of the power flowing through the HVDC link to supply small loads or remote communities nearby an HVDC link and also to increasing the power absorption capability to the nominal rating of the HVDC during a fault event.

8.2 Recommendations for further work

The work presented in this thesis could encourage further research is some very promising applications of power electronics in future HVDC grids. Some ideas are presented here.

The primary goal of the thesis was to to study the use of dynamic braking systems to provide fault ride-through during AC grid fault events. However, they could have the potential to support the transmission system during DC faults, which merits a more in depth study. For instance, during a pole-to-ground fault in symmetrical monopolar systems, the DBS could be used to limit the subsequent over-voltage in the non-faulted pole by discharging the energy stored in the DC capacitance. Furthermore, the DBS could help the restart of the DC grid after the fault, by discharging the DC cables prior to re-energising the system. In addition, the concept of the energy diverting converter could be further extended by proposing other functionalities besides the two explored in this work.

The intermittence of renewable energy sources is a well know drawback which challenges network operators to ensure the electrical system stability. From an economic perspective, the development of an energy storage solution to operate exclusively during the fault ride-through event is not very attractive. The converter and the storage elements need to be rated for a very high instantaneous power, but due to the short duration of the faults events, the recovered energy is relatively low. Future advances in storage technologies could however enable a bulk storage implementation to provide the fault ride-through capability as well a load balancing function for the grid, storing energy from the wind farms when demand is low to be later re-injected during consumption peaks. Battery or super-capacitor based storage could be added within the onshore VSC cells eliminating in this way the need for an additional dedicated converter. This same concept could be equally explored to provide virtual inertia to ensure the stability in future grids, where a large portion of synchronous generation might be replaced by power electronics.

At last, the HVDC tap converter concept, briefly investigated in this work, is an application that arouses great interest in industry at present. Further research in this topic should focus on obtaining a solution that performs the task in a simple but cost-effective manner. The reliability of the solution must also be analysed in great detail. Novel concepts for series connected taps should be considered as a promising direction to address these challenges.

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Appendix A

Derivations for the modulation strategy in half and full bridge DBS circuits

This appendix includes the derivation of the valve energy and average power dissipation expressions for the different modulation regions presented in sections 3.4 and 3.5 of chapter 3.

A.1 Expressions for full power dissipation with half-bridge circuit

A first set of equations is needed to characterize the modulation strategy at nominal power dissipation. The trapezoidal modulation period T_m is divided into six different subintervals (T_1..T_6) to be analysed individually, as shown in Fig. A.1.

T_1 / T_3 subintervals

Fig. A.1a shows that during these two subintervals the DBS valve voltage changes from V_{DC} to zero with the same constant voltage derivative dv/dt, and therefore from the power and energy calculation perspective the two can be considered equivalent. Thus the expressions only need to be calculated for one of them. By making the equivalence:

$$T_1 = T_3 = \frac{V_{DC}}{dv/dt} \tag{A.1}$$

the expressions for the DBS valve voltage, valve current, valve power and

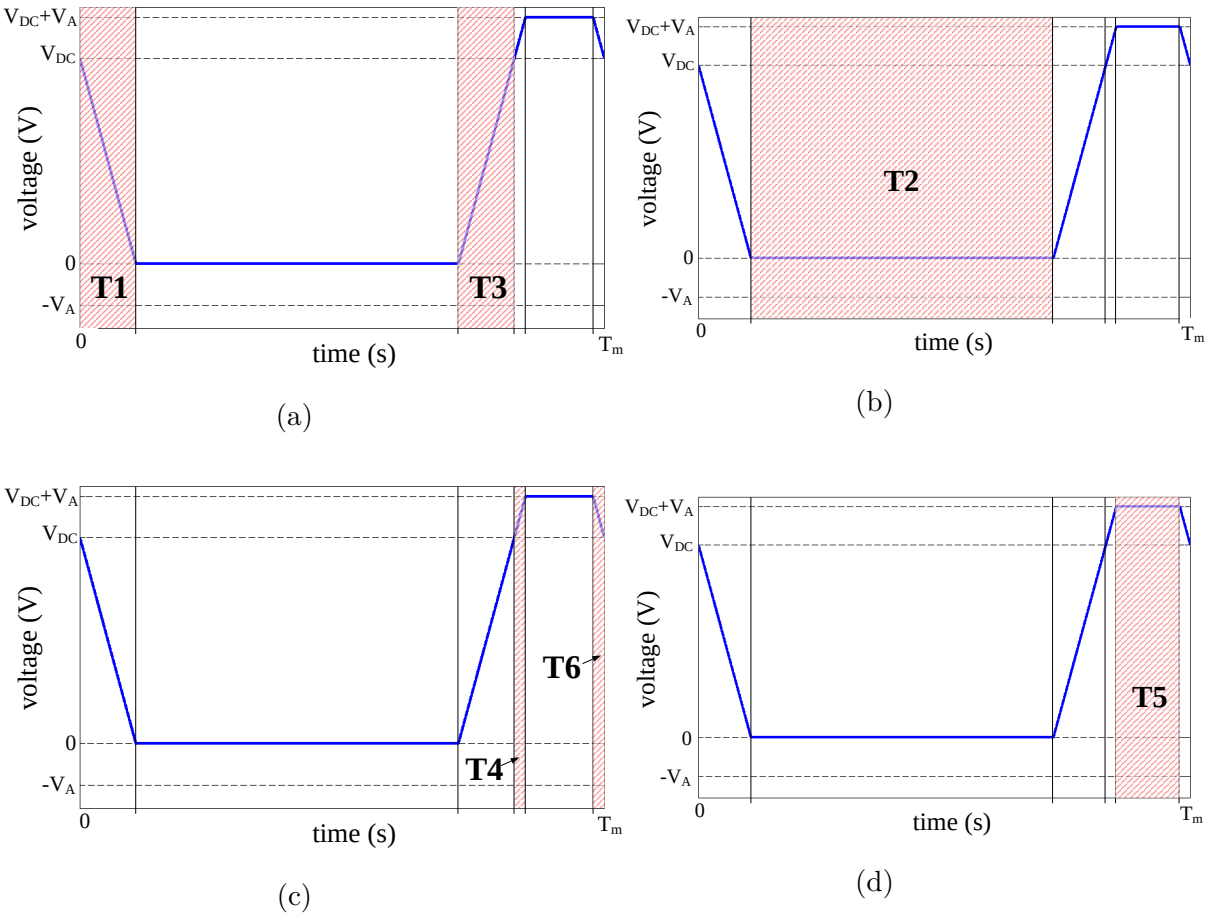


Fig. A.1 Different regions for trapezoidal modulation analysis in half-bridge multilevel DBS: nominal power dissipation.

valve energy variation are:

$$v_{valveT1} = V_{DC} - \frac{V_{DC}\, t}{T_1} = V_{DC} - t\, dv/dt \tag{A.2}$$

$$i_{dbsT1} = \frac{V_{DC}\, t}{R_{dbs}\, T_1} = \frac{t\, dv/dt}{R_{dbs}} \tag{A.3}$$

$$p_{valveT1} = v_{valveT1}\, i_{dbsT1} = \frac{t\, dv/dt\ (V_{DC} - t\, dv/dt)}{R_{dbs}} \tag{A.4}$$

$$\Delta E_{valveT1} = \int_0^{T_1} p_{valveT1}\, dt = \frac{{V_{DC}}^3}{6\, R_{dbs}\, dv/dt} \tag{A.5}$$

To calculate the average power dissipation in the braking resistor over a modulation period, the resistor power in the different regions needs to be integrated to obtain the energy expression $E_R = \int \frac{v_R^2}{R_{dbs}}\, dt$. Knowing that

$v_R = V_{DC} - v_{valve}$, then:

$$E_{RT1} = \frac{{V_{DC}}^3}{3\,R_{dbs}\,dv/dt} \tag{A.6}$$

$\mathbf{T_2}$ subinterval

Fig. A.1b shows subinterval T_2, where it can be appreciated that the arm voltage during this period equals zero, since all the voltage is applied across the braking resistor. Hence during this subinterval no energy is stored or released in the DBS valve:

$$\Delta E_{valveT2} = 0 \tag{A.7}$$

There is however power being dissipated in the resistor, and the energy expression is:

$$E_{RT2} = \frac{{V_{DC}}^2\,T_2}{R_{dbs}} \tag{A.8}$$

$\mathbf{T_4}$ / $\mathbf{T_6}$ subintervals

In this case (Fig. A.1c) both subintervals are also equivalent, and calculations are only required for one of them. Additionally, considering a constant dv/dt value during the circuit operation:

$$T_4 = T_6 = \frac{V_A}{dv/dt} \tag{A.9}$$

the resulting expressions are:

$$v_{valveT4} = V_{DC} + \frac{V_A\,t}{T_4} = V_{DC} + t\,dv/dt \tag{A.10}$$

$$i_{dbsT4} = \frac{-V_A\,t}{R_{dbs}\,T_4} = -\frac{t\,dv/dt}{R_{dbs}} \tag{A.11}$$

$$p_{valveT4} = v_{valveT4}\,i_{dbsT4} = -\frac{t\,dv/dt\ (V_{DC} + t\,dv/dt)}{R_{dbs}} \tag{A.12}$$

$$\Delta E_{valveT4} = \int_0^{T_4} p_{valveT4}\,dt = -\frac{2\,{V_A}^3 + 3\,V_{DC}\,{V_A}^2}{6\,R_{dbs}\,dv/dt} \tag{A.13}$$

and the energy in the braking resistor:

$$E_{RT4} = \frac{{V_A}^3}{3\,R_{dbs}\,dv/dt} \tag{A.14}$$

T_5 subinterval

The expressions for this last subinterval (Fig. A.1d) are:

$$v_{valveT5} = V_{DC} + V_A \tag{A.15}$$

$$i_{dbsT5} = -\frac{V_A}{R_{dbs}} \tag{A.16}$$

$$p_{valveT5} = v_{valveT5}\, i_{dbsT5} = -\frac{V_A\ (V_A + V_{DC})}{R_{dbs}} \tag{A.17}$$

$$\Delta E_{valveT5} = \int_0^{T_5} p_{valveT5}\, dt = -\frac{V_A\ (V_A + V_{DC})\ T_5}{R_{dbs}} \tag{A.18}$$

with the energy across the braking resistor:

$$E_{RT5} = \frac{{V_A}^2\, T_5}{R_{dbs}} \tag{A.19}$$

As observed from expressions (A.13) and (A.18), during the subintervals where the DBS valve discharges energy, one part of this energy is dissipated in the braking resistor and the remaining is re-injected in the DC link, to be later re-absorbed during the next modulation period.

A.2 Expressions for amplitude modulation with half-bridge circuit

In this section the equations to characterize the trapezoidal modulation for the amplitude modulation region are derived. Fig. A.2 shows the trapezoidal voltage waveform with the different time subintervals to consider for this analysis.

T_1 / T_3 subintervals

Fig. A.2a shows these subintervals. As in previous sections, equivalent subintervals are considered in order to simplify the calculations:

$$T_1 = T_3 = \frac{V_B}{dv/dt} \tag{A.20}$$

The expressions for the DBS valve voltage, current, power and energy variation are:

$$v_{valveT1} = V_{DC} - \frac{V_B\, t}{T_1} = V_{DC} - t\, dv/dt \tag{A.21}$$

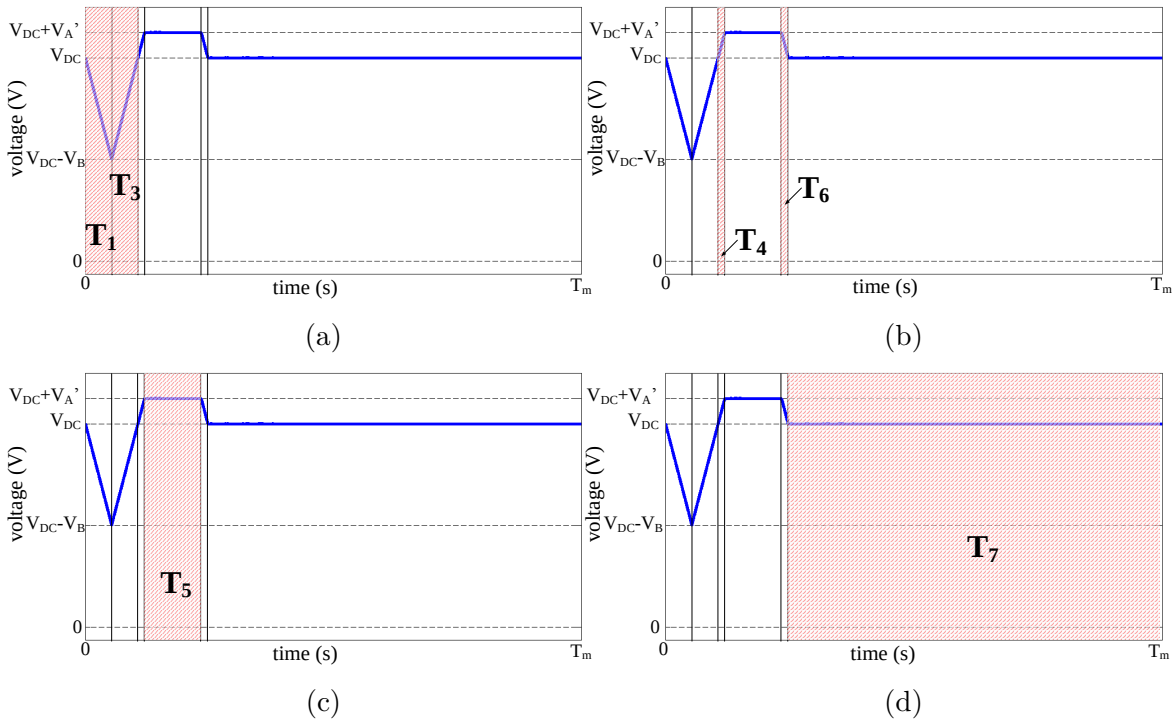


Fig. A.2 Different regions for trapezoidal modulation analysis in half-bridge multilevel DBS: amplitude modulation region.

$$i_{dbsT1} = \frac{V_B\, t}{R_{dbs}\, T_1} = \frac{t\, dv/dt}{R_{dbs}} \tag{A.22}$$

$$p_{valveT1} = v_{valveT1}\, i_{dbsT1} = \frac{t\, dv/dt\ (V_{DC} - t\, dv/dt)}{R_{dbs}} \tag{A.23}$$

$$\Delta E_{valveT1} = \int_0^{T_1} p_{valveT1}\, dt = -\frac{{V_B}^2\ (2\, V_B - 3\, V_{DC})}{6\, R_{dbs}\, dv/dt} \tag{A.24}$$

And the energy dissipated in the braking resistor:

$$E_{RT1} = \frac{{V_B}^3}{3\, R_{dbs}\, dv/dt} \tag{A.25}$$

$\mathbf{T_4}$ / $\mathbf{T_6}$ subintervals

In this case (Fig. A.2b), the following equivalence is also defined:

$$T_4 = T_6 = \frac{V'_A}{dv/dt} \tag{A.26}$$

and the resulting expressions are:

$$v_{valveT4} = V_{DC} + \frac{V'_A\, t}{T_4} = V_{DC} + t\, dv/dt \tag{A.27}$$

$$i_{dbsT4} = \frac{-V'_A\, t}{R_{dbs}\, T_4} = -\frac{t\, dv/dt}{R_{dbs}} \tag{A.28}$$

$$p_{valveT4} = v_{valveT4}\, i_{dbsT4} = -\frac{t\, dv/dt\ (V_{DC} + t\, dv/dt)}{R_{dbs}} \tag{A.29}$$

$$\Delta E_{valveT4} = \int_0^{T_4} p_{valveT4}\, dt = -\frac{{V'_A}^2\ (2\, V'_A + 3\, V_{DC})}{6\, R_{dbs}\, dv/dt} \tag{A.30}$$

and the energy in the braking resistor:

$$E_{RT4} = \frac{{V'_A}^3}{3\, R_{dbs}\, dv/dt} \tag{A.31}$$

T_5 subinterval

The expressions for this subinterval (Fig. A.2c) are:

$$v_{valveT5} = V_{DC} + V'_A \tag{A.32}$$

$$i_{dbsT5} = -\frac{V'_A}{R_{dbs}} \tag{A.33}$$

$$p_{valveT5} = v_{valveT5}\, i_{dbsT5} = -\frac{V'_A\ (A' + V_{DC})}{R_{dbs}} \tag{A.34}$$

$$\Delta E_{valveT5} = \int_0^{T_5} p_{valveT5}\, dt = -\frac{V'_A\ (V'_A + V_{DC})\ T_5}{R_{dbs}} \tag{A.35}$$

and the energy across the braking resistor:

$$E_{RT5} = \frac{{V'_A}^2\, T_5}{R_{dbs}} \tag{A.36}$$

T_7 subinterval

As shown in Fig. A.2d, this is the last subinterval to complete the trapezoidal modulation period. The voltage generated by the braking valve equals the HVDC pole voltage, therefore there is no current flowing through the arm, and no energy is stored in the DBS arm or dissipated in the resistor.

$$\Delta E_{valveT7} = 0 \tag{A.37}$$

$$E_{RT7} = 0 \tag{A.38}$$

A.3 Expressions for full power dissipation with full-bridge circuit

As before, the set of equations to characterize the modulation strategy to dissipate HVDC nominal power are presented here. The trapezoidal pulse is divided into six different subintervals to perform an individual analysis in each of them, as shown in Fig. A.3.

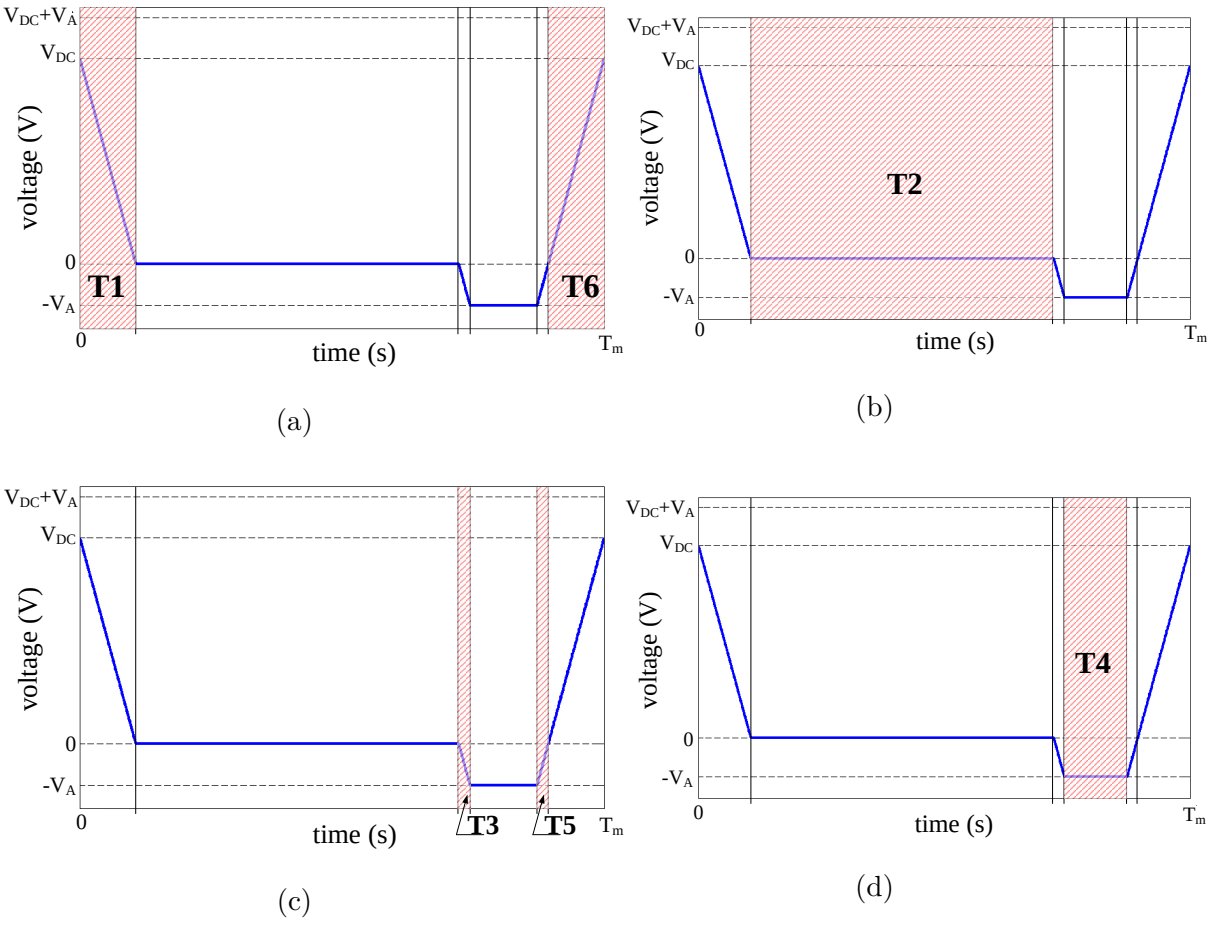


Fig. A.3 Different regions for trapezoidal modulation analysis in full-bridge multilevel DBS.

$\mathbf{T_1}$ / $\mathbf{T_6}$ subintervals

The two subintervals are equivalent, as can be seen in Fig. A.3a, with the valve voltage changing between V_{DC} and zero with constant dv/dt. Therefore, the subintervals duration can be expressed as:

$$T_1 = T_6 = \frac{V_{DC}}{dv/dt} \tag{A.39}$$

The expressions for the valve voltage, current, power and energy variation are:

$$v_{valveT1} = V_{DC} - \frac{V_{DC}\, t}{T_1} = V_{DC} - t\, dv/dt \tag{A.40}$$

$$i_{dbsT1} = \frac{V_{DC}\, t}{R_{dbs}\, T_1} = \frac{t\, dv/dt}{R_{dbs}} \tag{A.41}$$

$$p_{valveT1} = v_{valveT1}\, i_{dbsT1} = \frac{t\, dv/dt\ (V_{DC} - t\, dv/dt)}{R_{dbs}} \tag{A.42}$$

$$\Delta E_{valveT1} = \int_0^{T_1} p_{valveT1}\, dt = \frac{{V_{DC}}^3}{6\, R_{dbs}\, dv/dt} \tag{A.43}$$

And the energy expression in the braking resistor is:

$$E_{RT1} = \frac{{V_{DC}}^3}{3\, R_{dbs}\, dv/dt} \tag{A.44}$$

T_2 subinterval

Fig. A.3b shows that the valve voltage during this subinterval is zero, and therefore no energy is exchanged between the HVDC system and the valve capacitance.

$$\Delta E_{valveT2} = 0 \tag{A.45}$$

The voltage across the braking resistor is maximum during this subinterval, and the energy expression is:

$$E_{RT2} = \frac{{V_{DC}}^2\, T_2}{R_{dbs}} \tag{A.46}$$

T_3 / T_5 subintervals

During these equivalent subintervals the trapezoidal pulse differs from the one utilized with the half-bridge DBS, and the valve voltage takes negative values, as observed in Fig. A.3c. Considering a constant dv/dt:

$$T_3 = T_5 = \frac{V_A}{dv/dt} \tag{A.47}$$

And the expressions to determine the valve energy variation are:

$$v_{valveT3} = -\frac{V_A\, t}{T_3} = -t\, dv/dt \tag{A.48}$$

$$i_{dbsT3} = \frac{V_{DC} + \frac{V_A\, t}{T_3}}{R_{dbs}} = \frac{t\, dv/dt + V_{DC}}{R_{dbs}} \tag{A.49}$$

$$p_{valveT3} = v_{valveT3}\, i_{dbsT3} = -\frac{t\, dv/dt\ (t\, dv/dt + V_{DC})}{R_{dbs}} \tag{A.50}$$

$$\Delta E_{valveT3} = \int_0^{T_3} p_{valveT3}\, dt = -\frac{2\, {V_A}^3 + 3\, V_{DC}\, {V_A}^2}{6\, R_{dbs}\, dv/dt} \tag{A.51}$$

and the energy in the braking resistor:

$$E_{RT3} = \frac{{V_A}^3 + 3\, V_{DC}\, {V_A}^2 + 3\, {V_{DC}}^2\, V_A}{3\, R_{dbs}\, dv/dt} \tag{A.52}$$

$\mathbf{T_4}$ subinterval

As shown in Fig. A.3d, during this subinterval the voltage stays constant with an amplitude -A. The resulting equations are:

$$v_{valveT4} = -V_A \tag{A.53}$$

$$i_{dbsT4} = \frac{V_{DC} + V_A}{R_{dbs}} \tag{A.54}$$

$$p_{valveT4} = v_{valveT4}\, i_{dbsT4} = -\frac{V_A\ (V_A + V_{DC})}{R_{dbs}} \tag{A.55}$$

$$\Delta E_{valveT4} = \int_0^{T_4} p_{valve4}\, dt = -\frac{V_A\ (V_A + V_{DC})\ T_4}{R_{dbs}} \tag{A.56}$$

with the energy on the braking resistor:

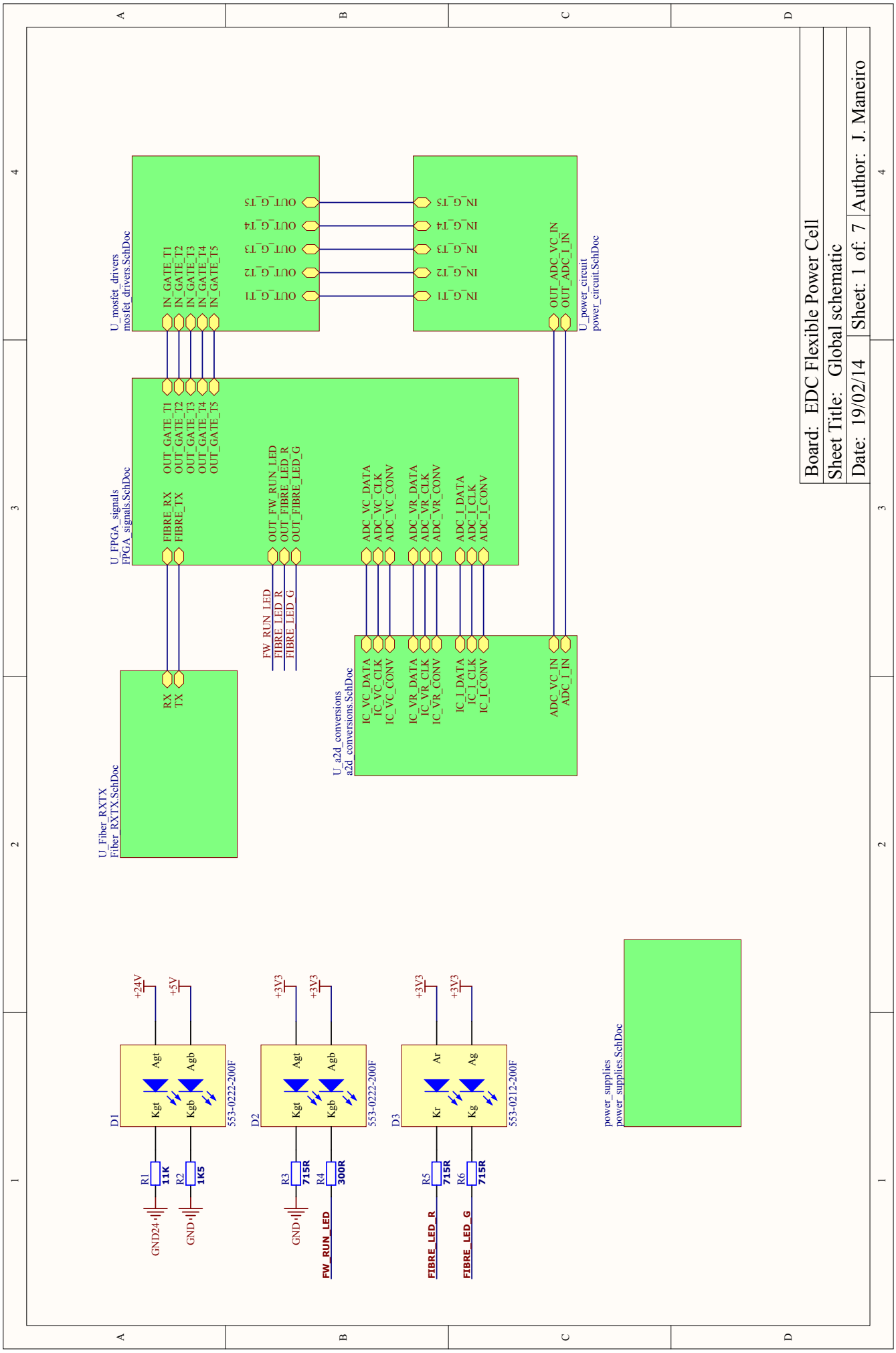
$$E_{RT4} = \frac{V_A + {V_{DC}}^2\, T_4}{R_{dbs}} \tag{A.57}$$

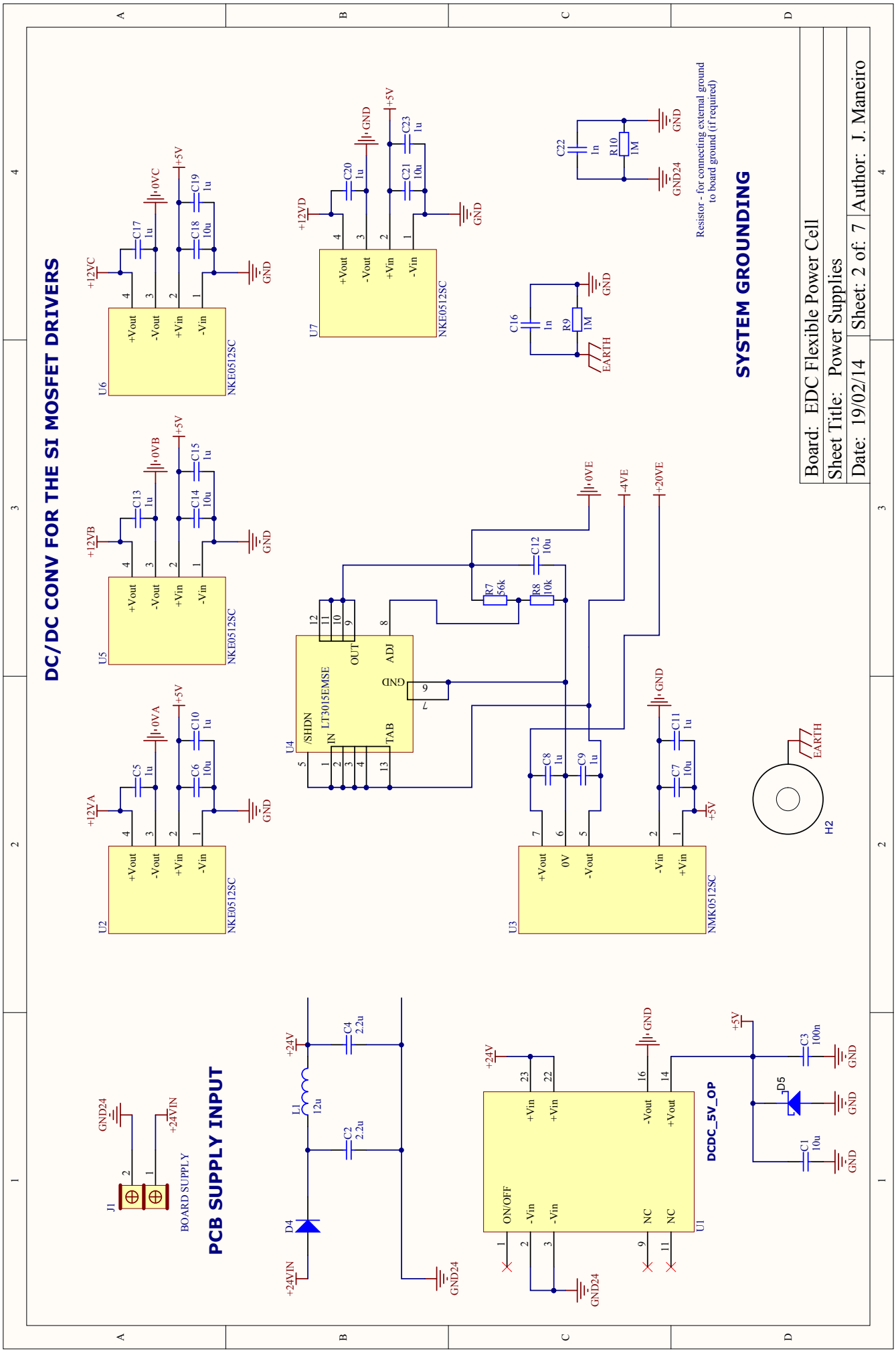
Appendix B

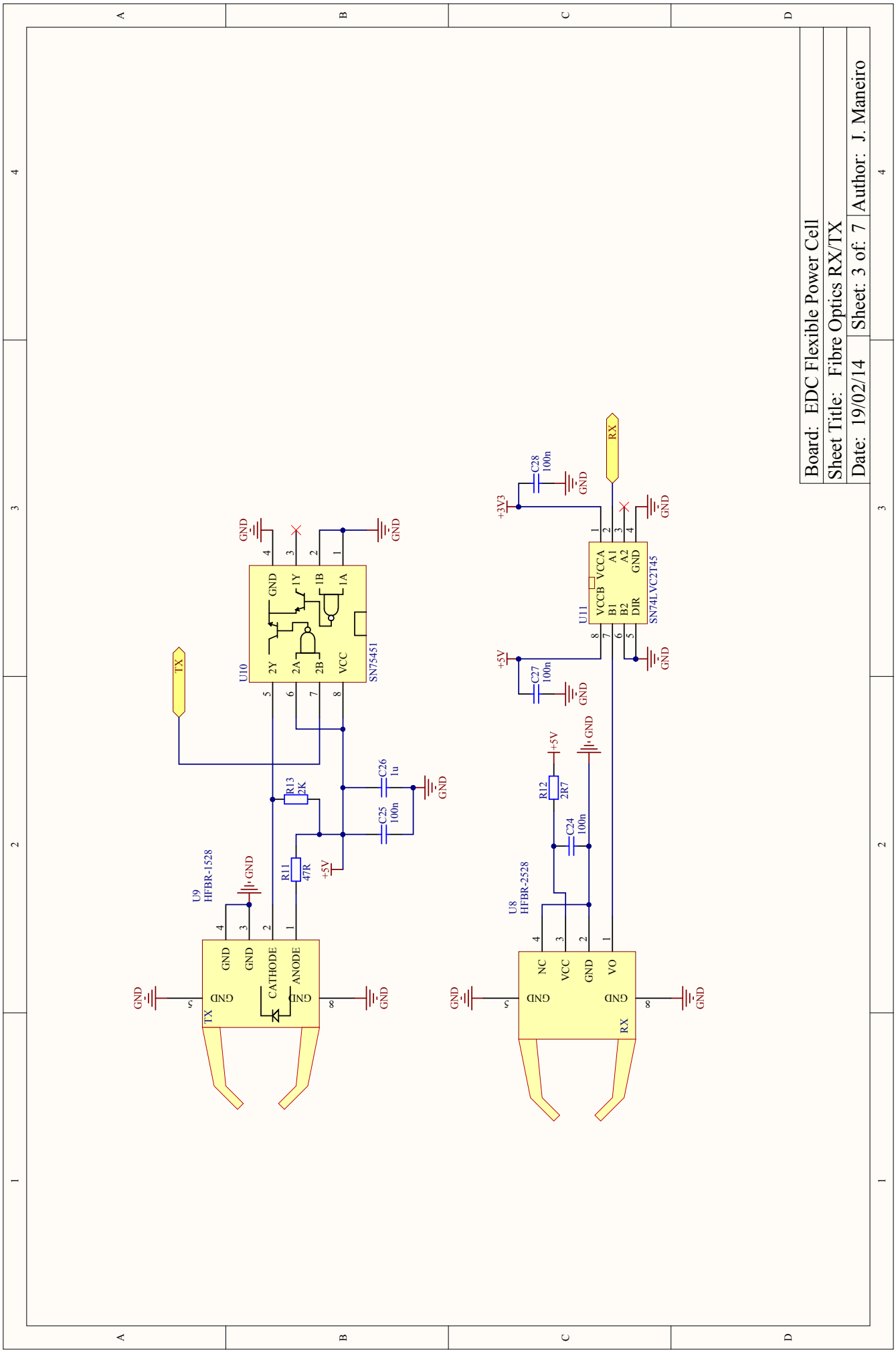
Laboratory test platform PCB schematics

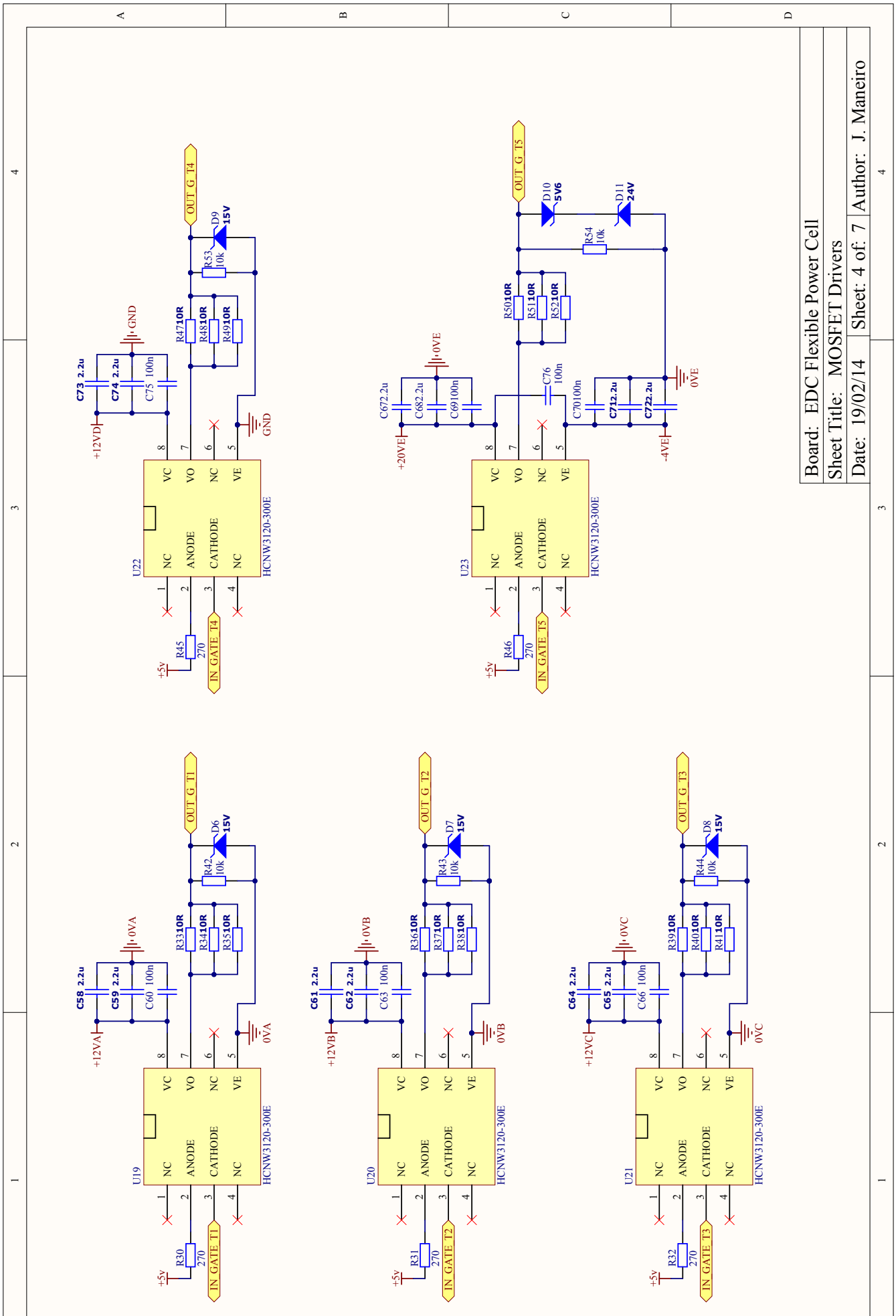
In this appendix the schematics of the four printed circuit boards designed for the re-configurable test platform are included. The represented boards are:

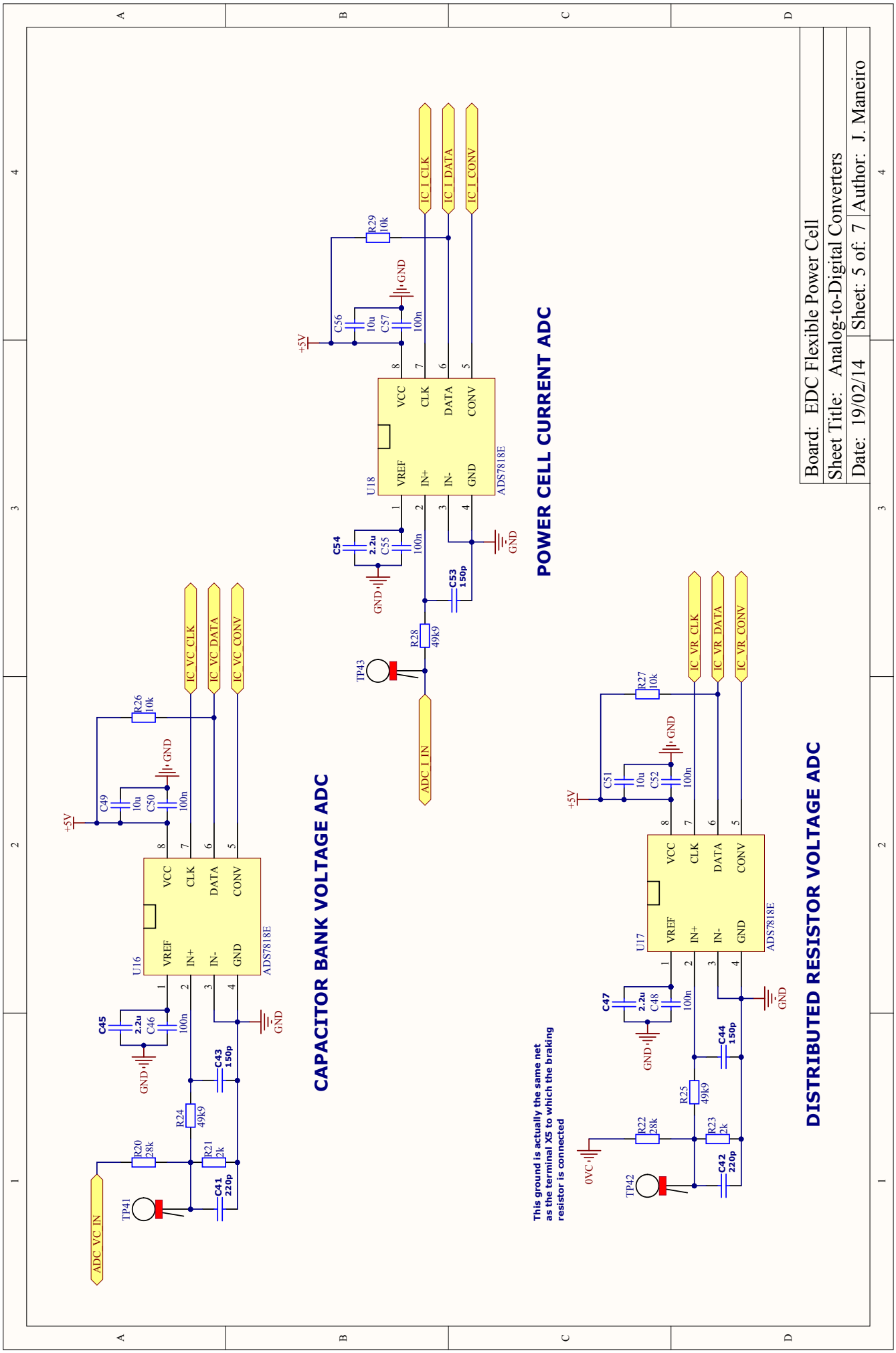
- Flexible Power Cell (PCB_EDC004)
- VSC Control Board (PCB_EDC001)
- EDC Control Board (PCB_EDC003)
- Global Control Board (PCB_EDC002)

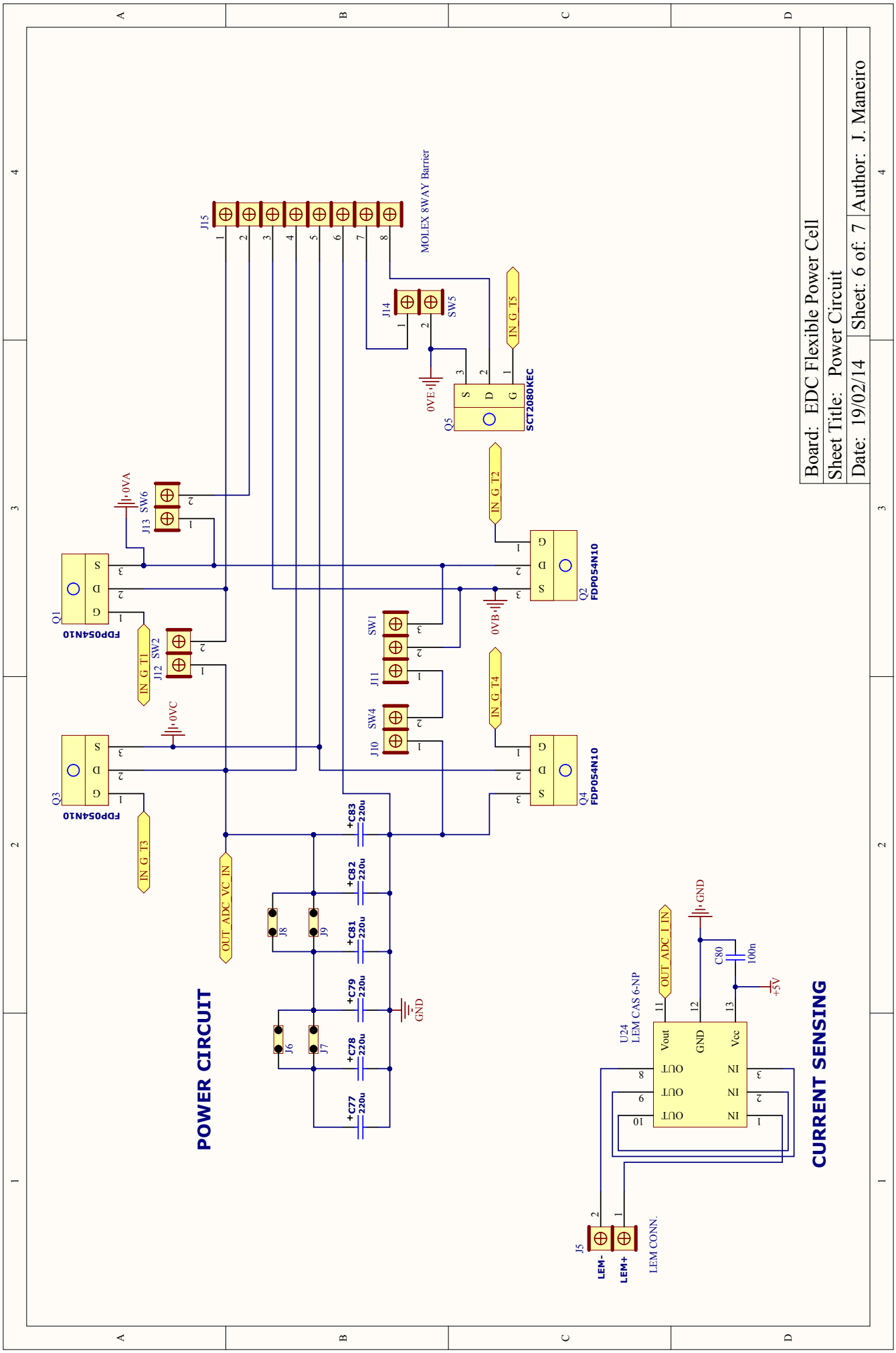

Board: EDC Flexible Power Cell
Sheet Title: Global schematic
Date: 19/02/14
Sheet: 1 of: 7
Author: J. Maneiro
U_mosfet_drivers
mosfet_drivers.SchDoc
IN_GATE_T1
IN_GATE_T2
IN_GATE_T3
IN_GATE_T4
IN_GATE_T5
OUT_G_T1
OUT_G_T2
OUT_G_T3
OUT_G_T4
OUT_G_T5
U_power_circuit
power_circuit.SchDoc
OUT_ADC_VC_IN
OUT_ADC_I_IN
U_FPGA_signals
FPGA_signals.SchDoc
FIBRE_RX
FIBRE_TX
OUT_GATE_T1
OUT_GATE_T2
OUT_GATE_T3
OUT_GATE_T4
OUT_GATE_T5
OUT_FW_RUN_LED
OUT_FIBRE_LED_R
OUT_FIBRE_LED_G
ADC_VC_DATA
ADC_VC_CLK
ADC_VC_CONV
ADC_VR_DATA
ADC_VR_CLK
ADC_VR_CONV
ADC_I_DATA
ADC_I_CLK
ADC_I_CONV
U_Fiber_RXTX
Fiber_RXTX.SchDoc
RX
TX
FW_RUN_LED
FIBRE_LED_R
FIBRE_LED_G
U_a2d_conversions
a2d_conversions.SchDoc
IC_VC_DATA
IC_VC_CLK
IC_VC_CONV
IC_VR_DATA
IC_VR_CLK
IC_VR_CONV
IC_I_DATA
IC_I_CLK
IC_I_CONV
ADC_VC_IN
ADC_I_IN
power_supplies
power_supplies.SchDoc
D1
553-0222-200F
Agt
Agb
Kgt
Kgb
+24V
+5V
R1
11K
R2
1K5
GND24
GND
D2
553-0222-200F
+3V3
R3
715R
R4
300R
FW_RUN_LED
D3
553-0212-200F
Ar
Ag
Kr
Kg
R5
715R
R6
715R
FIBRE_LED_R
FIBRE_LED_G

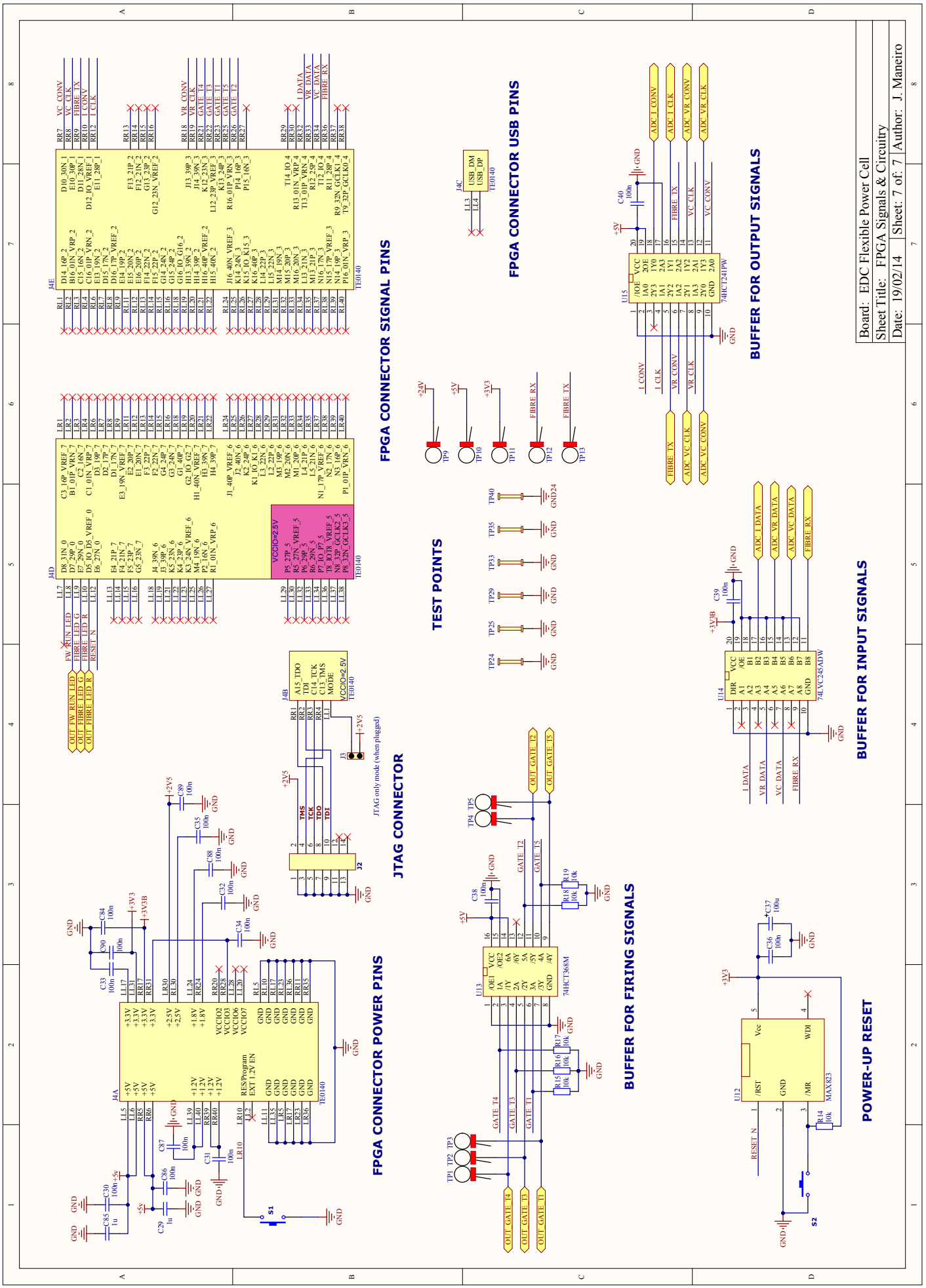

PCB SUPPLY INPUT
BOARD SUPPLY
J1
GND24
+24VIN
DCDC_5V_OP
U1
ON/OFF
-Vin
+Vin
NC
-Vout
+Vout
D4
D5
L1
12u
C1
C2
C3
C4
DC/DC CONV FOR THE SI MOSFET DRIVERS
U2
U3
U4
U5
U6
U7
NKE0512SC
NMK0512SC
LT3015EMSE
/SHDN
ADJ
OUT
GND
TAB
SYSTEM GROUNDING
Resistor - for connecting external ground
to board ground (if required)
EARTH
H2
R7
R8
R9
R10
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
Board: EDC Flexible Power Cell
Sheet Title: Power Supplies
Date: 19/02/14
Sheet: 2 of: 7
Author: J. Maneiro

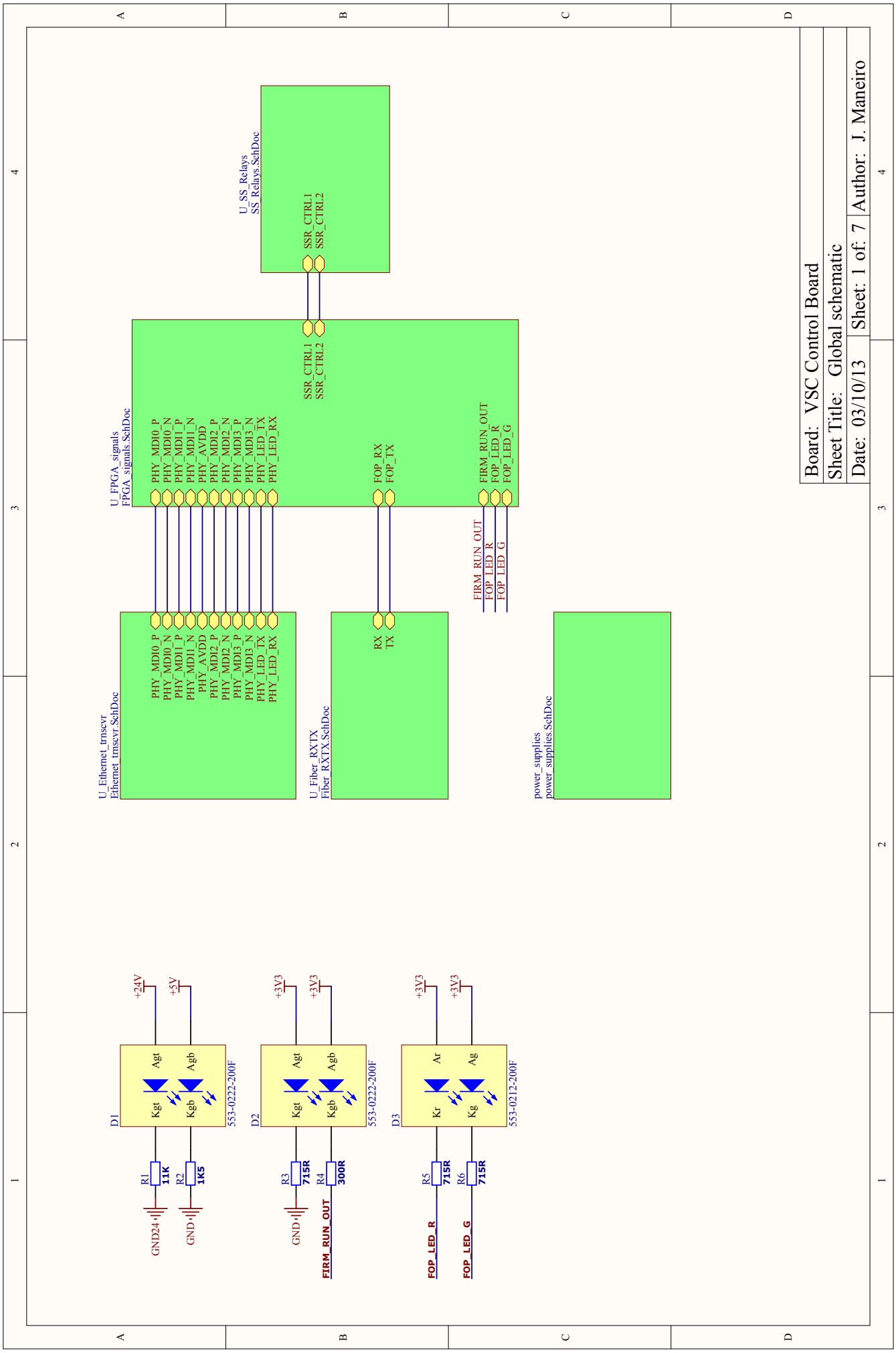

Board: EDC Flexible Power Cell
Sheet Title: Fibre Optics RX/TX
Date: 19/02/14
Sheet: 3 of: 7
Author: J. Maneiro
U9
HFBR-1528
U10
SN75451
U8
HFBR-2528
U11
SN74LVC2T45
TX
RX
R11
47R
R12
2R7
R13
2K
C24
100n
C25
100n
C26
1u
C27
100n
C28
100n
+5V
+3V3
GND

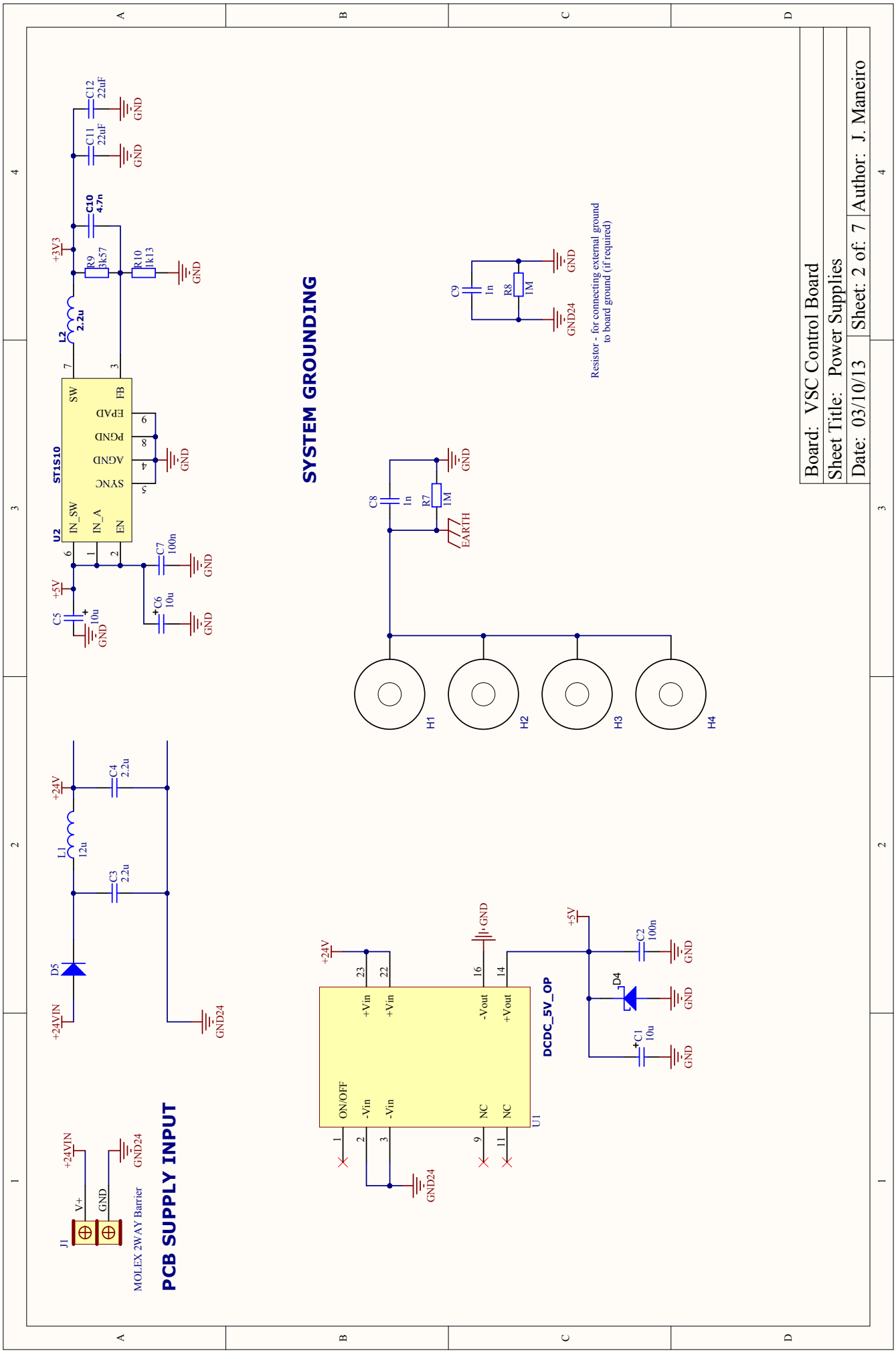

Board: EDC Flexible Power Cell
Sheet Title: MOSFET Drivers
Date: 19/02/14
Sheet: 4 of: 7
Author: J. Maneiro
U19
U20
U21
U22
U23
HCNW3120-300E
NC
ANODE
CATHODE
NC
VC
VO
VE
+12VA
+12VB
+12VC
+12VD
+20VE
-4VE
0VA
0VB
0VC
0VE
GND
+5v
IN_GATE_T1
IN_GATE_T2
IN_GATE_T3
IN_GATE_T4
IN_GATE_T5
OUT_G_T1
OUT_G_T2
OUT_G_T3
OUT_G_T4
OUT_G_T5
R30 270
R31 270
R32 270
R45 270
R46 270
R33 10R
R34 10R
R35 10R
R36 10R
R37 10R
R38 10R
R39 10R
R40 10R
R41 10R
R47 10R
R48 10R
R49 10R
R50 10R
R51 10R
R52 10R
R42 10k
R43 10k
R44 10k
R53 10k
R54 10k
D6 15V
D7 15V
D8 15V
D9 15V
D10 5V6
D11 24V
C58 2.2u
C59 2.2u
C60 100n
C61 2.2u
C62 2.2u
C63 100n
C64 2.2u
C65 2.2u
C66 100n
C73 2.2u
C74 2.2u
C75 100n
C672.2u
C682.2u
C69100n
C76 100n
C70100n
C712.2u
C722.2u

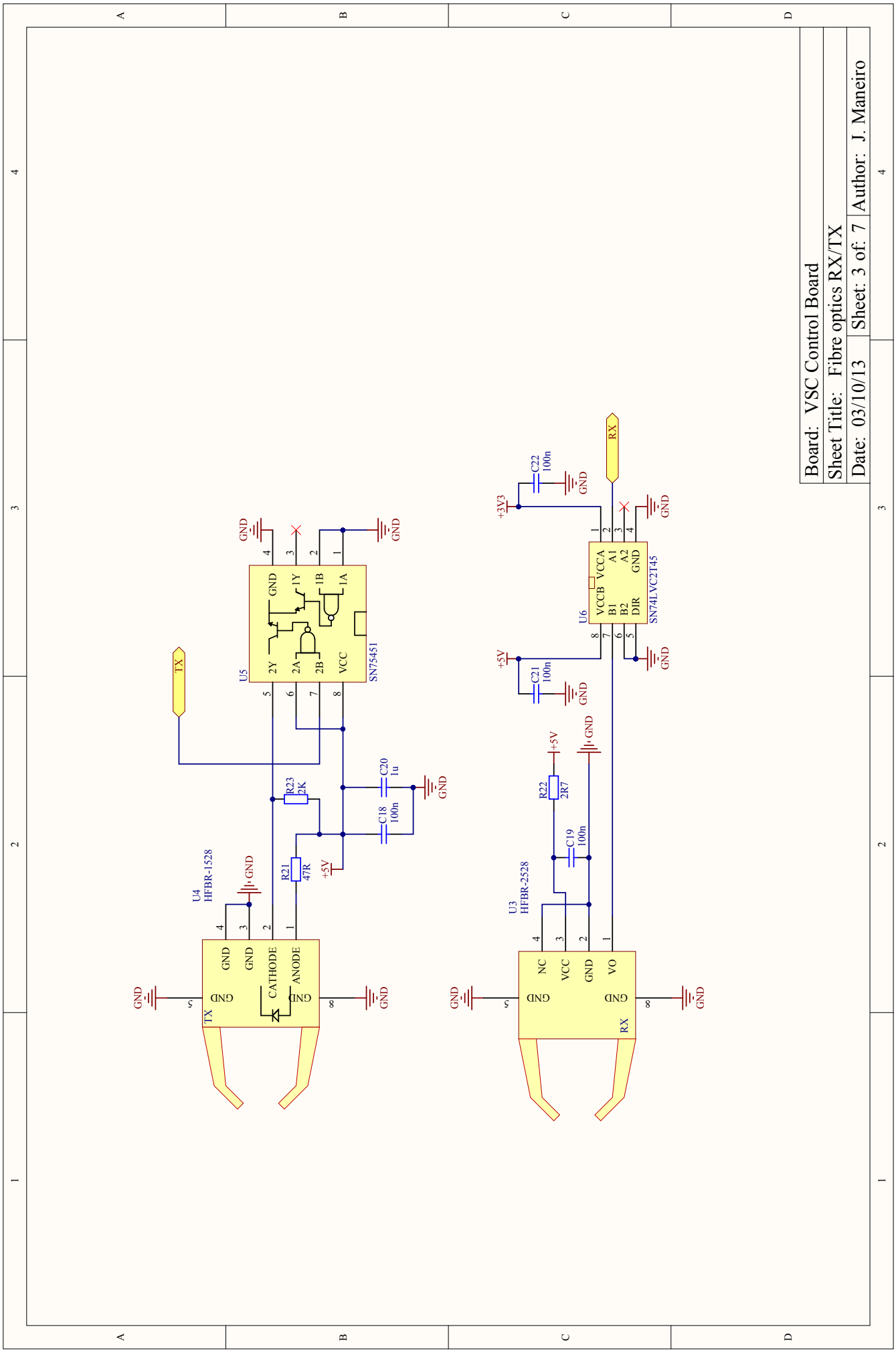

CAPACITOR BANK VOLTAGE ADC
POWER CELL CURRENT ADC
DISTRIBUTED RESISTOR VOLTAGE ADC
This ground is actually the same net as the terminal X5 to which the braking resistor is connected
ADC_VC_IN
ADC_I_IN
IC_VC_CLK
IC_VC_DATA
IC_VC_CONV
IC_I_CLK
IC_I_DATA
IC_I_CONV
IC_VR_CLK
IC_VR_DATA
IC_VR_CONV
U16
U17
U18
ADS7818E
VREF
IN+
IN-
GND
VCC
CLK
DATA
CONV
+5V
0VC
TP41
TP42
TP43
R20 28k
R21 2k
R22 28k
R23 2k
R24 49k9
R25 49k9
R26 10k
R27 10k
R28 49k9
R29 10k
C41 220p
C42 220p
C43 150p
C44 150p
C45 2.2u
C46 100n
C47 2.2u
C48 100n
C49 10u
C50 100n
C51 10u
C52 100n
C53 150p
C54 2.2u
C55 100n
C56 10u
C57 100n
Board: EDC Flexible Power Cell
Sheet Title: Analog-to-Digital Converters
Date: 19/02/14
Sheet: 5 of: 7
Author: J. Maneiro

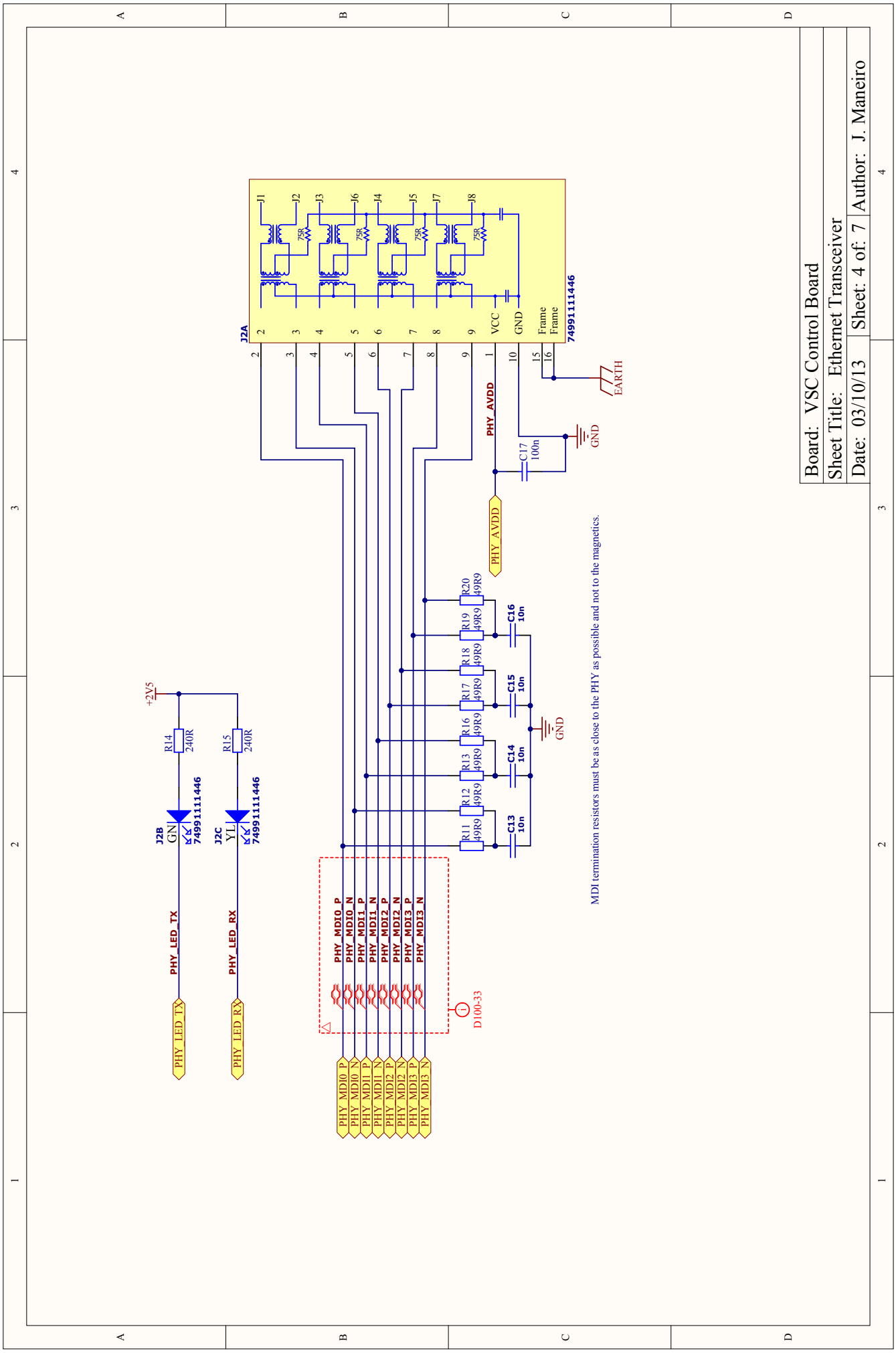

Board: EDC Flexible Power Cell
Sheet Title: Power Circuit
Date: 19/02/14
Sheet: 6 of: 7
Author: J. Maneiro
POWER CIRCUIT
CURRENT SENSING
MOLEX 8WAY Barrier
J15
J14
SW5
SW6
SW1
SW2
SW4
J13
J12
J11
J10
Q1
Q2
Q3
Q4
Q5
FDP054N10
SCT2080KEC
IN_G_T1
IN_G_T2
IN_G_T3
IN_G_T4
IN_G_T5
0VA
0VB
0VC
0VE
OUT_ADC_VC_IN
OUT_ADC_I_IN
GND
+5V
J6
J7
J8
J9
+C77 220u
+C78 220u
+C79 220u
+C81 220u
+C82 220u
+C83 220u
C80 100n
U24
LEM CAS 6-NP
Vout
GND
Vcc
OUT
IN
J5
LEM-
LEM+
LEM CONN.

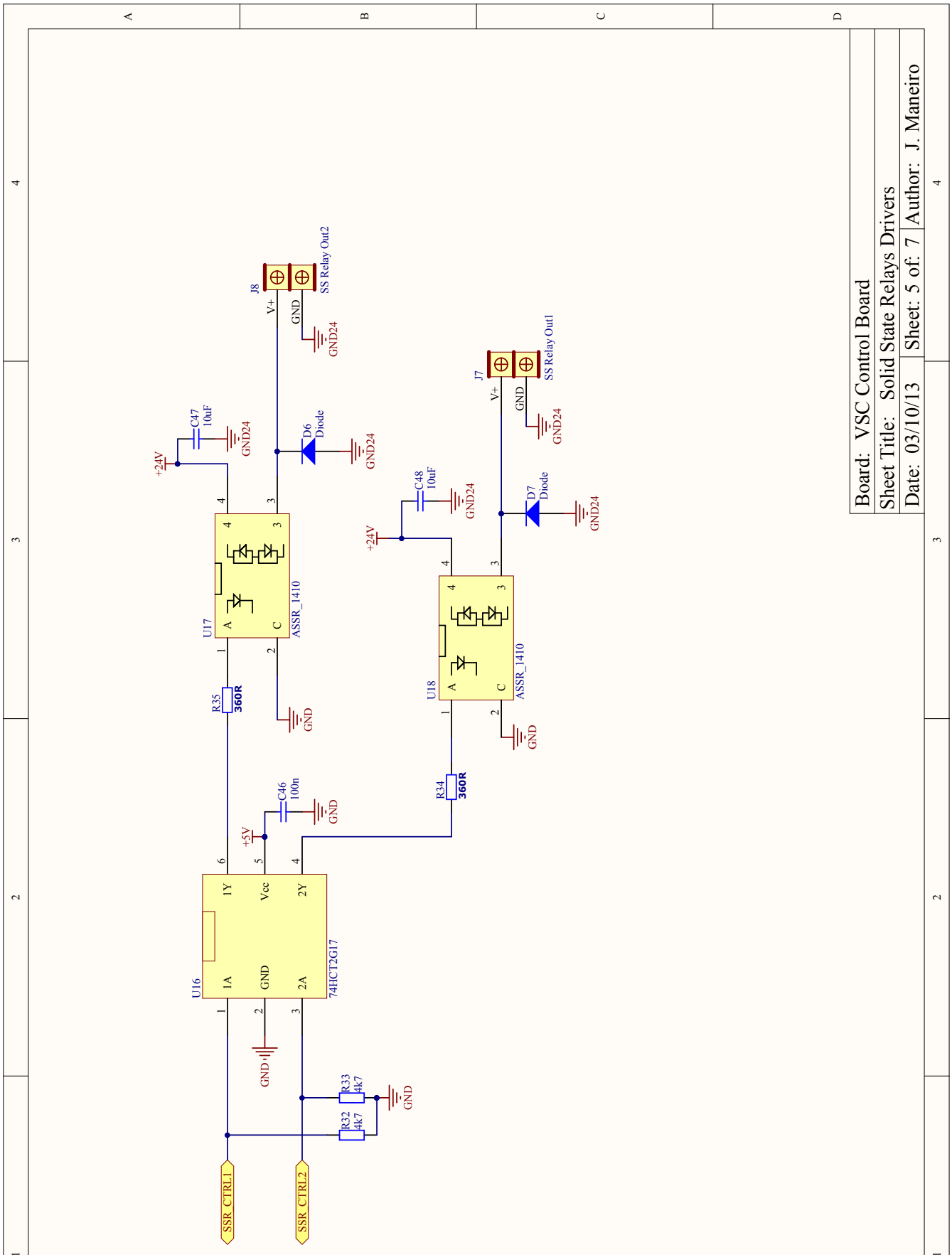

FPGA CONNECTOR SIGNAL PINS
FPGA CONNECTOR USB PINS
TEST POINTS
JTAG CONNECTOR
FPGA CONNECTOR POWER PINS
BUFFER FOR FIRING SIGNALS
BUFFER FOR OUTPUT SIGNALS
BUFFER FOR INPUT SIGNALS
POWER-UP RESET
Board: EDC Flexible Power Cell
Sheet Title: FPGA Signals & Circuitry
Date: 19/02/14
Sheet: 7 of: 7
Author: J. Maneiro

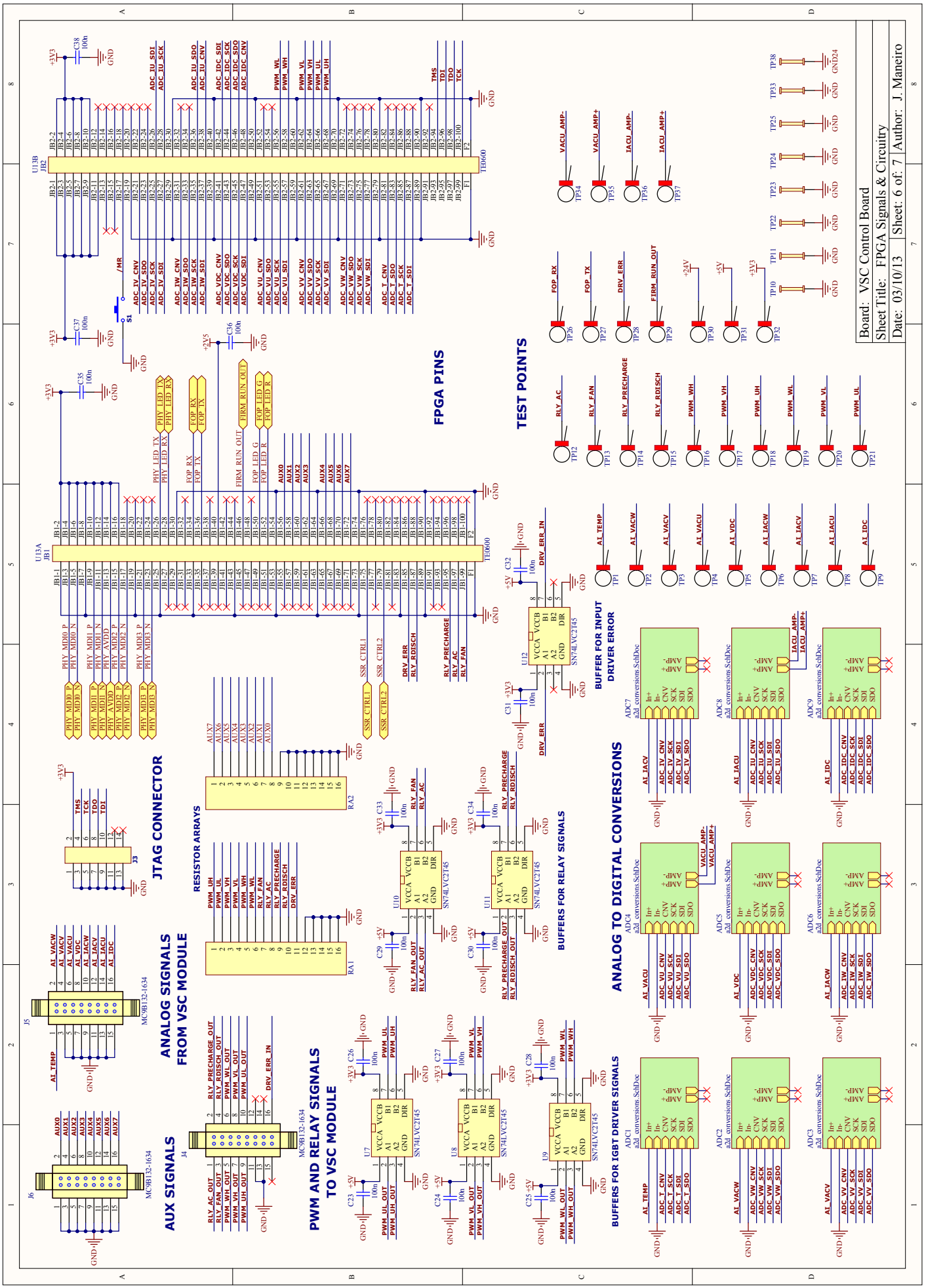

U_SS_Relays
SS_Relays.SchDoc
SSR_CTRL1
SSR_CTRL2
U_FPGA_signals
FPGA_signals.SchDoc
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_AVDD
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
PHY_LED_TX
PHY_LED_RX
FOP_RX
FOP_TX
FIRM_RUN_OUT
FOP_LED_R
FOP_LED_G
U_Ethernet_trnscvr
Ethernet_trnscvr.SchDoc
U_Fiber_RXTX
Fiber_RXTX.SchDoc
RX
TX
power_supplies
power_supplies.SchDoc
D1
553-0222-200F
Agt
Agb
Kgt
Kgb
+24V
+5V
R1
11K
R2
1K5
GND24
GND
D2
553-0222-200F
+3V3
R3
715R
R4
300R
FIRM_RUN_OUT
D3
553-0212-200F
Ar
Ag
Kr
Kg
R5
715R
R6
715R
FOP_LED_R
FOP_LED_G
Board: VSC Control Board
Sheet Title: Global schematic
Date: 03/10/13
Sheet: 1 of: 7
Author: J. Maneiro

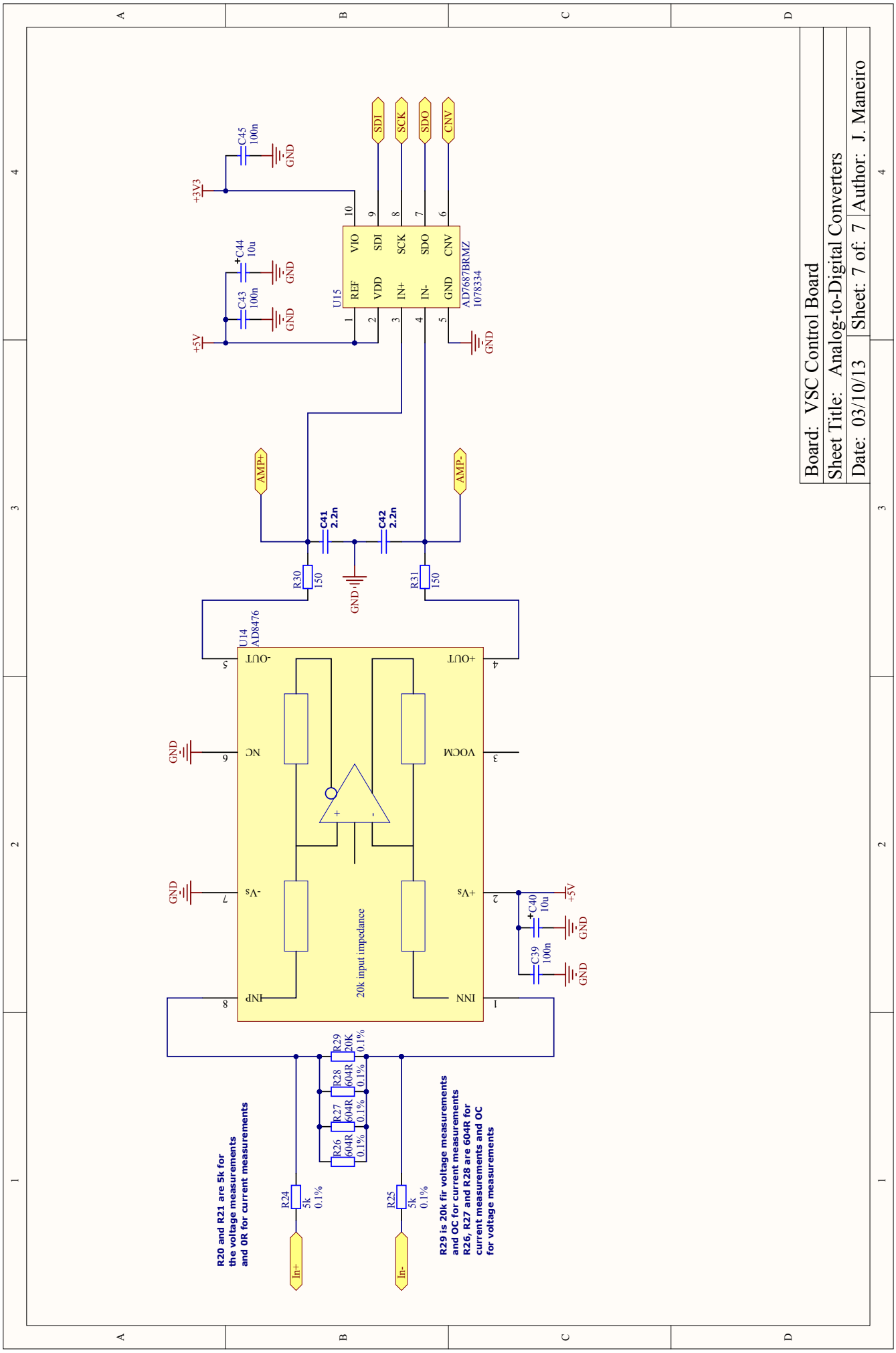

PCB SUPPLY INPUT
SYSTEM GROUNDING
Board: VSC Control Board
Sheet Title: Power Supplies
Date: 03/10/13
Sheet: 2 of: 7
Author: J. Maneiro
Resistor - for connecting external ground to board ground (if required)
MOLEX 2WAY Barrier
ST1S10
DCDC_5V_OP
+24VIN
GND24
+24V
+5V
+3V3
GND
EARTH

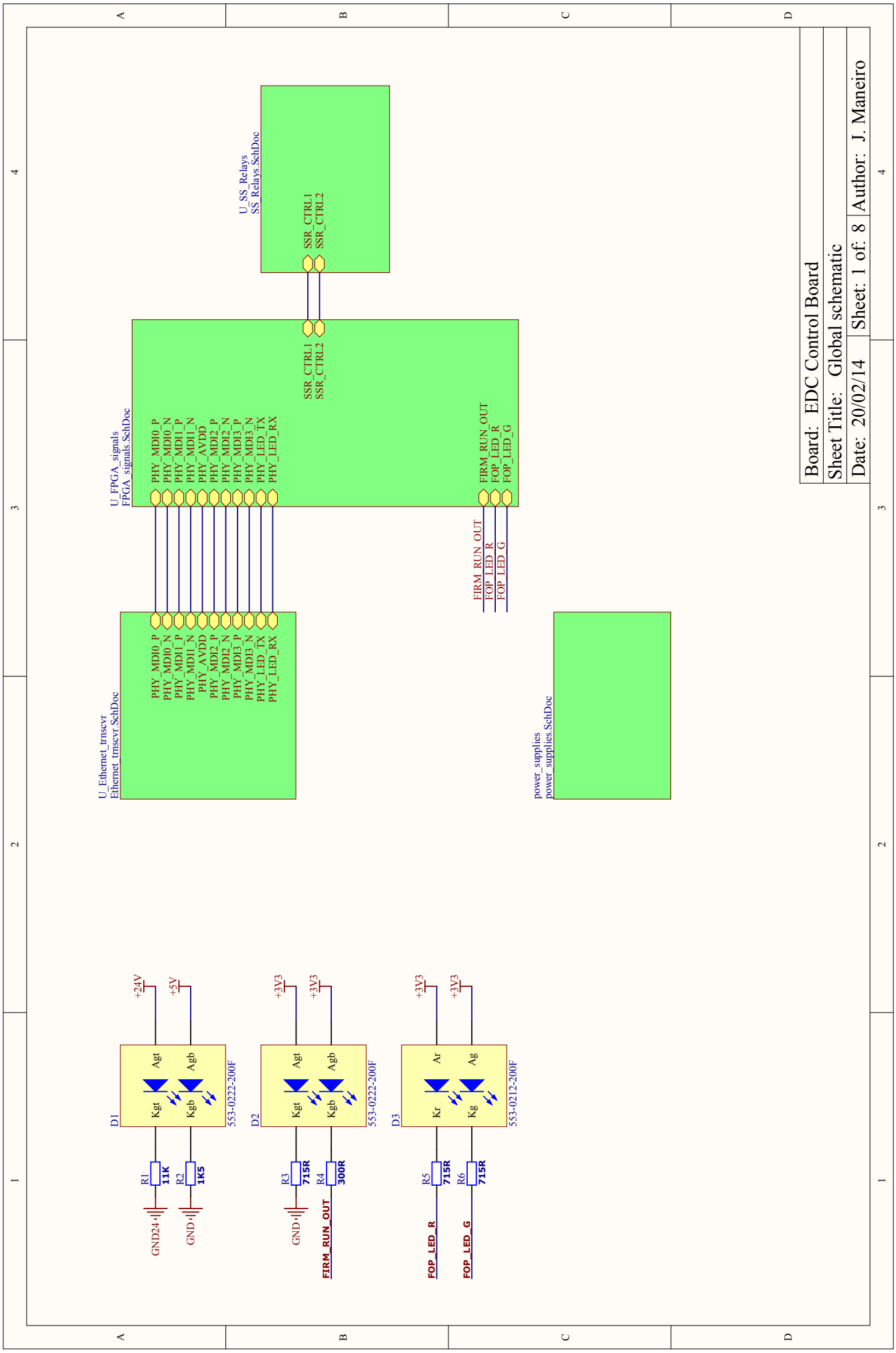

Board: VSC Control Board
Sheet Title: Fibre optics RX/TX
Date: 03/10/13
Sheet: 3 of: 7
Author: J. Maneiro
TX
RX
U4
HFBR-1528
U5
SN75451
U3
HFBR-2528
U6
SN74LVC2T45
R21
47R
R22
2R7
R23
2K
C18
100n
C19
100n
C20
1u
C21
100n
C22
100n
+5V
+3V3
GND

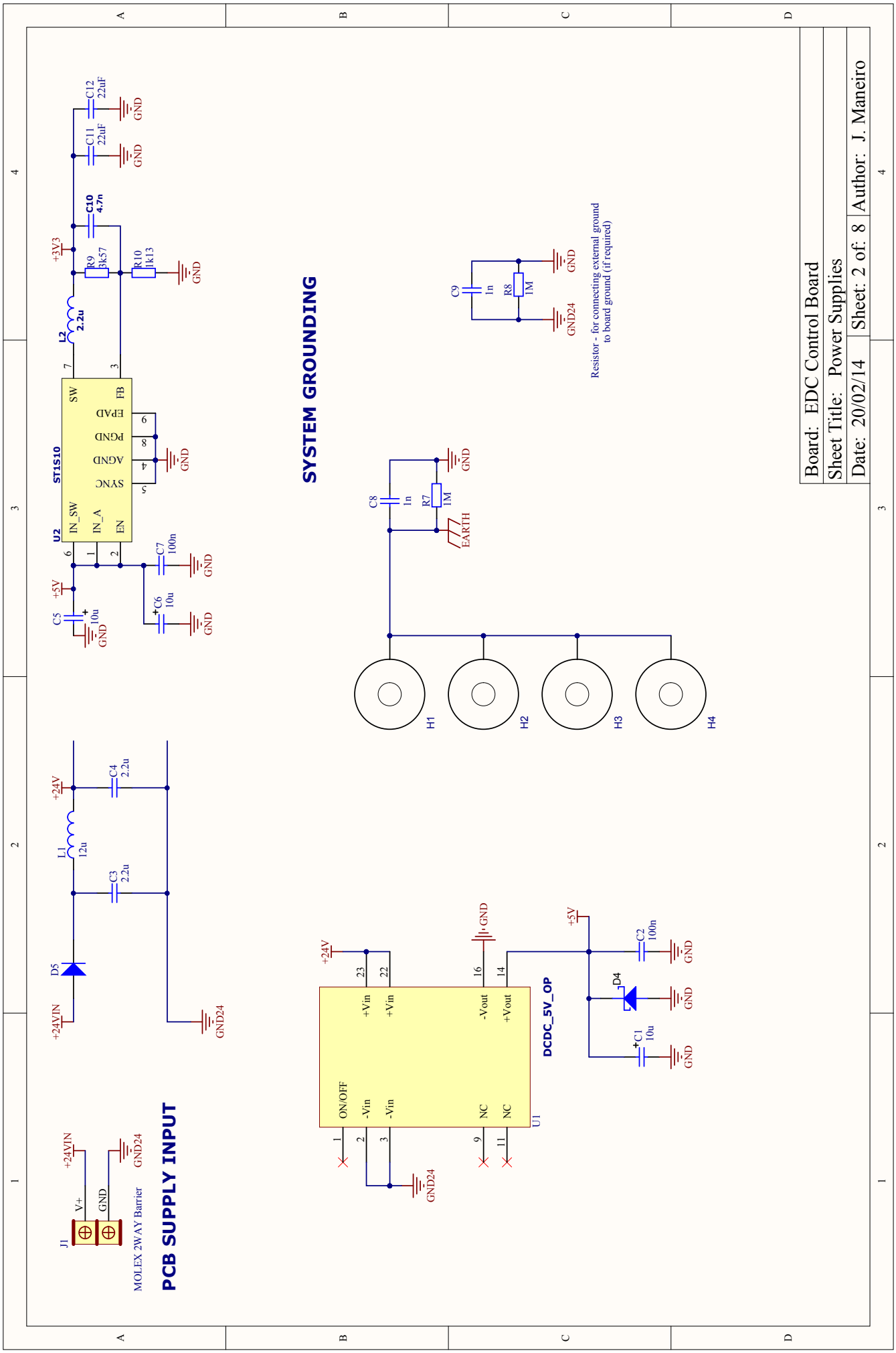

Board: VSC Control Board
Sheet Title: Ethernet Transceiver
Date: 03/10/13
Sheet: 4 of: 7
Author: J. Maneiro
J2A
74991111446
J1
J2
J3
J6
J4
J5
J7
J8
75R
VCC
GND
Frame
Frame
EARTH
PHY_AVDD
C17
100n
R20
R19
R18
R17
R16
R13
R12
R11
49R9
C16
C15
C14
C13
10n
R14
R15
240R
+2V5
J2B
J2C
GN
YL
PHY_LED_TX
PHY_LED_RX
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
D100-33
MDI termination resistors must be as close to the PHY as possible and not to the magnetics.

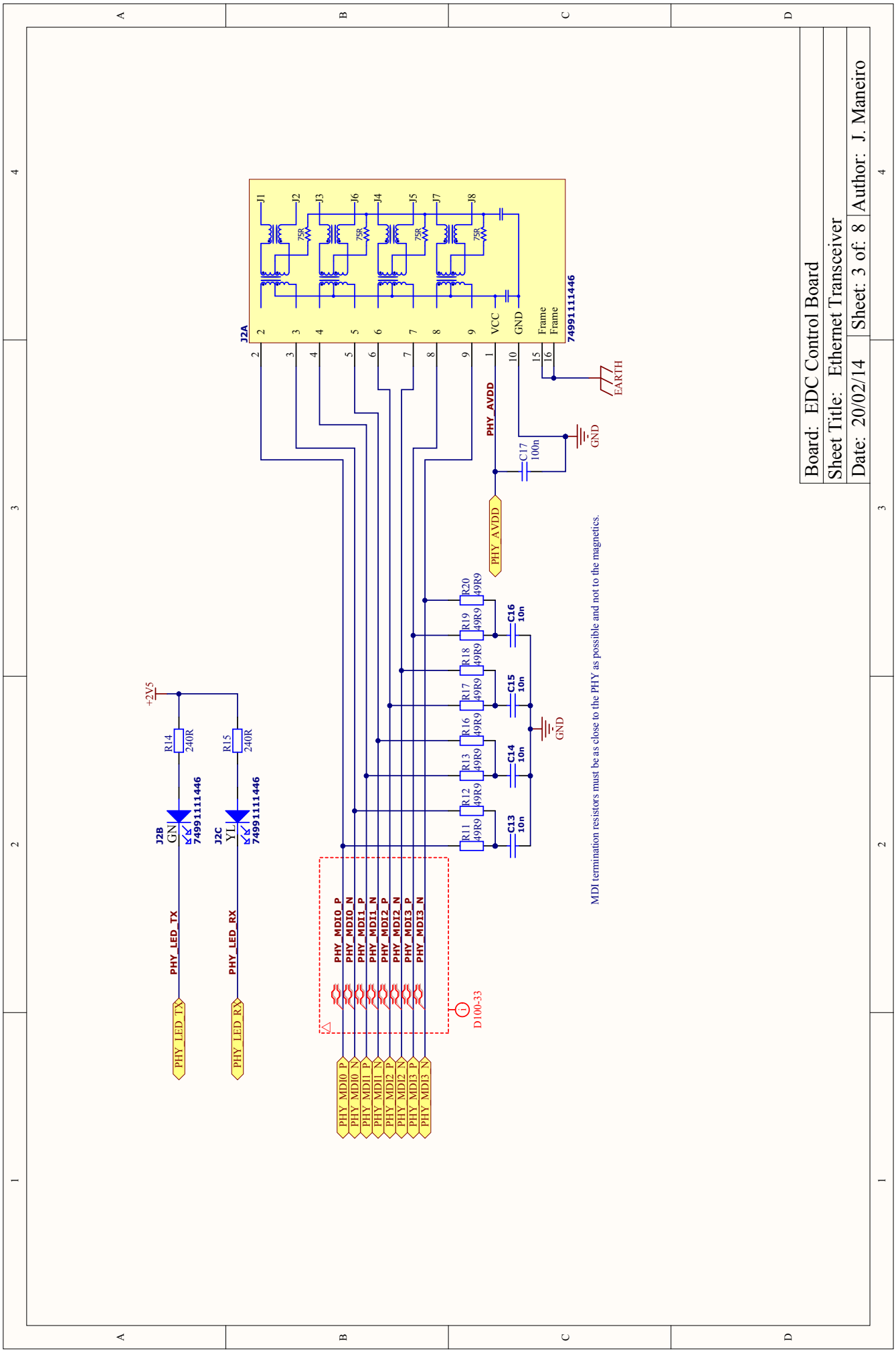

Board: VSC Control Board
Sheet Title: Solid State Relays Drivers
Date: 03/10/13
Sheet: 5 of: 7
Author: J. Maneiro
SS Relay Out2
SS Relay Out1
Diode
ASSR_1410
74HCT2G17
360R
10uF
100n
4k7
GND24
GND
+24V
+5V
SSR_CTRL1
SSR_CTRL2

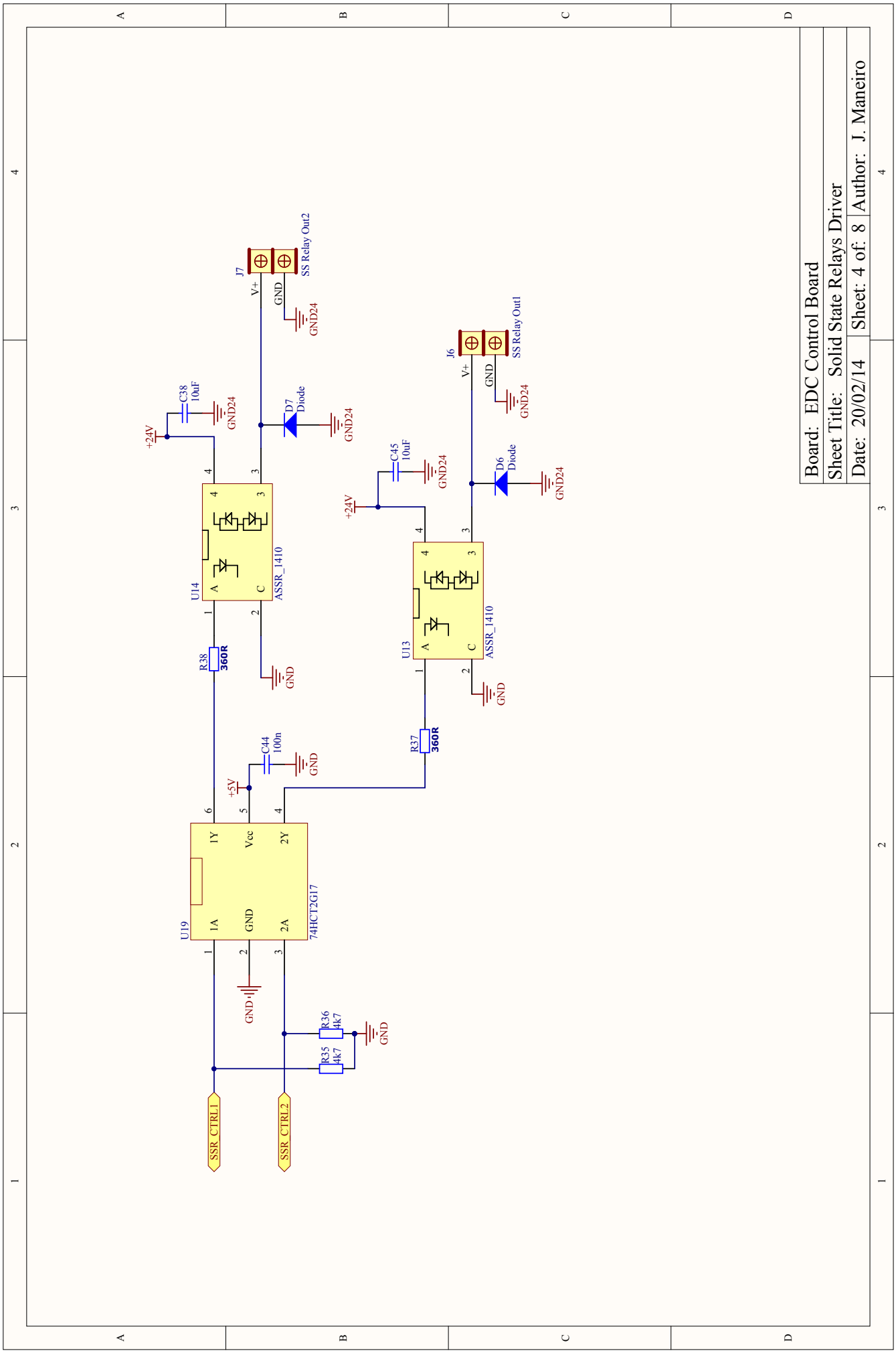

Board: VSC Control Board
Sheet Title: FPGA Signals & Circuitry
Date: 03/10/13
Sheet: 6 of: 7
Author: J. Maneiro
FPGA PINS
TEST POINTS
JTAG CONNECTOR
ANALOG SIGNALS FROM VSC MODULE
AUX SIGNALS
PWM AND RELAY SIGNALS TO VSC MODULE
RESISTOR ARRAYS
BUFFERS FOR RELAY SIGNALS
BUFFER FOR INPUT DRIVER ERROR
ANALOG TO DIGITAL CONVERSIONS
BUFFERS FOR IGBT DRIVER SIGNALS
MC9B132-1634
SN74LVC2T45
TE0600
RLY_AC
RLY_FAN
RLY_PRECHARGE
RLY_RDISCH
PWM_WH
PWM_VH
PWM_UH
PWM_WL
PWM_VL
FOP_RX
FOP_TX
DRV_ERR
FIRM_RUN_OUT
VACU_AMP-
VACU_AMP+
IACU_AMP-
IACU_AMP+
TMS
TDI
TDO
TCK
GND
+3V3
+2V5
+5V

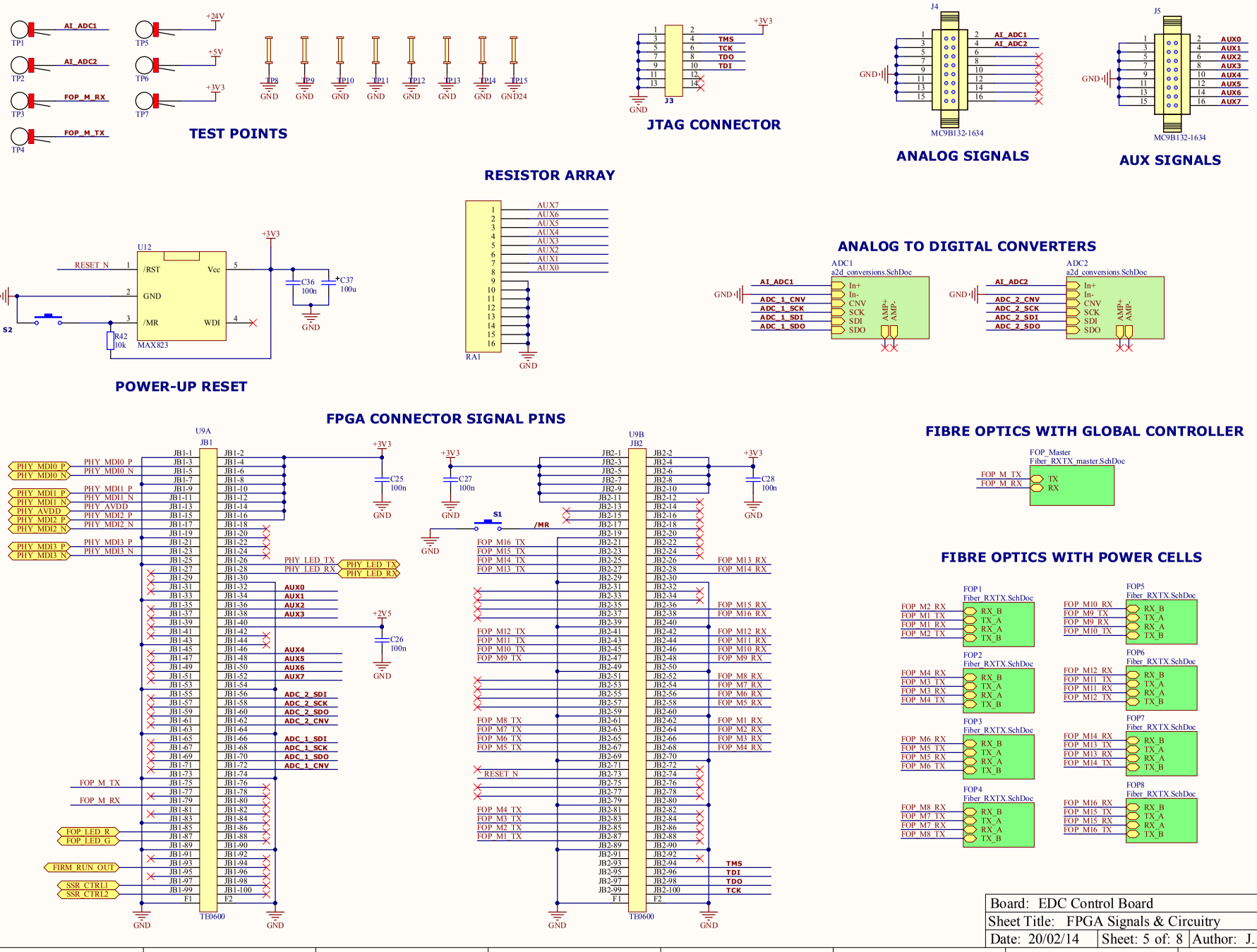

Board: VSC Control Board
Sheet Title: Analog-to-Digital Converters
Date: 03/10/13
Sheet: 7 of: 7
Author: J. Maneiro
U15
AD7687BRMZ
1078334
REF
VDD
VIO
SDI
SCK
SDO
CNV
IN+
IN-
GND
U14
AD8476
-OUT
+OUT
NC
VOCM
-Vs
+Vs
INP
INN
20k input impedance
C45 100n
C44 10u
C43 100n
C41 2.2n
C42 2.2n
C40 10u
C39 100n
R30 150
R31 150
R24 5k 0.1%
R25 5k 0.1%
R26 604R 0.1%
R27 604R 0.1%
R28 604R 0.1%
R29 20K 0.1%
+3V3
+5V
GND
AMP+
AMP-
In+
In-
SDI
SCK
SDO
CNV
R20 and R21 are 5k for the voltage measurements and 0R for current measurements
R29 is 20k fir voltage measurements and OC for current measurements R26, R27 and R28 are 604R for current measurements and OC for voltage measurements

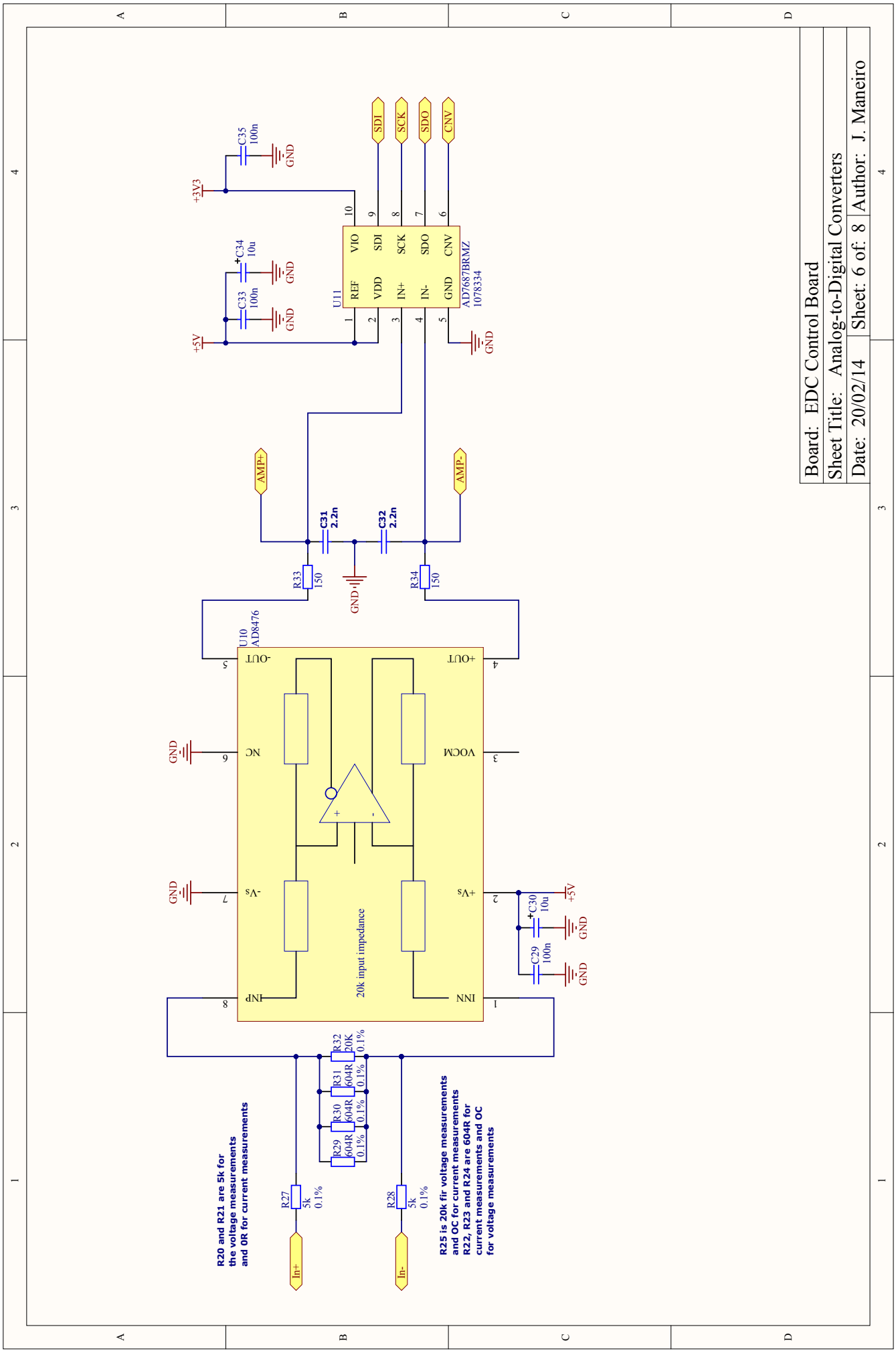

Board: EDC Control Board
Sheet Title: Global schematic
Date: 20/02/14
Sheet: 1 of: 8
Author: J. Maneiro
U_SS_Relays
SS_Relays.SchDoc
SSR_CTRL1
SSR_CTRL2
U_FPGA_signals
FPGA_signals.SchDoc
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_AVDD
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
PHY_LED_TX
PHY_LED_RX
FIRM_RUN_OUT
FOP_LED_R
FOP_LED_G
U_Ethernet_trnscvr
Ethernet_trnscvr.SchDoc
power_supplies
power_supplies.SchDoc
D1
D2
D3
553-0222-200F
553-0212-200F
Agt
Agb
Kgt
Kgb
Ar
Kr
Ag
Kg
+24V
+5V
+3V3
R1
11K
R2
1K5
R3
715R
R4
300R
R5
715R
R6
715R
GND24
GND
FIRM_RUN_OUT
FOP_LED_R
FOP_LED_G

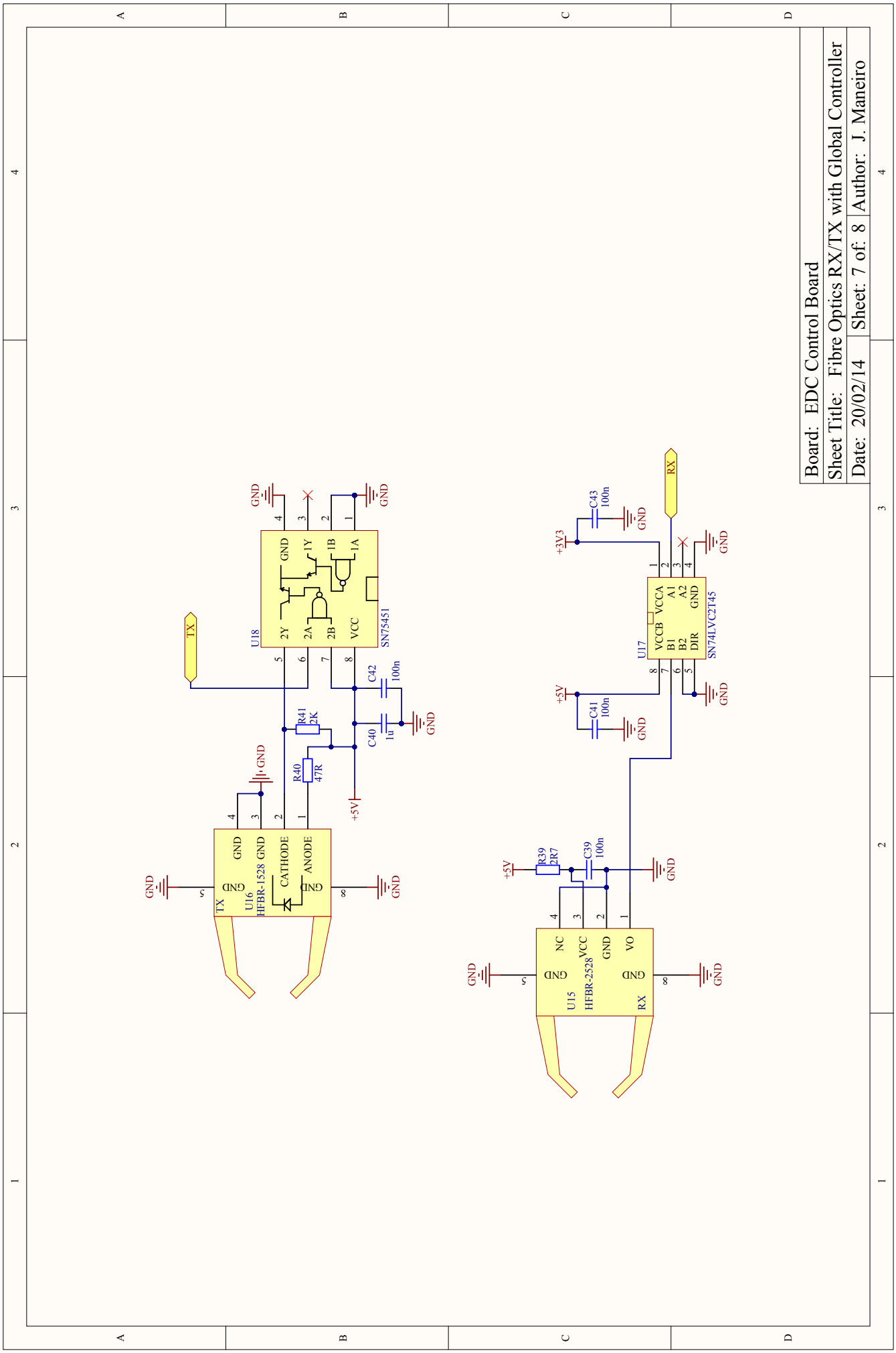

PCB SUPPLY INPUT
SYSTEM GROUNDING
Board: EDC Control Board
Sheet Title: Power Supplies
Date: 20/02/14
Sheet: 2 of: 8
Author: J. Maneiro
Resistor - for connecting external ground to board ground (if required)
MOLEX 2WAY Barrier
ST1S10
DCDC_5V_OP
+24VIN
GND24
+5V
+3V3
+24V
GND
EARTH

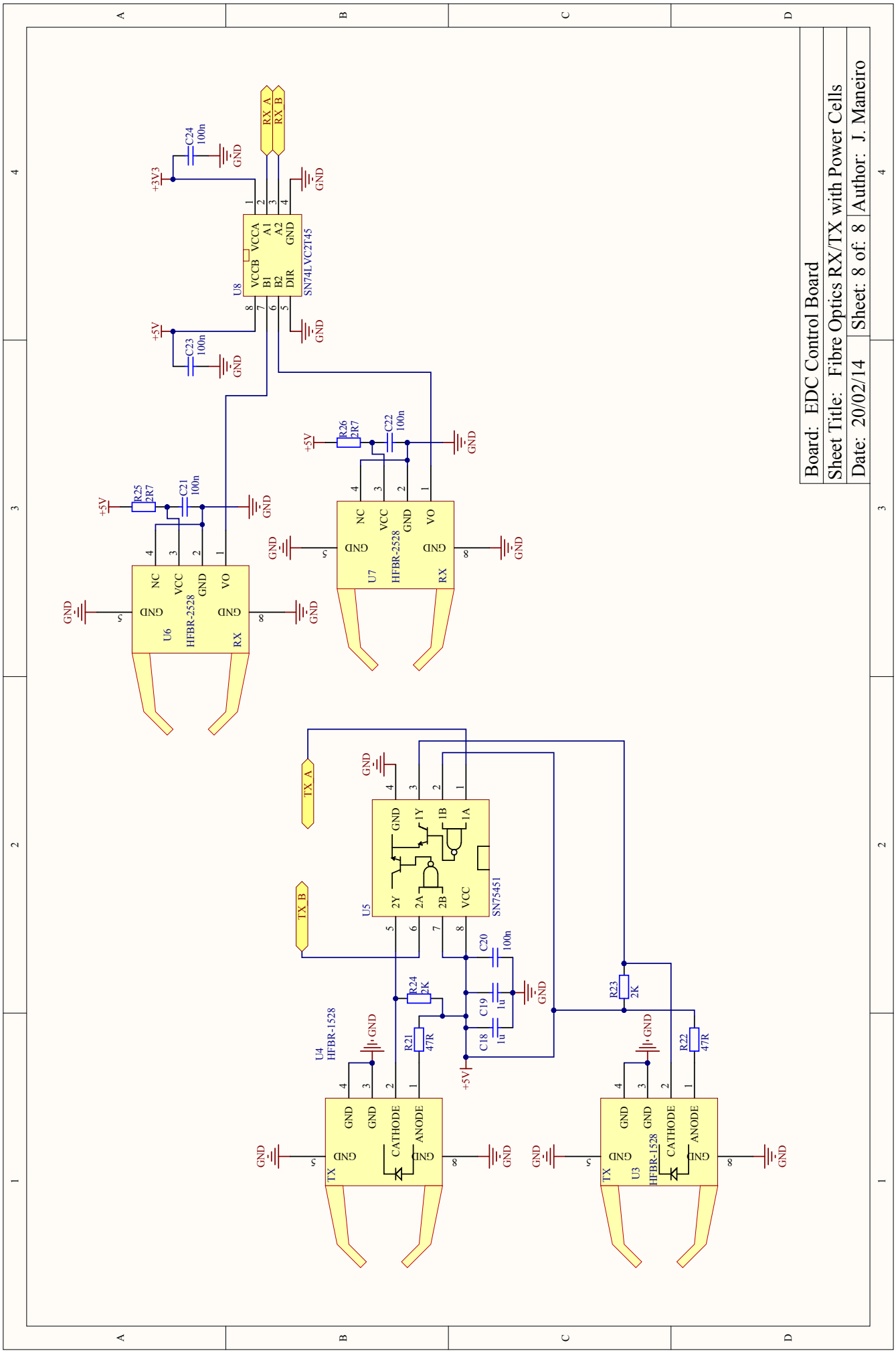

Board: EDC Control Board
Sheet Title: Ethernet Transceiver
Date: 20/02/14
Sheet: 3 of: 8
Author: J. Maneiro
J2A
74991111446
J1
J2
J3
J6
J4
J5
J7
J8
75R
VCC
GND
Frame
Frame
EARTH
PHY_AVDD
C17
100n
R20
49R9
R19
R18
R17
R16
R13
R12
R11
C16
C15
C14
C13
10n
J2B
GN
J2C
YL
R14
R15
240R
+2V5
PHY_LED_TX
PHY_LED_RX
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
D100-33
MDI termination resistors must be as close to the PHY as possible and not to the magnetics.

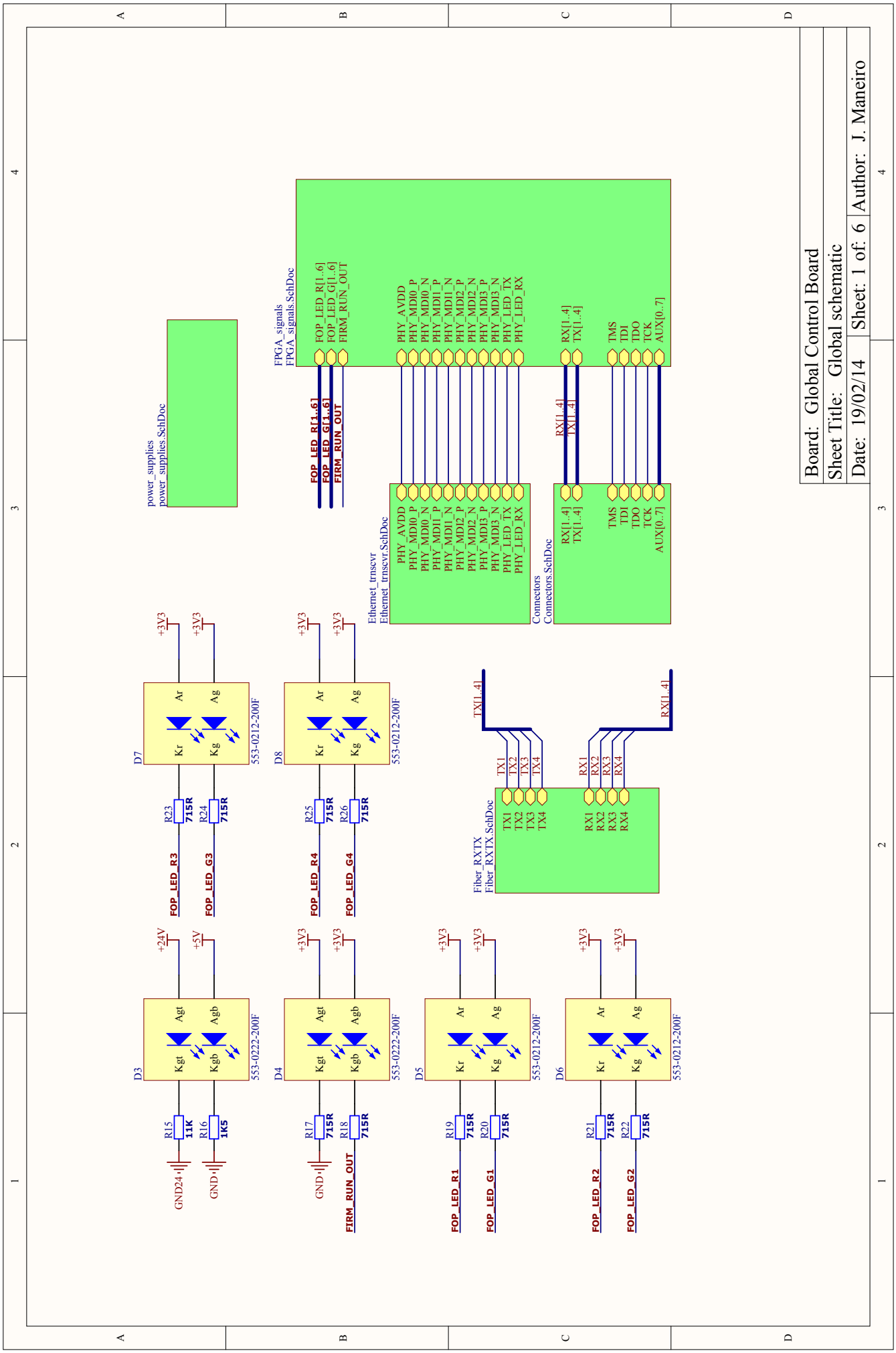

Board: EDC Control Board
Sheet Title: Solid State Relays Driver
Date: 20/02/14
Sheet: 4 of: 8
Author: J. Maneiro
SS Relay Out2
SS Relay Out1
ASSR_1410
74HCT2G17
Diode
SSR_CTRL1
SSR_CTRL2
+24V
+5V
GND
GND24
360R
4k7
10uF
100n

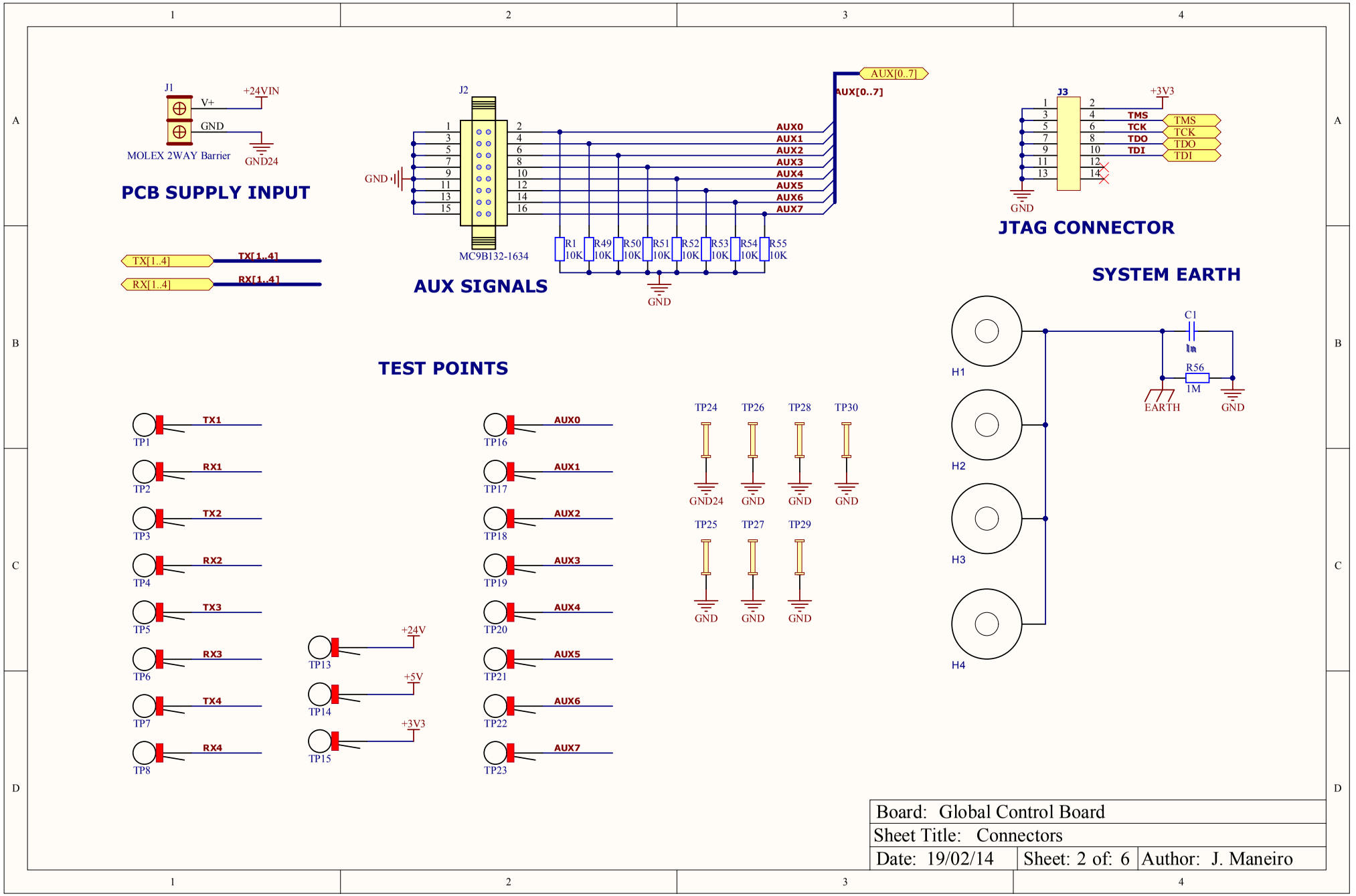

TEST POINTS
JTAG CONNECTOR
ANALOG SIGNALS
AUX SIGNALS
RESISTOR ARRAY
POWER-UP RESET
ANALOG TO DIGITAL CONVERTERS
FPGA CONNECTOR SIGNAL PINS
FIBRE OPTICS WITH GLOBAL CONTROLLER
FIBRE OPTICS WITH POWER CELLS
Board: EDC Control Board
Sheet Title: FPGA Signals & Circuitry
Date: 20/02/14
Sheet: 5 of: 8
Author: J. Maneiro

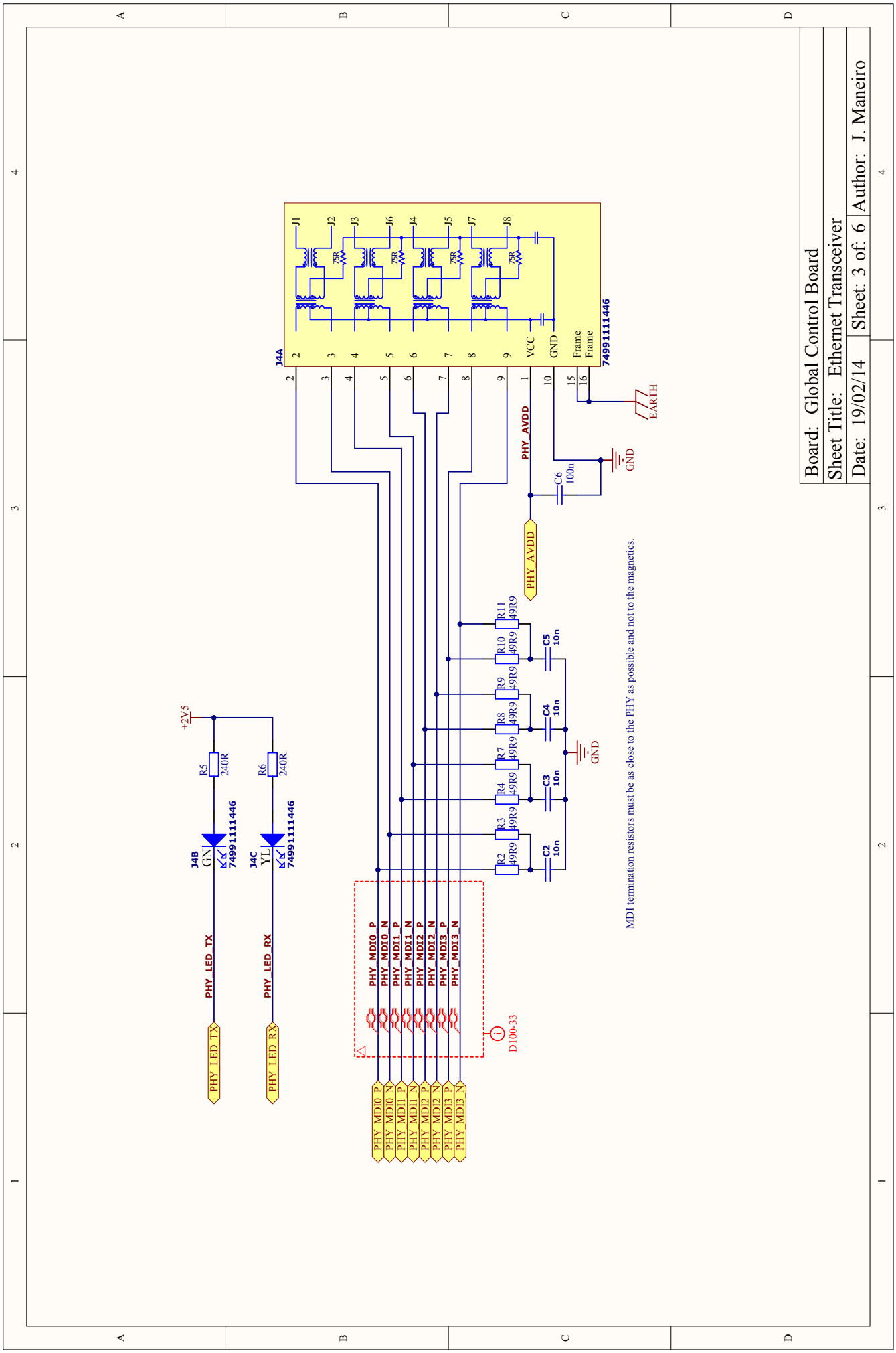

Board: EDC Control Board
Sheet Title: Analog-to-Digital Converters
Date: 20/02/14
Sheet: 6 of: 8
Author: J. Maneiro
U10
AD8476
U11
AD7687BRMZ
1078334
20k input impedance
R20 and R21 are 5k for the voltage measurements and 0R for current measurements
R25 is 20k fir voltage measurements and OC for current measurements R22, R23 and R24 are 604R for current measurements and OC for voltage measurements
In+
In-
AMP+
AMP-
SDI
SCK
SDO
CNV
+5V
+3V3
GND

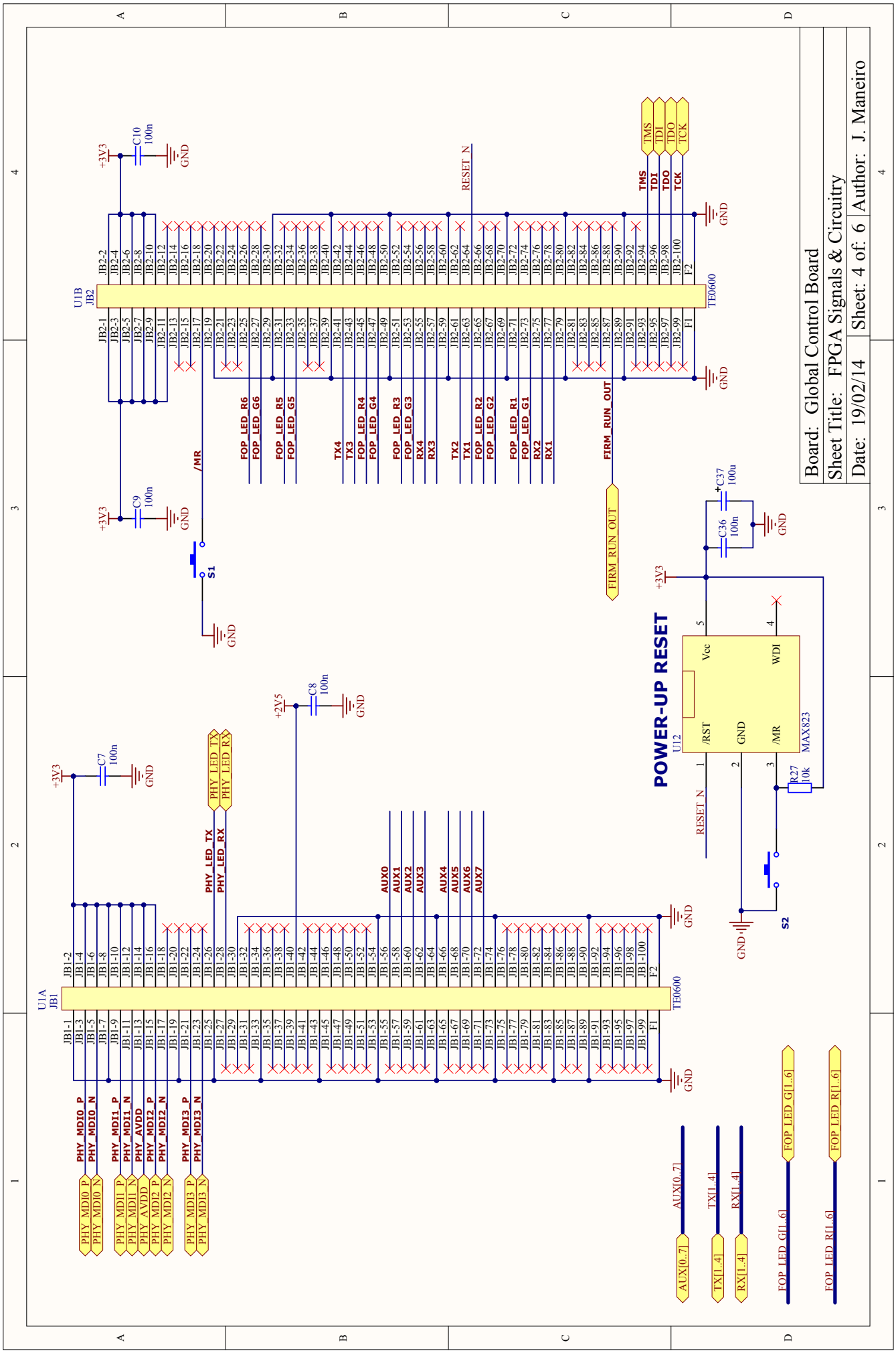

Board: EDC Control Board
Sheet Title: Fibre Optics RX/TX with Global Controller
Date: 20/02/14
Sheet: 7 of: 8
Author: J. Maneiro
TX
RX
U16
HFBR-1528
U15
HFBR-2528
U17
SN74LVC2T45
U18
SN75451
R39 2R7
R40 47R
R41 2K
C39 100n
C40 1u
C41 100n
C42 100n
C43 100n
+5V
+3V3
GND

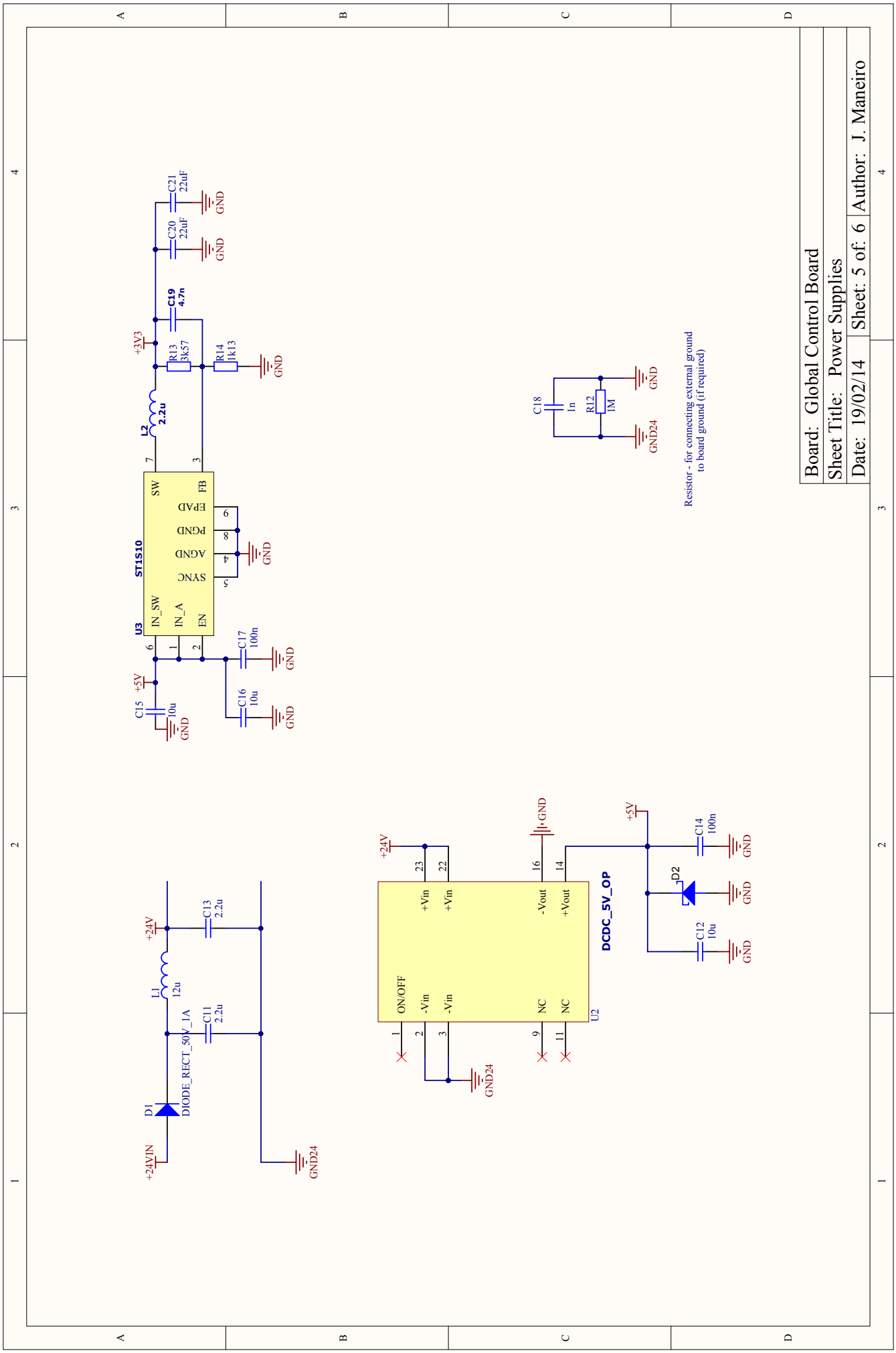

Board: EDC Control Board
Sheet Title: Fibre Optics RX/TX with Power Cells
Date: 20/02/14
Sheet: 8 of: 8
Author: J. Maneiro
RX A
RX B
TX A
TX B
U8
SN74LVC2T45
VCCB
VCCA
B1
A1
B2
A2
DIR
GND
U6
U7
HFBR-2528
NC
VCC
GND
VO
RX
U5
SN75451
1A
1B
1Y
2A
2B
2Y
U4
U3
HFBR-1528
TX
CATHODE
ANODE
C24
C23
C22
C21
C20
C19
C18
100n
1u
R26
R25
R24
R23
R22
R21
2K
47R
+3V3
+5V
GND

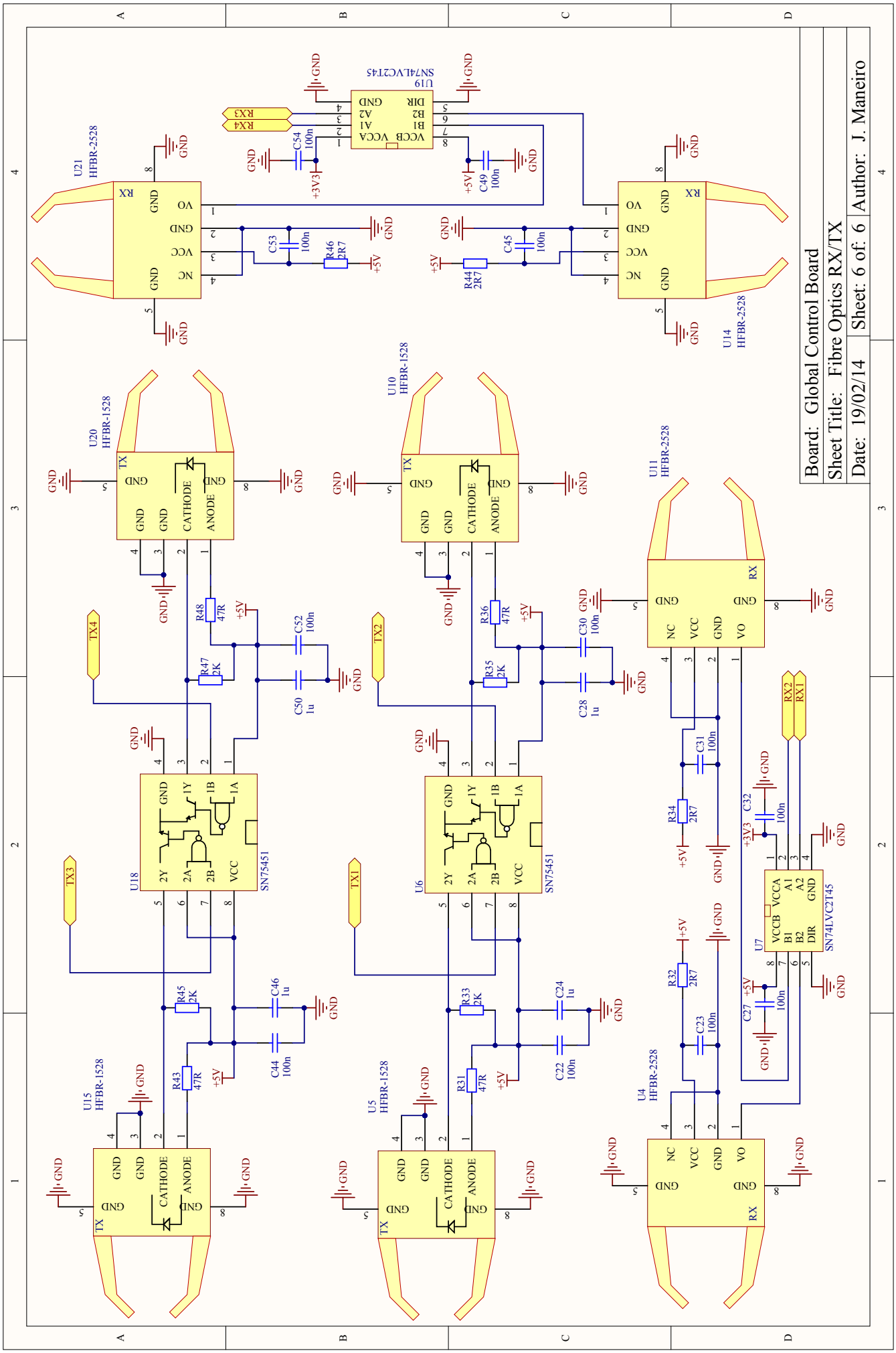

Board: Global Control Board
Sheet Title: Global schematic
Date: 19/02/14
Sheet: 1 of: 6
Author: J. Maneiro
power_supplies
power_supplies.SchDoc
FPGA_signals
FPGA_signals.SchDoc
FOP_LED_R[1..6]
FOP_LED_G[1..6]
FIRM_RUN_OUT
PHY_AVDD
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
PHY_LED_TX
PHY_LED_RX
RX[1..4]
TX[1..4]
TMS
TDI
TDO
TCK
AUX[0..7]
Ethernet_trnscvr
Ethernet_trnscvr.SchDoc
Connectors
Connectors.SchDoc
Fiber_RXTX
Fiber_RXTX.SchDoc
TX1
TX2
TX3
TX4
RX1
RX2
RX3
RX4
D3
D4
D5
D6
D7
D8
553-0222-200F
553-0212-200F
Agt
Agb
Kgt
Kgb
Ar
Ag
Kr
Kg
+24V
+5V
+3V3
GND24
GND
R15
11K
R16
1K5
R17
715R
R18
715R
R19
715R
R20
715R
R21
715R
R22
715R
R23
715R
R24
715R
R25
715R
R26
715R
FOP_LED_R1
FOP_LED_G1
FOP_LED_R2
FOP_LED_G2
FOP_LED_R3
FOP_LED_G3
FOP_LED_R4
FOP_LED_G4
FIRM_RUN_OUT


J1
V+
GND
+24VIN
GND24
MOLEX 2WAY Barrier
PCB SUPPLY INPUT
TX[1..4]
RX[1..4]
J2
MC9B132-1634
AUX[0..7]
AUX0
AUX1
AUX2
AUX3
AUX4
AUX5
AUX6
AUX7
R1 10K
R49 10K
R50 10K
R51 10K
R52 10K
R53 10K
R54 10K
R55 10K
GND
AUX SIGNALS
J3
+3V3
TMS
TCK
TDO
TDI
JTAG CONNECTOR
SYSTEM EARTH
C1
1n
R56
1M
EARTH
H1
H2
H3
H4
TEST POINTS
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP13
TP14
TP15
TP16
TP17
TP18
TP19
TP20
TP21
TP22
TP23
TP24
TP25
TP26
TP27
TP28
TP29
TP30
GND24
Board: Global Control Board
Sheet Title: Connectors
Date: 19/02/14
Sheet: 2 of: 6
Author: J. Maneiro


Board: Global Control Board
Sheet Title: Ethernet Transceiver
Date: 19/02/14
Sheet: 3 of: 6
Author: J. Maneiro
J4A
74991111446
VCC
GND
Frame
Frame
EARTH
PHY_AVDD
C6 100n
GND
MDI termination resistors must be as close to the PHY as possible and not to the magnetics.
R11 49R9
R10 49R9
R9 49R9
R8 49R9
R7 49R9
R4 49R9
R3 49R9
R2 49R9
C5 10n
C4 10n
C3 10n
C2 10n
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
D100-33
+2V5
R5 240R
R6 240R
J4B GN
J4C YL
PHY_LED_TX
PHY_LED_RX


Board: Global Control Board
Sheet Title: FPGA Signals & Circuitry
Date: 19/02/14
Sheet: 4 of: 6
Author: J. Maneiro
POWER-UP RESET
U1A
JB1
U1B
JB2
U12
MAX823
TE0600
S1
S2
C7 100n
C8 100n
C9 100n
C10 100n
C36 100n
C37 100u
R27 10k
+3V3
+2V5
GND
/MR
RESET_N
FIRM_RUN_OUT
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_AVDD
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
PHY_LED_TX
PHY_LED_RX
AUX0
AUX1
AUX2
AUX3
AUX4
AUX5
AUX6
AUX7
FOP_LED_R6
FOP_LED_G6
FOP_LED_R5
FOP_LED_G5
FOP_LED_R4
FOP_LED_G4
FOP_LED_R3
FOP_LED_G3
FOP_LED_R2
FOP_LED_G2
FOP_LED_R1
FOP_LED_G1
TX4
TX3
RX4
RX3
TX2
TX1
RX2
RX1
TMS
TDI
TDO
TCK
AUX[0..7]
TX[1..4]
RX[1..4]
FOP_LED_G[1..6]
FOP_LED_R[1..6]


Board: Global Control Board
Sheet Title: Power Supplies
Date: 19/02/14
Sheet: 5 of: 6
Author: J. Maneiro
Resistor - for connecting external ground to board ground (if required)
ST1S10
DCDC_5V_OP
DIODE_RECT_50V_1A
+24VIN
+24V
+5V
+3V3
GND
GND24


Board: Global Control Board
Sheet Title: Fibre Optics RX/TX
Date: 19/02/14
Sheet: 6 of: 6
Author: J. Maneiro
U21 HFBR-2528
U14 HFBR-2528
U19 SN74LVC2T45
U20 HFBR-1528
U10 HFBR-1528
U11 HFBR-2528
U18 SN75451
U6 SN75451
U15 HFBR-1528
U5 HFBR-1528
U4 HFBR-2528
U7 SN74LVC2T45
TX4
TX2
TX3
TX1
RX2
RX1
RX3
RX4
+5V
+3V3
GND

Appendix C

Laboratory test platform data packets for communications

The different data packets used for communication between the elements of the laboratory tests platform are presented in this appendix. The concerned communication links are:

- User interface in PC ⇒ Global control board (Ethernet/UDP)
- Global control board ⇒ User interface in PC (Ethernet/UDP)
- Global control board ⇒ EDC control board (Fibre optics)
- Global control board ⇒ VSC1 control board (Fibre optics)
- Global control board ⇒ VSC2 control board (Fibre optics)
- VSC control board 1 and 2 ⇒ Global control board (Fibre optics)
- EDC control board ⇒ Global control board (Fibre optics)
- EDC control board ⇒ Power Cell (Fibre optics)
- Power Cell ⇒ EDC control board (Fibre optics)

DATA PACKET: PC → GLOBAL CONTROLLER (ETHERNET)

BYTE #	B1		B2		B3		B4		B5		B6		B7		B8	
BIT #	b159	b152	b151	b144	b143	b136	b135	b128	b127	b120	b119	b112	b111	b104	b103	b96
	BYTE #1		BYTE #2		BYTE #3		BYTE #4		HVDC P DEM [15:8]		HVDC P DEM [7:0]		TAP P DEM [7:0]		HVDC VDC DEM [15:8]	

BYTE #	B9		B10		B11		B12		B13		B14		B15		B16	
BIT #	b95	b88	b87	b80	b79	b72	b71	b64	b63	b56	b55	b48	b47	b40	b39	b32
	HVDC VDC DEM [7:0]		FAULT DURATION [15:8]		Fault duration [7:0]		Overvoltage (%) [7:0]		KII [15:8]		KII [7:0]		KPI [15:8]		KPI [7:0]	

BYTE #	B17		B18		B19		B20	
BIT #	b31	b24	b23	b16	b15	b8	b7	b0
	KIV [15:8]		KIV [7:0]		KPV [15:8]		KPV [7:0]	

DESCRIPTION OF THE 20 BYTES OF DATA BEING SENT:

KPV **(16bits) :** VSC2 DC voltage regulator proportional gain.
KIV **(16bits) :** VSC2 DC voltage regulator integral gain.
KPI **(16bits) :** VSC2 active power regulator proportional gain.
KII **(16bits) :** VSC2 active power regulator integral gain.
OVERVOLTAGE (%) **(8bits) :** Allowed level of overvoltage for the DBS circuits operation (not used).
FAULT DURATION **(16bits) :** Time duration for the AC system fault trigered by the EDC platform.
HVDC VDC DEM **(16bits) :** DC voltage demand for the voltage regulator in VSC2.
TAP P DEM **(8bits) :** Active power demand for the operation of the EDC system configured as an HVDC tap (not used).
HVDC P DEM **(16bits) :** Active power demand for the power regulator in VSC1.

BYTE #1, #2, #3 and #4 **(16bits) :** Individual bits to manually control individual components in the platform, manage faults and enable/disable the operation of the converters.

BYTE #1	BIT #	b0	b1	b2	b3	b4	b5	b6	b7
		T5 ON/OFF	T5 PWM/MAN	T3/T4 ON/OFF	T1/T2 ON/OFF	HB PWM/MAN	BLOCK CONVERTER	EMPTY	EMPTY

BYTE #2	BIT #	b0	b1	b2	b3	b4	b5	b6	b7
		AC RLY VSC1	PCHG RLY VSC1	DISCH RLY VSC1	FAN VSC1	FAULT RLY A	FAULT RLY B	PCHG RLY 4	EMPTY

BYTE #3	BIT #	b0	b1	b2	b3	b4	b5	b6	b7
		AC RLY VSC2	PCHG RLY VSC2	DISCH RLY VSC2	FAN VSC2	AC RLY VSC3	PCHG RLY VSC3	DISCH RLY VSC3	FAN VSC3

BYTE #4	BIT #	b0	b1	b2	b3	b4	b5	b6	b7
		START HVDC	START TAP	ENABLE VSC1	ENABLE VSC2	ENABLE VSC3	ENABLE DBR	TRIGGER FAULT	RESET FAULT

DATA PACKET:GLOBAL CONTROLLER → PC (ETHERNET)

PROVENANCE OF EACH BYTE (FROM WHICH CONVERTER):

B137	B60 B59	B40 B39	B20 B19	B0
EDC (624 bits)	VSC3 (160 bits) (EMPTY)	VSC2 (160 bits)	VSC1 (160 bits)	

DESCRIPTION OF EACH BYTE INSIDE THE PACKET:

BYTE #	B137	B136	B135	B134	B133	B132	B131	B130
	SM & FLT [15:8]	SM & FLT [7:0]	IDC [15:8]	IDC [7:0]	VDC [15:8]	VDC [7:0]	PM16 I [11:4]	PM16 VR [11:8] | PM16 I [3:0]
BYTE #	B129	B128	B127	B126	B125	B124	B123	B122
	PM16 VR [7:0]	PM16 VC [11:4]	PM15 I [11:8] | PM16 VC [3:0]	PM15 I [7:0]	PM15 VR [11:4]	PM15 VC [11:8] | PM15 VR [3:0]	PM15 VC [7:0]	PM14 I [11:4]
BYTE #	B121	B120	B119	B118	B117	B116	B115	B114
	PM14 VR [11:8] | PM14 I [3:0]	PM14 VR [7:0]	PM14 VC [11:4]	PM13 I [11:8] | PM14 VC [3:0]	PM13 I [7:0]	PM13 VR [11:4]	PM13 VC [11:8] | PM13 VR [3:0]	PM13 VC [7:0]
BYTE #	B113	B112	B111	B110	B109	B108	B107	B106
	PM12 I [11:4]	PM12 VR [11:8] | PM12 I [3:0]	PM12 VR [7:0]	PM12 VC [11:4]	PM11 I [11:8] | PM12 VC [3:0]	PM11 I [7:0]	PM11 VR [11:4]	PM11 VC [11:8] | PM11 VR [3:0]
BYTE #	B105	B104	B103	B102	B101	B100	B99	B98
	PM11 VC [7:0]	PM10 I [11:4]	PM10 VR [11:8] | PM10 I [3:0]	PM10 VR [7:0]	PM10 VC [11:4]	PM9 I [11:8] | PM10 VC [3:0]	PM9 I [7:0]	PM9 VR [11:4]
BYTE #	B97	B96	B95	B94	B93	B92	B91	B90
	PM9 VC [11:8] | PM9 VR [3:0]	PM9 VC [7:0]	PM8 I [11:4]	PM8 VR [11:8] | PM8 I [3:0]	PM8 VR [7:0]	PM8 VC [11:4]	PM7 I [11:8] | PM8 VC [3:0]	PM7 I [7:0]
BYTE #	B89	B88	B87	B86	B85	B84	B83	B82
	PM7 VR [11:4]	PM7 VC [11:8] | PM7 VR [3:0]	PM7 VC [7:0]	PM6 I [11:4]	PM6 VR [11:8] | PM6 I [3:0]	PM6 VR [7:0]	PM6 VC [11:4]	PM5 I [11:8] | PM6 VC [3:0]
BYTE #	B81	B80	B79	B78	B77	B76	B75	B74
	PM5 I [7:0]	PM5 VR [11:4]	PM5 VC [11:8] | PM5 VR [3:0]	PM5 VC [7:0]	PM4 VI [11:4]	PM4 VR [11:8] | PM4 VI [3:0]	PM4 VR [7:0]	PM4 VC [11:4]
BYTE #	B73	B72	B71	B70	B69	B68	B67	B66
	PM3 I [11:8] | PM4 VC [3:0]	PM3 I [7:0]	PM3 VR [11:4]	PM3 VC [11:8] | PM3 VR [3:0]	PM3 VC [7:0]	PM2 I [11:4]	PM2 VR [11:8] | PM2 I [3:0]	PM2 VR [7:0]
BYTE #	B65	B64	B63	B62	B61	B60	B59	B58
	PM2 VC [11:4]	PM1 VI [11:8] | PM2 VC [3:0]	PM1 I [7:0]	PM1 VR [11:4]	PM1 VC [11:8] | PM1 VR [3:0]	PM1 VC [7:0]	SM & FLT [15:8]	SM & FLT [7:0]
BYTE #	B57	B56	B55	B54	B53	B52	B51	B50
	TEMP [15:8]	TEMP [7:0]	IDC [15:8]	IDC [7:0]	VDC [15:8]	VDC [7:0]	IAC3 [15:8]	IAC3 [7:0]
BYTE #	B49	B48	B47	B46	B45	B44	B43	B42
	IAC2 [15:8]	IAC2 [7:0]	IAC1 [15:8]	IAC1 [7:0]	VAC3 [15:8]	VAC3[7:0]	VAC2 [15:8]	VAC2[7:0]
BYTE #	B41	B40	B39	B38	B37	B36	B35	B34
	VAC1 [15:8]	VAC1 [7:0]	SM & FLT [15:8]	SM & FLT [7:0]	TEMP [15:8]	TEMP [7:0]	IDC [15:8]	IDC [7:0]
BYTE #	B33	B32	B31	B30	B29	B28	B27	B26
	VDC [15:8]	VDC [7:0]	IAC3 [15:8]	IAC3 [7:0]	IAC2 [15:8]	IAC2 [7:0]	IAC1 [15:8]	IAC1 [7:0]
BYTE #	B25	B24	B23	B22	B21	B20	B19	B18
	VAC3 [15:8]	VAC3[7:0]	VAC2 [15:8]	VAC2[7:0]	VAC1 [15:8]	VAC1 [7:0]	SM & FLT [15:8]	SM & FLT [7:0]
BYTE #	B17	B16	B15	B14	B13	B12	B11	B10
	TEMP [15:8]	TEMP [7:0]	IDC [15:8]	IDC [7:0]	VDC [15:8]	VDC [7:0]	IAC3 [15:8]	IAC3 [7:0]
BYTE #	B9	B8	B7	B6	B5	B4	B3	B2
	IAC2 [15:8]	IAC2 [7:0]	IAC1 [15:8]	IAC1 [7:0]	VAC3 [15:8]	VAC3[7:0]	VAC2 [15:8]	VAC2[7:0]
BYTE #	B1	B0						
	VAC1 [15:8]	VAC1 [7:0]						

VAC*X* **(16bits) :** Conversion result for the AC voltage at the converter AC terminals of the VSC converters.
VAC*X* **(16bits) :** Conversion result for the AC current at the converter AC terminals of the VSC converters.
VDC **(16bits) :** Conversion result for the DC voltage across DC terminals of VSC and EDC converters.
IDC **(16bits) :** Conversion result for the DC current measured in the VSC converters or across the EDC converter.
TEMP **(16bits) :** Conversion result for the measured IGBT module temperature in the VSC converters.
SM & FLT **(16bits) :** Internal state machine status and fault signals for VSC and EDC converters.
PM*X* VC **(12bits) :** Capacitor voltage for a particular power cell in the EDC converter.
PM*X* VR **(12bits) :** Distributed resistor voltage for a particular power cell in the EDC converter.
PM*X* I **(12bits) :** Cell current for a particular power cell in the EDC converter.

DATA PACKET: GLOBAL CONTROLLER → EDC CONTROLLER (FIBRE OPTICS)

BIT #	b31 – b24	b23	b22	b21	b20	b19	b18
	OVERVOLTAGE % [7:0]	BLOCK CONV	HB PWM/MAN	T1/T2 ON/OFF	T3/T4 ON/OFF	T5 PWM/MAN	T5 ON/OFF

BIT #	b17	b16	b15	b14	b13	b12 – b1	b0
	PCHG RLY4	RESET FAULT	ENABLE DBR	START TAP	START HVDC	EXT. STATE MACHINES	FAST FAULT

DESCRIPTION OF THE 32 BITS OF DATA BEING SENT:

OVERVOLTAGE %	**(8 bits) :**	Overvoltage limit setpoint for the operation of the EDC as a DBR. When a fault takes place, the DBR will regulate the DC system voltage to that level of overvoltage.
BLOCK CONV	**(1bit) :**	Signal to test the power module operation. Blocks any switching pulse going to the mosfets and keeps them in the off state.
HB PWM/MAN	**(1bit) :**	Signal to test the power module operation. It selects between aplying a 2kHz waveform or the state selected in the LabVIEW HMI front panel to the switches in the H-Bridge.
T1/T2 ON/OFF	**(1bit) :**	Signal to test the power module operation. Manual switching state definition for the complementary par T1/T2 mosfets in the power module.
T3/T4 ON/OFF	**(1bit) :**	Signal to test the power module operation. Manual switching state definition for the complementary par T3/T4 mosfets in the power module.
T5 PWM/MAN	**(1bit) :**	Signal to test the power module operation. It selects between aplying a 2kHz waveform or the state selected in the LabVIEW HMI front panel to switch T5.
T5 ON/OFF	**(1bit) :**	Signal to test the power module operation. Manual switching state definition for switch T5.
PCHG RLY4	**(1bit) :**	Manual control over the precharge relay for the EDC operation as an HVDC tap.
RESET FAULT	**(1bit) :**	Signal to clear the fault inside the fault monitoring module implemented in the different controllers.
ENABLE DBR	**(1bit) :**	Enable signal for the EDC converter. When the signal is low, the control board will block the commutation of the semiconductors in all the power modules.
START TAP	**(1bit) :**	Signal to start the operation of the EDC test platform configured to operate as an HVDC tap.
START HVDC	**(1bit) :**	Signal to start the operation of the EDC test platform configured to operate as a normal HVDC transmission link.
EXT. STATE MACHINES	**(12 bits):**	The signal contains the current state machones for the other 3 converters in the platform, [11:8] = SM_VSC1, [7:4] = SM_VSC2 and [3:0] = SM_VSC3.
FAST FAULT	**(1 bit):**	Provision for a possible link to quickly share a fault condition flag among the 4 converters without having to go through the PC.

DATA PACKET: GLOBAL CONTROLLER → VSC1 CONTROLLER (FIBRE OPTICS)

BIT #	b36 b21	b20	b19	b18	b17	b16	b15	b14
	HVDC Pdem[15:0]	FAN VSC1	DISCH RLY VSC1	PCHG RLY VSC1	AC RLY VSC1	RESET FAULT	ENABLE VSC1	OVERRIDE_PROT

BIT #	b13	b12 b1	b0
	START HVDC	EXT. STATE MACHINES	FAST FAULT

DESCRIPTION OF THE 37 BITS OF DATA BEING SENT:

HVDC Pdem	**(16 bits) :**	Power demand signal for VSC1 to be inserted from the AC network into the DC link. In the lab setup VSC1 controls the active power and VSC2 controls the DC voltage.
FAN VSC1	**(1bit) :**	Manual control over the fan in VSC1 converter.
DISCH RLY VSC1	**(1bit) :**	Manual control over the DC discharge relay in VSC1 converter.
PCHG RLY VSC1	**(1bit) :**	Manual control over the AC precharge relay in VSC1 converter.
AC RLY VSC1	**(1bit) :**	Manual control over the AC contactor externallly connected to VSC1 converter.
RESET FAULT	**(1bit) :**	Signal to clear the fault inside the fault monitoring module implemented inside the SysGen generated code from Simulink.
ENABLE VSC1	**(1bit) :**	Enable signal for VSC1. When the signal is low, the control board will block the commutation of the semiconductors in VSC1 converter.
OVERRIDE_PROT	**(1bit) :**	Signal to disable the overcurrent protections in VSC1 received from VSC2 at the end of a fault simulation to avoid system to trip.
START HVDC	**(1bit) :**	Signal to start the operation of the EDC test platform configured to operate as a normal HVDC transmission link.
EXT. STATE MACHINES	**(12 bits):**	The signal contains the current state machines for the other 3 converters in the platform, [11:8] = SM_VSC2, [7:4] = SM_VSC3 and [3:0] = SM_EDC.
FAST FAULT	**(1 bit):**	Provision for a possible link to quickly share a fault condition flag among the 4 converters without having to go through the PC.

DATA PACKET: GLOBAL CONTROLLER → VSC2 CONTROLLER (FIBRE OPTICS)

BIT #	b55 b40	b39 b24	b23	b22	b21	b20	b19
	HVDC VDCdem [15:0]	FAULT DURATION [15:0]	FLT RLY B	FLT RLY A	FAN VSC2	DISCH RLY VSC2	PCHG RLY VSC2

BIT #	b18	b17	b16	b15	b14	b13	b12 b1	b0
	AC RLY VSC2	RESET FAULT	TRIGGER FAULT	ENABLE VSC2	START TAP	START HVDC	EXT. STATE MACHINES	FAST FAULT

DESCRIPTION OF THE 56 BITS OF DATA BEING SENT:

HVDC VDCdem	**(16 bits) :**	DC voltage demand signal for VSC2 controller. In the lab setup VSC1 controls the active power and VSC2 controls the DC voltage.
FAULT DURATION	**(16 bits) :**	Duration of the fault simulation in milli-seconds. A low inpedance will be connected to the AC terminals of VSC2 by fault relays A and B (Solid State Relays) for a time duration equal to this value.
FLT RLY B	**(1bit) :**	Fault relay B. This relay (SSR1) connects or disconnects VSC2 converter from the AC network. When it is 'open', a high load (10kOhms) will be inserted between the AC source and the converter AC terminals.
FLT RLY A	**(1bit) :**	Fault relay A. This relay (SSR2) connects or disconnects VSC2 converter AC terminals to a very small impedance (rheostat 0-100ohms) in order to simulate the effect of an AC fault.
FAN VSC2	**(1bit) :**	Manual control over the fan in VSC2 converter.
DISCH RLY VSC2	**(1bit) :**	Manual control over the DC discharge relay in VSC2 converter.
PCHG RLY VSC2	**(1bit) :**	Manual control over the AC precharge relay in VSC2 converter.
AC RLY VSC2	**(1bit) :**	Manual control over the AC contactor externallly connected to VSC2 converter.
RESET FAULT	**(1bit) :**	Signal to clear the fault inside the fault monitoring module implemented inside the SysGen generated code from Simulink.
TRIGGER FAULT	**(1bit) :**	This signal triggers the fault event in order to operate fault relays A and B to simulate an AC fault in the AC terminals of VSC2.
ENABLE VSC2	**(1bit) :**	Enable signal for VSC2. When the signal is low, the control board will block the commutation of the semiconductors in VSC2 converter.
START TAP	**(1bit) :**	Signal to start the operation of the EDC test platform configured to operate as an HVDC tap.
START HVDC	**(1bit) :**	Signal to start the operation of the EDC test platform configured to operate as a normal HVDC transmission link.
EXT. STATE MACHINES	**(12 bits):**	The signal contains the current state machine state for the other 3 converters in the platform, [11:8] = SM_VSC1, [7:4] = SM_VSC3 and [3:0] = SM_EDC.
FAST FAULT	**(1 bit):**	Provision for a possible link to quickly share a fault condition flag among the 4 converters without having to go through the PC.

DATA PACKET: VSC CONTROLLER → GLOBAL CONTROLLER (FIBRE OPTICS)

BYTE #	B19		B18		B17		B16		B15		B14		B13		B12		B11		B10	
BIT #	b159	b152	b151	b144	b143	b136	b135	b128	b127	b120	b119	b112	b111	b104	b103	b96	b95	b88	b87	b80
	SM & FLT [15:8]		SM & FLT [7:0]		TEMP [15:8]		TEMP [7:0]		IDC [15:8]		IDC [7:0]		VDC [15:8]		VDC [7:0]		IAC3 [15:8]		IAC3 [7:0]	

BYTE #	B9		B8		B7		B6		B5		B4		B3		B2		B1		B0	
BIT #	b79	b72	b71	b64	b63	b56	b55	b48	b47	b40	b39	b32	b31	b24	b23	b16	b15	b8	b7	b0
	IAC2 [15:8]		IAC2 [7:0]		IAC1 [15:8]		IAC1 [7:0]		VAC3 [15:8]		VAC3 [7:0]		VAC2 [15:8]		VAC2 [7:0]		VAC1 [15:8]		VAC1 [7:0]	

DESCRIPTION OF THE 20 BYTES OF DATA BEING SENT:

VAC*X* **(16bits) :** Conversion result for the AC voltage at the converter AC terminals

IAC*X* **(16bits) :** Conversion result for the AC current at the converter AC terminals. Positive direction from the converter towards the AC network. Since the differential amplifier before the ADC inverts the signal, the current direction is actually compensated for the vector control required sign convention.

VDC **(16bits) :** Conversion result for the DC voltage at the converter DC terminals.
IDC **(16bits) :** Conversion result for the DC current measured between the converter DC terminals and the DC capacitance.
TEMP **(16bits) :** Conversion result for the measured IGBT module temperature.
SM & FLT **(16bits) :** Internal state machine state and fault signals. The word description is:

BIT #	b15	b14	b12	b11	b8	b7	b4	b3	b0
	FLT FLAG	EMPTY		FLT CODE		FLT CODE		SM STATE	

FLT CODE flags description for VSC1:

b4:	Vdc undervoltage
b5:	Vdc overvoltage
b6:	Idc overcurrent
b7:	Iac RMS overcurrent
b8:	Iac peak overcurrent
b9:	PLL unlock
b10..b11:	Empty
b15:	Fast fault flag

FLT CODE flags description for VSC2:

b4:	Vdc controller settling timeout
b5:	Vdc undervoltage
b6:	Vdc overvoltage
b7:	Idc overcurrent
b8:	Iac RMS overcurrent
b9:	Iac peak overcurrent
b10:	PLL unlock
b11:	Empty
b15:	Fast fault flag

b12: OVERRIDE_FLT -> in VSC2 will be used to send a signal to VSC1 to override the overcurrent faults during 40ms after the fault condition is removed and the brakers operate.

DATA PACKET: EDC CONTROLLER → GLOBAL CONTROLLER (FIBRE OPTICS)

BYTE #	B77		B76		B75		B74		B73		B72		B71	
BIT #	b623	b616	b615	b608	b607	b600	b599	b592	b591	b584	b583	b576	b575	b568
	SM & FLT [15:8]		SM & FLT [7:0]		IDC [15:8]		IDC [7:0]		VDC [15:8]		VDC [7:0]		PM16 I [11:4]	
BYTE #	B70		B69		B68		B67		B66		B65		B64	
BIT #	b567	b560	b559	b552	b551	b544	b543	b536	b535	b528	b527	b520	b519	b512
	PM16 I [3:0] | PM16 VR [11:8]		PM16 VR [7:0]		PM16 VC [11:4]		PM16 VC [3:0] | PM15 I [11:8]		PM15 I [7:0]		PM15 VR [11:4]		PM15 VR [3:0] | PM15 VC [11:8]	
BYTE #	B63		B62		B61		B60		B59		B58		B57	
BIT #	b511	b504	b503	b496	b495	b488	b487	b480	b479	b472	b471	b464	b463	b456
	PM15 VC [7:0]		PM14 I [11:4]		PM14 I [3:0] | PM14 VR [11:8]		PM14 VR [7:0]		PM14 VC [11:4]		PM14 VC [3:0] | PM13 I [11:8]		PM13 I [7:0]	
BYTE #	B56		B55		B54		B53		B52		B51		B50	
BIT #	b455	b448	b447	b440	b439	b432	b431	b424	b423	b416	b415	b408	b407	b400
	PM13 VR [11:4]		PM13 VR [3:0] | PM13 VC [11:8]		PM13 VC [7:0]		PM12 I [11:4]		PM12 I [3:0] | PM12 VR [11:8]		PM12 VR [7:0]		PM12 VC [11:4]	
BYTE #	B49		B48		B47		B46		B45		B44		B43	
BIT #	b399	b392	b391	b384	b383	b376	b375	b368	b367	b360	b359	b352	b351	b344
	PM12 VC [3:0] | PM11 I [11:8]		PM11 I [7:0]		PM11 VR [11:4]		PM11 VR [3:0] | PM11 VC [11:8]		PM11 VC [7:0]		PM10 I [11:4]		PM10 I [3:0] | PM10 VR [11:8]	
BYTE #	B42		B41		B40		B39		B38		B37		B36	
BIT #	b343	b336	b335	b328	b327	b320	b319	b312	b311	b304	b303	b296	b295	b288
	PM10 VR [7:0]		PM10 VC [11:4]		PM10 VC [3:0] | PM9 I [11:8]		PM9 I [7:0]		PM9 VR [11:4]		PM9 VR [3:0] | PM9 VC [11:8]		PM9 VC [7:0]	
BYTE #	B35		B34		B33		B32		B31		B30		B29	
BIT #	b287	b280	b279	b272	b271	b264	b263	b256	b255	b248	b247	b240	b239	b232
	PM8 I [11:4]		PM8 I [3:0] | PM8 VR [11:8]		PM8 VR [7:0]		PM8 VC [11:4]		PM8 VC [3:0] | PM7 I [11:8]		PM7 I [7:0]		PM7 VR [11:4]	
BYTE #	B28		B27		B26		B25		B24		B23		B22	
BIT #	b231	b224	b223	b216	b215	b208	b207	b200	b199	b192	b191	b184	b183	b176
	PM7 VR [3:0] | PM7 VC [11:8]		PM7 VC [7:0]		PM6 I [11:4]		PM6 I [3:0] | PM6 VR [11:8]		PM6 VR [7:0]		PM6 VC [11:4]		PM6 VC [3:0] | PM5 I [11:8]	
BYTE #	B21		B20		B19		B18		B17		B16		B15	
BIT #	b175	b168	b167	b160	b159	b152	b151	b144	b143	b136	b135	b128	b127	b120
	PM5 I [7:0]		PM5 VR [11:4]		PM5 VR [3:0] | PM5 VC [11:8]		PM5 VC [7:0]		PM4 VI [11:4]		PM4 VI [3:0] | PM4 VR [11:8]		PM4 VR [7:0]	
BYTE #	B14		B13		B12		B11		B10		B9		B8	
BIT #	b119	b112	b111	b104	b103	b96	b95	b88	b87	b80	b79	b72	b71	b64
	PM4 VC [11:4]		PM4 VC [3:0] | PM3 I [11:8]		PM3 I [7:0]		PM3 VR [11:4]		PM3 VR [3:0] | PM3 VC [11:8]		PM3 VC [7:0]		PM2 I [11:4]	
BYTE #	B7		B6		B5		B4		B3		B2		B1	
BIT #	b63	b56	b55	b48	b47	b40	b39	b32	b31	b24	b23	b16	b15	b8
	PM2 I [3:0] | PM2 VR [11:8]		PM2 VR [7:0]		PM2 VC [11:4]		PM2 VC [3:0] | PM1 VI [11:8]		PM1 I [7:0]		PM1 VR [11:4]		PM1 VR [3:0] | PM1 VC [11:8]	
BYTE #	B0													
BIT #	b7	b0												
	PM1 VC [7:0]													

DESCRIPTION OF THE 78 BYTES OF DATA BEING SENT:

PM*X* VC **(12bits) :** Capacitor bank voltage for the specified X-th power cell in the EDC converter.
PM*X* VR **(12bits) :** Distributed resistor voltage for the specified X-th power cell in the EDC converter.
PM*X* I **(12bits) :** Cell current for the specified X-th power cell in the EDC converter.
VDC **(16bits) :** Conversion result for the voltage across the DC bus.
IDC **(16bits) :** Conversion result for the current measurement through the EDC converter.

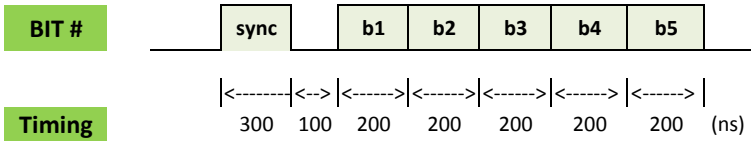
SM & FLT **(16bits) :** Internal state machine state and fault signals. The word description is:

BIT #	b15	b14	b11	b10	b8	b7	b4	b3	b0
	FLT FLAG	EMPTY		FLT CODE		EMPTY		SM STATE	

FLT CODE description

b10: EDC detected over-current
b9: EDC detected DC over-voltage
b8: Fault detecetd in one or several power cells

DATA PACKET: EDC CONTROLLER → POWER CELL (FIBRE OPTICS)



DESCRIPTION OF THE 6 BITS OF DATA BEING SENT:

sync	**:**	Synchronizing sequence to indicate start of new data packet. It has to parts, pulse and zero. Pulse duration is 300ns and zero duration 100ns.
bit1	**:**	T1 gate pulse.
bit2	**:**	T2 gate pulse.
bit3	**:**	T3 gate pulse.
bit 4	**:**	T4 gate pulse.
bit 5	**:**	T5 gate pulse.

The total duration of the data packet is 1.4 micro-seconds and a new packet is received from the EDC control board every 5 micro-seconds (200kHz).

DATA PACKET: POWER CELL → EDC CONTROLLER (FIBRE OPTICS)

BIT #	b38	b37 b26	b25	b24 b13	b12	b11 b0
	flt#1	VC [11:0]	flt#2	VR [11:0]	flt#3	I [11:0]

DESCRIPTION OF THE 39 BITS OF DATA BEING SENT:

flt#1	**(1bit):**	This is a fault flag generated inside the power module which combines the timeout flag from the VC ADC plus the local fault flag (which monitor capacitor overvoltage or module overcurrent).
VC	**(12 bits):**	Capacitor voltage ADC conversion result (unisgned).
flt#2	**(1bit):**	This is a fault flag generated inside the power module containing the timeout flag from the VR ADC.
VR	**(12 bits):**	Distributed resistor voltage ADC conversion result (unisgned).
flt#3	**(1bit):**	This is a fault flag generated inside the power module containing the timeout flag from the I ADC.
I	**(12 bits):**	Module current ADC conversion result (unisgned).

Appendix D

Simulation models

The Matlab/Simulink simulation block diagrams and the controller gains used for the simulations studies in Chapter 4 and Chapter 7 are presented here.

D.1 DBS circuit simulations from Chapter 4

In this section the block diagrams of the HVDC link plus each of the four different DBS circuits is presented. The values of PI gains in the VSC station controllers are detailed in Table D.1, while the gains for the different DBS controllers are detailed in Table D.2.

D.1.1 General HVDC interconnector

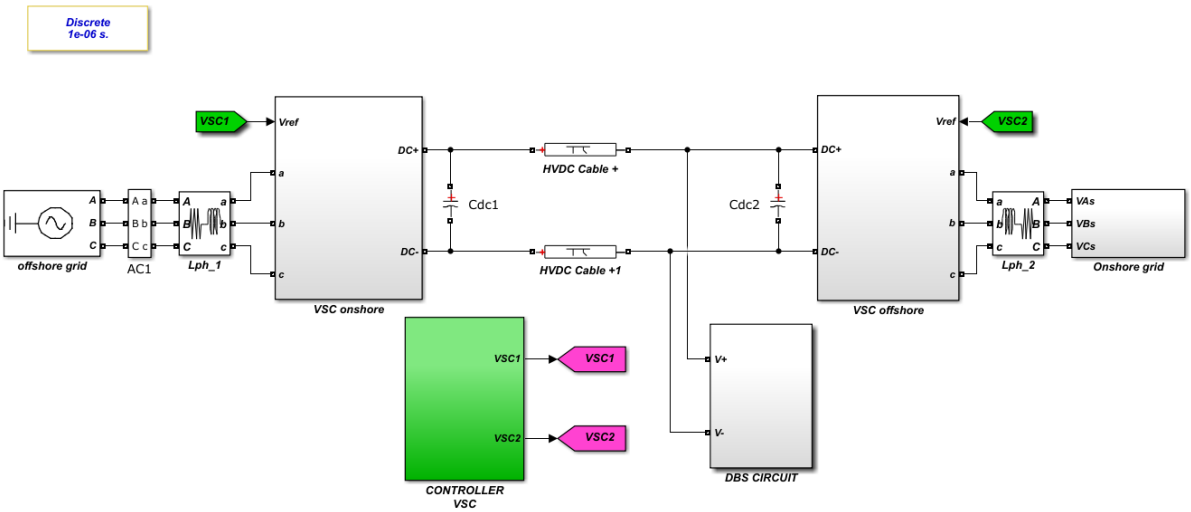


Fig. D.1 Global simulation block diagram.

Table D.1 PI controller gains for VSC stations.

VSC controller gains			
DC link voltage PI		AC current PI	
k_p	0.132	k_p	226
k_i	41.452	k_i	415.4

Table D.2 P and PI controller gains for DBS converters.

DBS converter controller gains				
	DBS#1	DBS#2	DBS#3	DBS#4
V_{DC} open loop controller gain				
k_p	20	320	20	20
Valve energy controller gains				
k_p	-	-	1e-6	3e-6
k_i	-	-	5e-7	12e-7

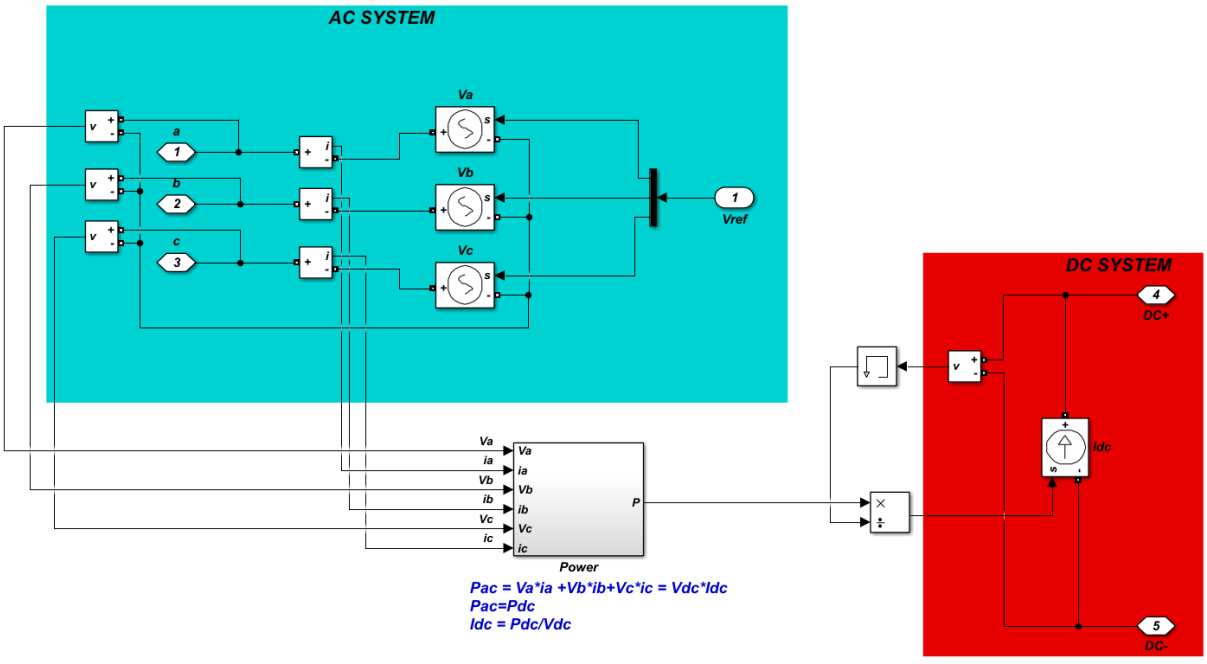


Fig. D.2 Average model of VSC stations.

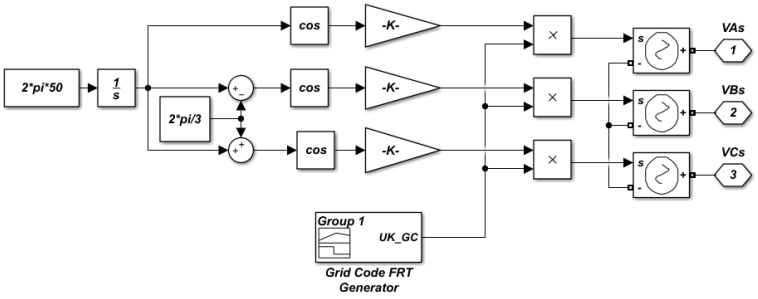


Fig. D.3 Onshore AC grid equivalent model with FRT characteristic.

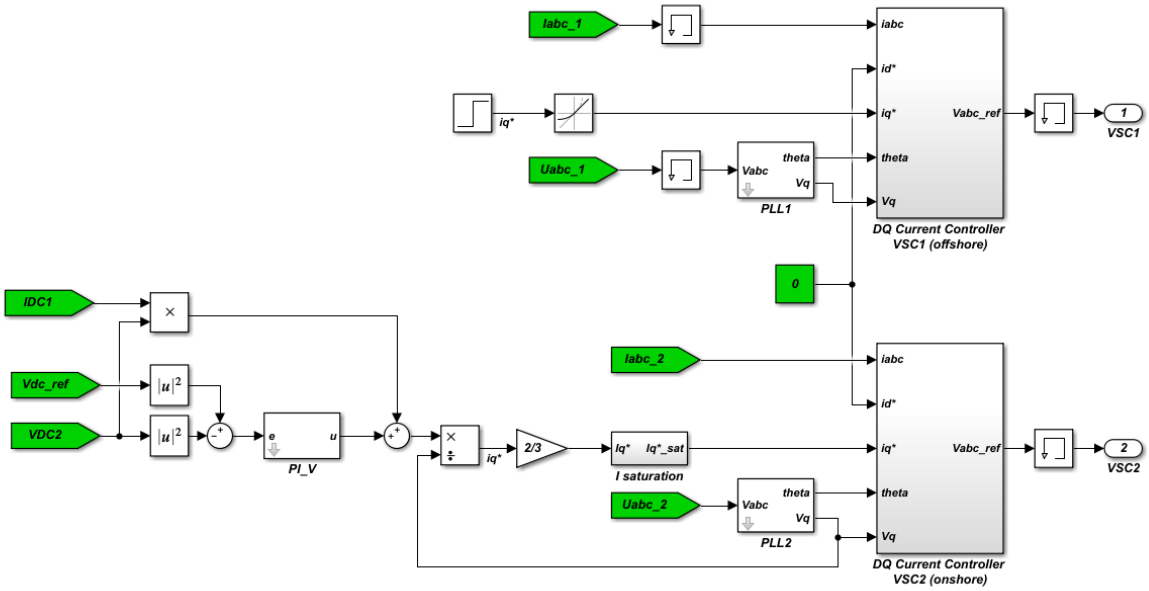


Fig. D.4 VSC station controller.

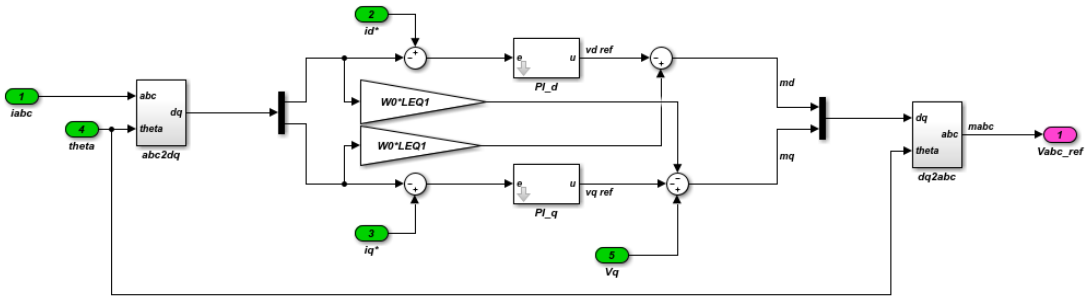


Fig. D.5 Detail of the inner current control loop.

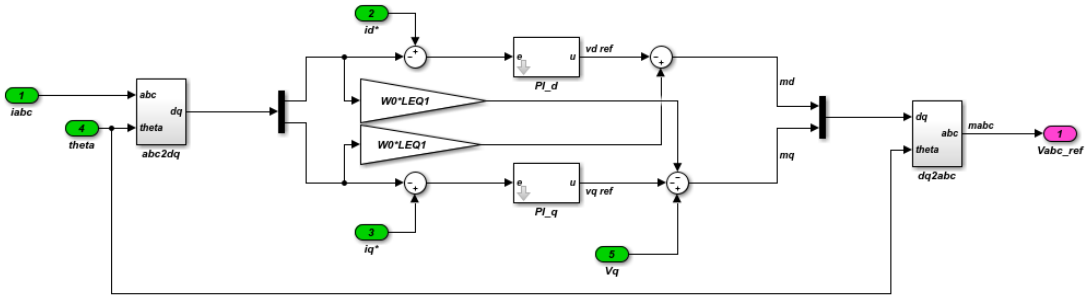


Fig. D.6 Detail of the inner current control loop.

D.1.2 HVDC chopper DBS circuit (DBS#1)

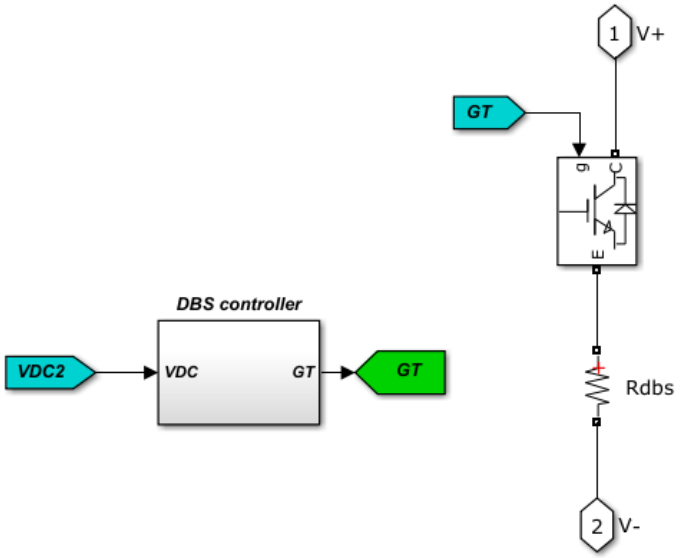


Fig. D.7 Global diagram of the HVDC chopper DBS.

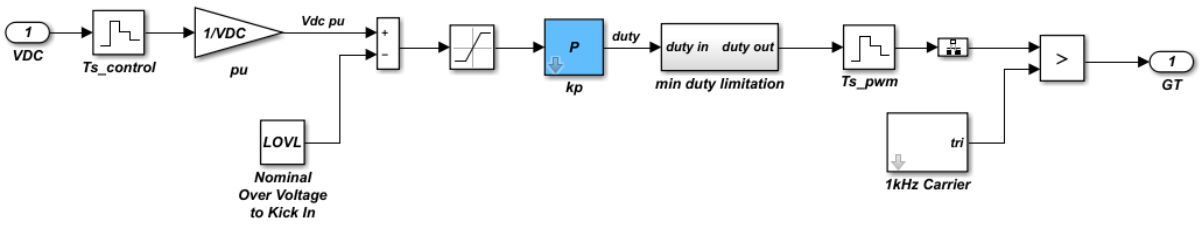


Fig. D.8 Controller detail for the HVDC chopper DBS.

D.1.3 Multilevel chopper DBS circuit (DBS#2)

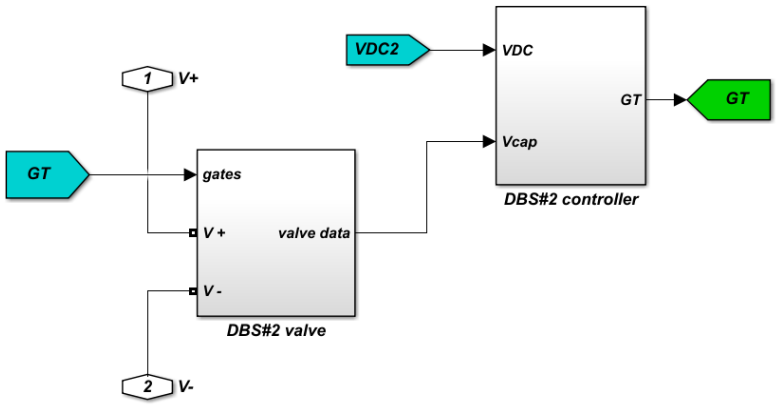


Fig. D.9 Global diagram of the multilevel chopper DBS.

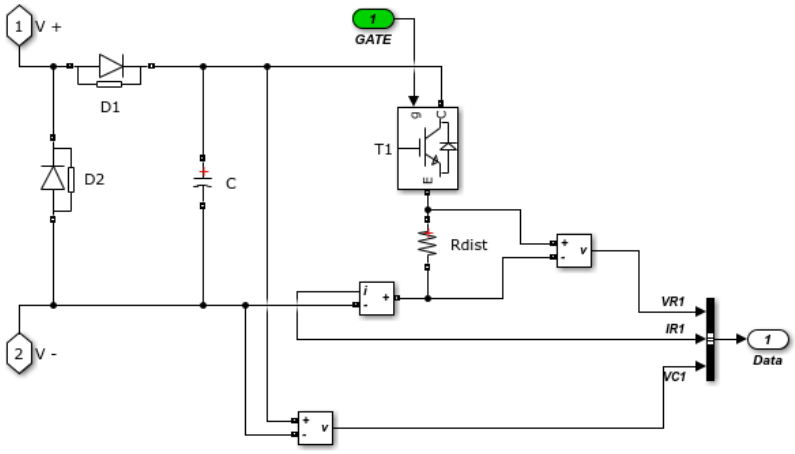


Fig. D.10 Cell detail for the multilevel chopper DBS.

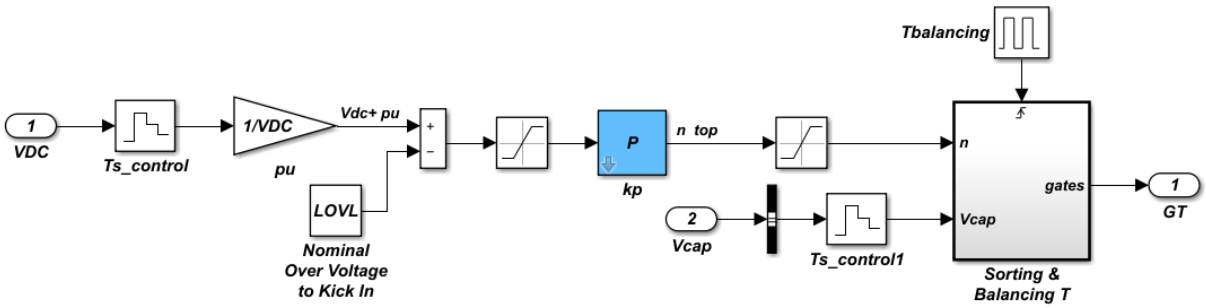


Fig. D.11 Controller detail for the multilevel chopper DBS.

D.1.4 Half-bridge multilevel DBS circuit (DBS#3)

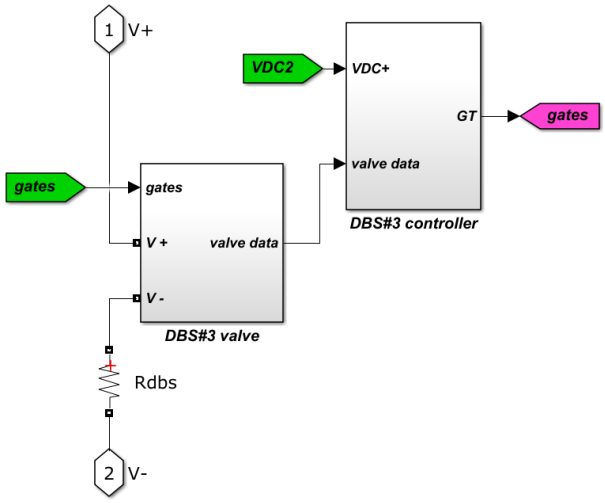


Fig. D.12 Global diagram of the half-bridge multilevel DBS.

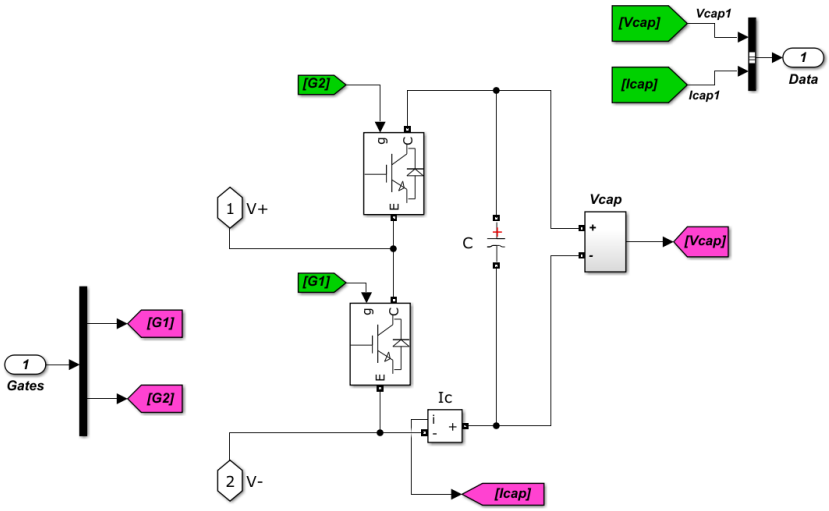


Fig. D.13 Cell detail for the half-bridge multilevel DBS.

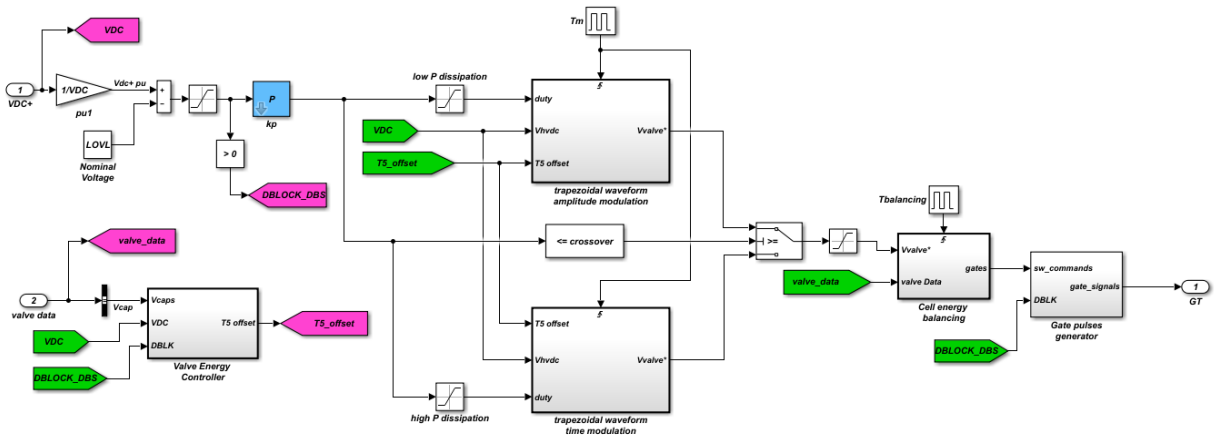


Fig. D.14 Controller detail for the half-bridge multilevel DBS.

D.1.5 Full-bridge multilevel DBS circuit (DBS#4)

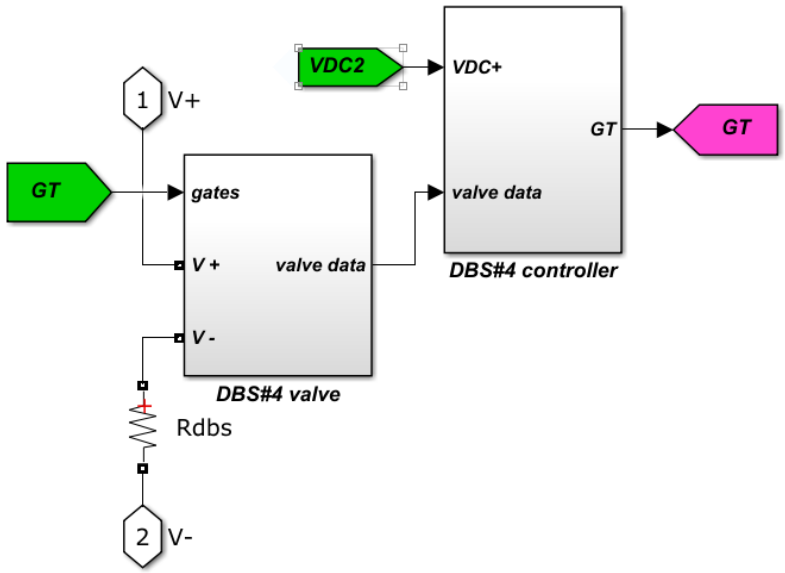


Fig. D.15 Global diagram of the full-bridge multilevel DBS.

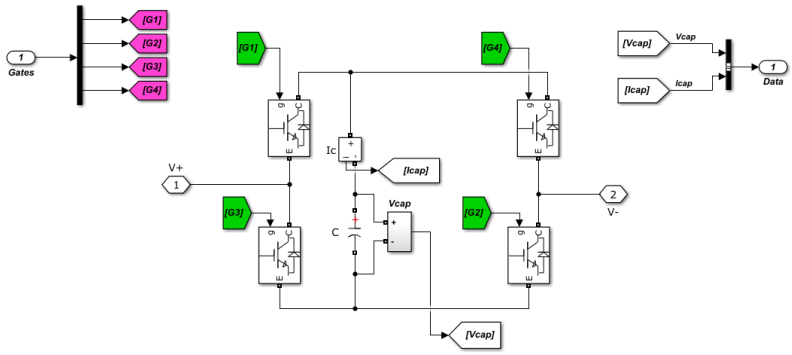


Fig. D.16 Cell detail for the full-bridge multilevel DBS.

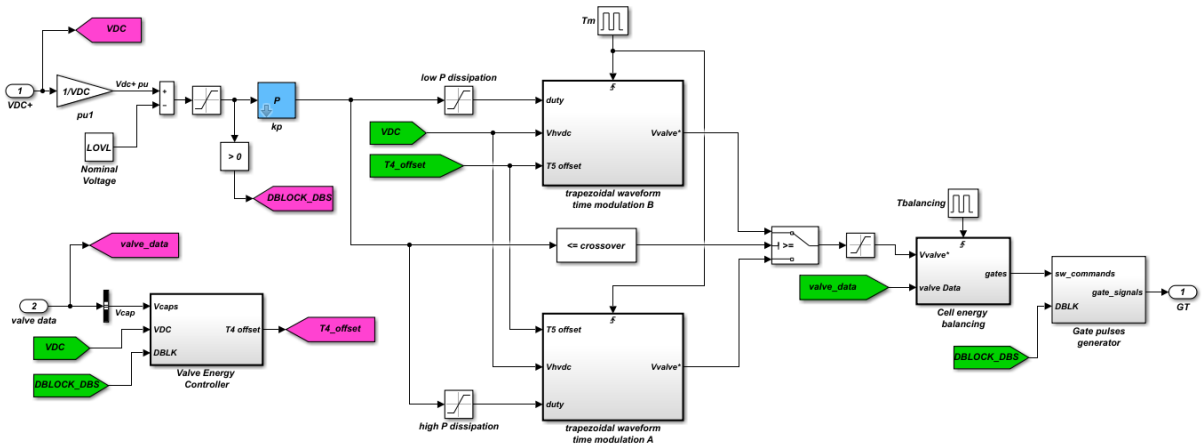


Fig. D.17 Controller detail for the full-bridge multilevel DBS.

D.2 HVDC tap circuit simulations from Chapter 7

In this section the block diagrams of the DC-DC converter for the implementation of the HVDC tap as well as the modified version that combines both the tap and DBS functionality are presented.

D.2.1 HVDC tap simulation model

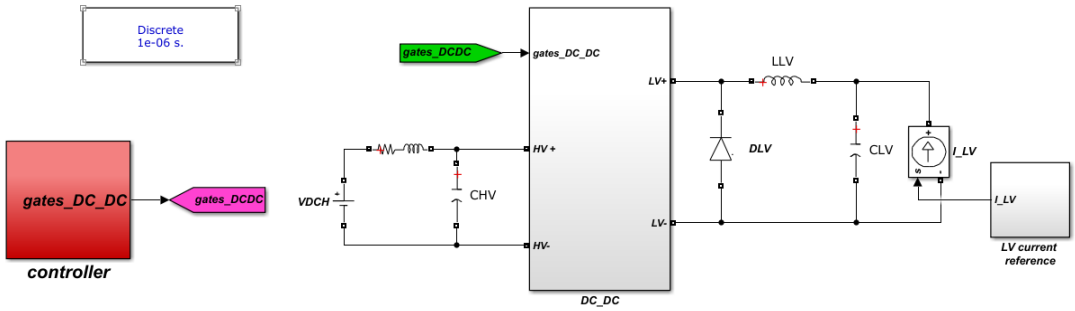


Fig. D.18 Global diagram of the HVDC tap simulation.

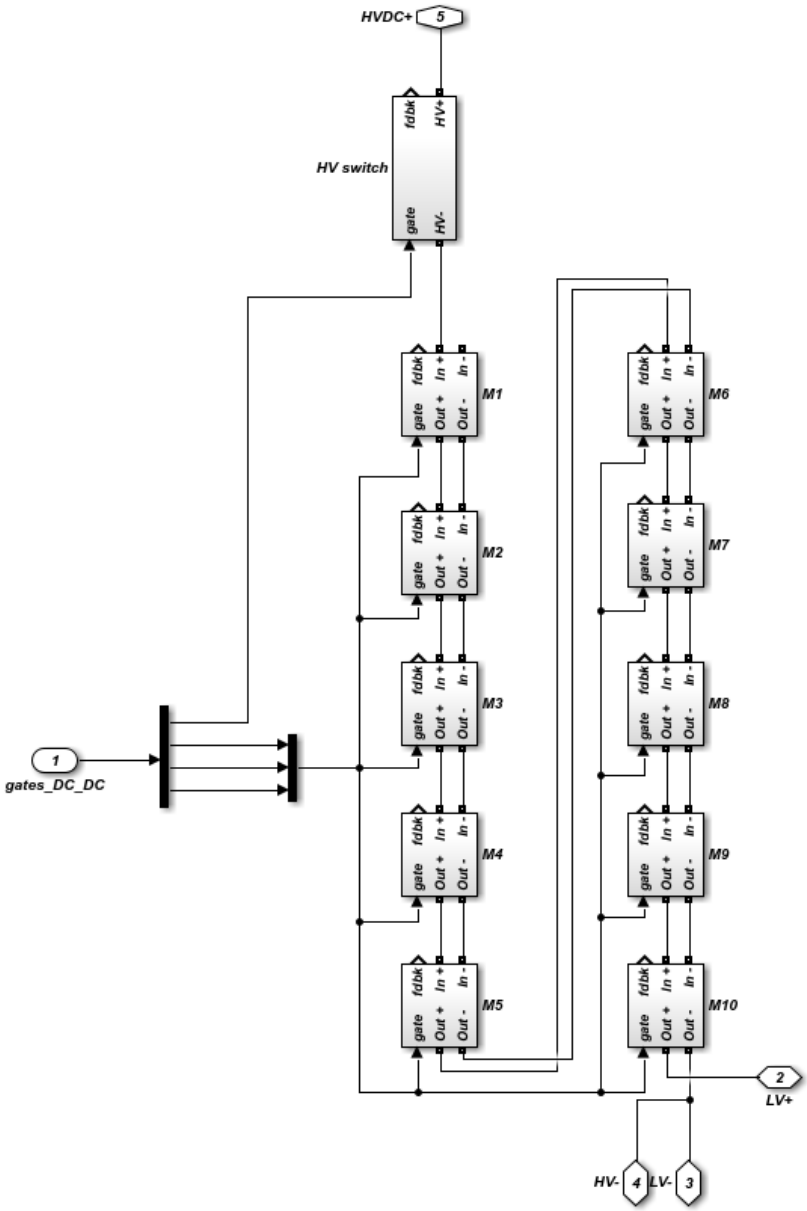


Fig. D.19 Detail of the DC-DC converter internal diagram.

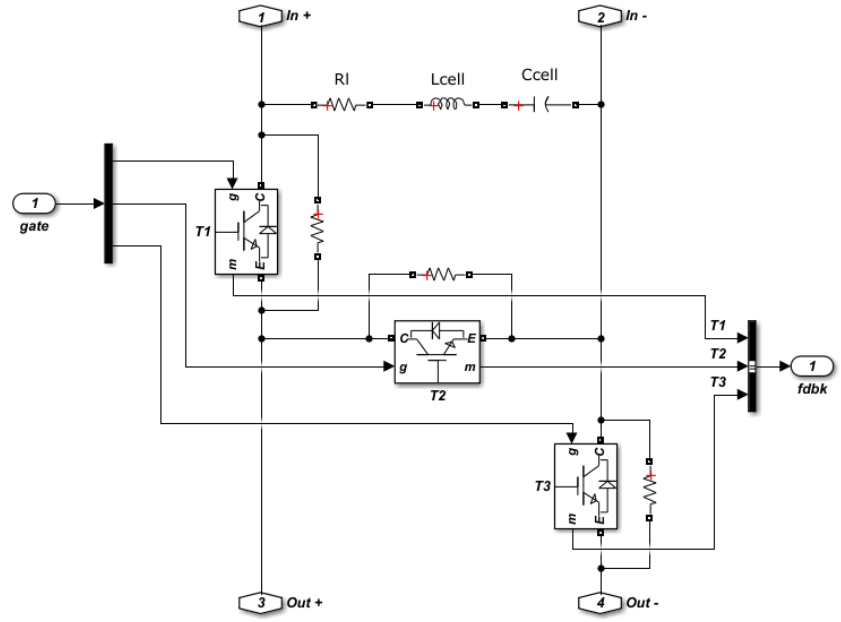


Fig. D.20 Detail of the DC-DC converter cell.

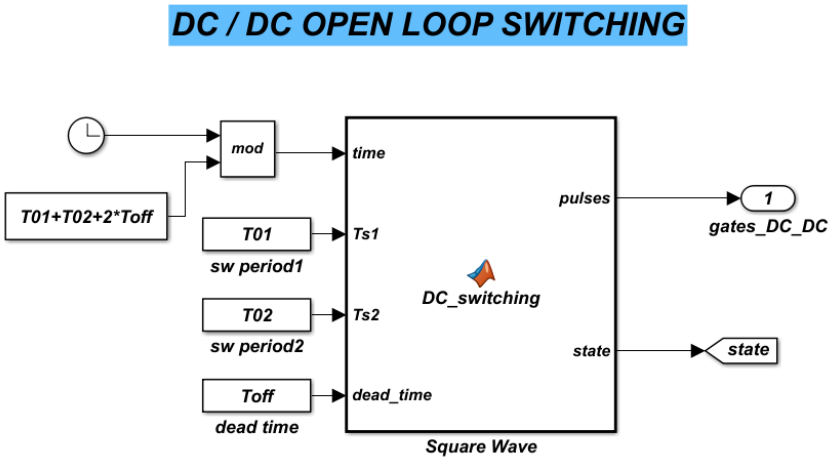


Fig. D.21 Controller detail for the DC-DC converter.

D.2.2 HVDC tap integrating DBS functionality simulation from Chapter 7

The simulation model is identical to the one presented in section D.2.1 with a few variations which are presented here. The proportional gain for the open loop voltage controller when operating in DBS mode is the same one specified in Table D.2 for the multilevel chopper (DBS#2).

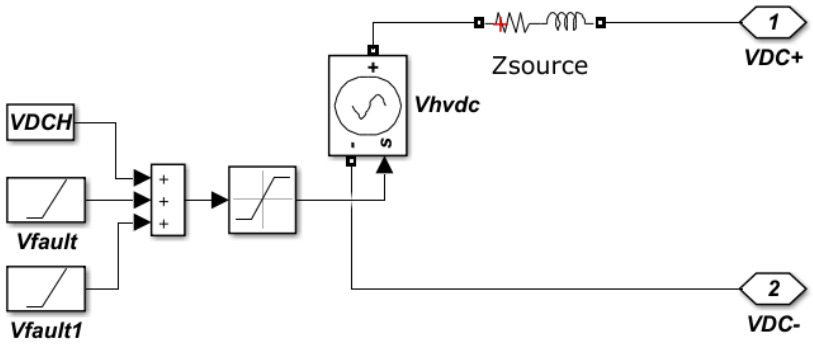


Fig. D.22 Detail of the high-voltage DC link for the HVDC tap integrating DBS simulations.

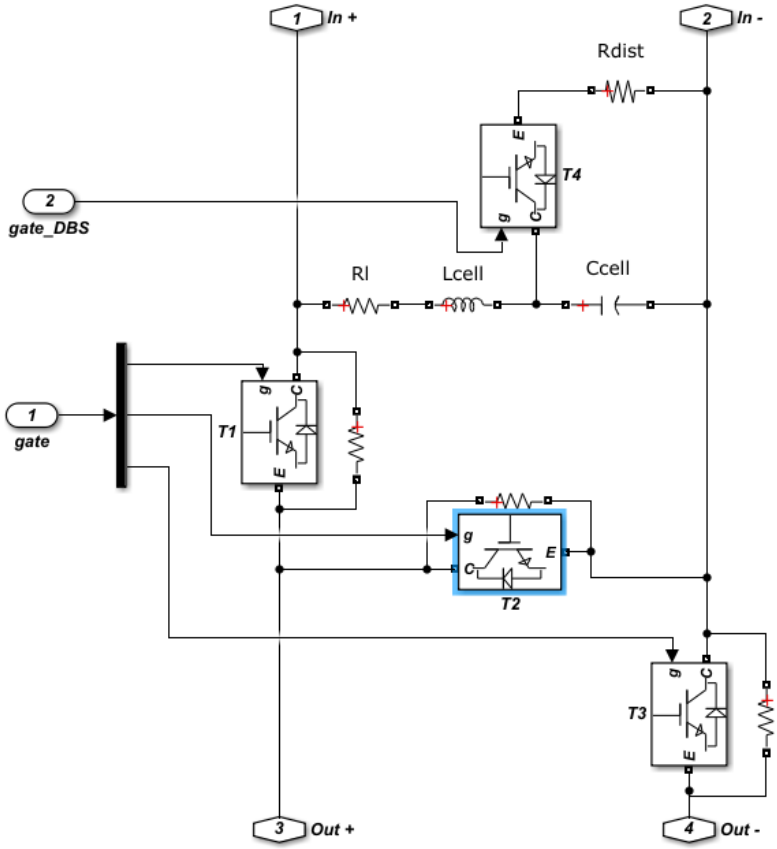


Fig. D.23 Modified cell including the distributed chopper circuit.

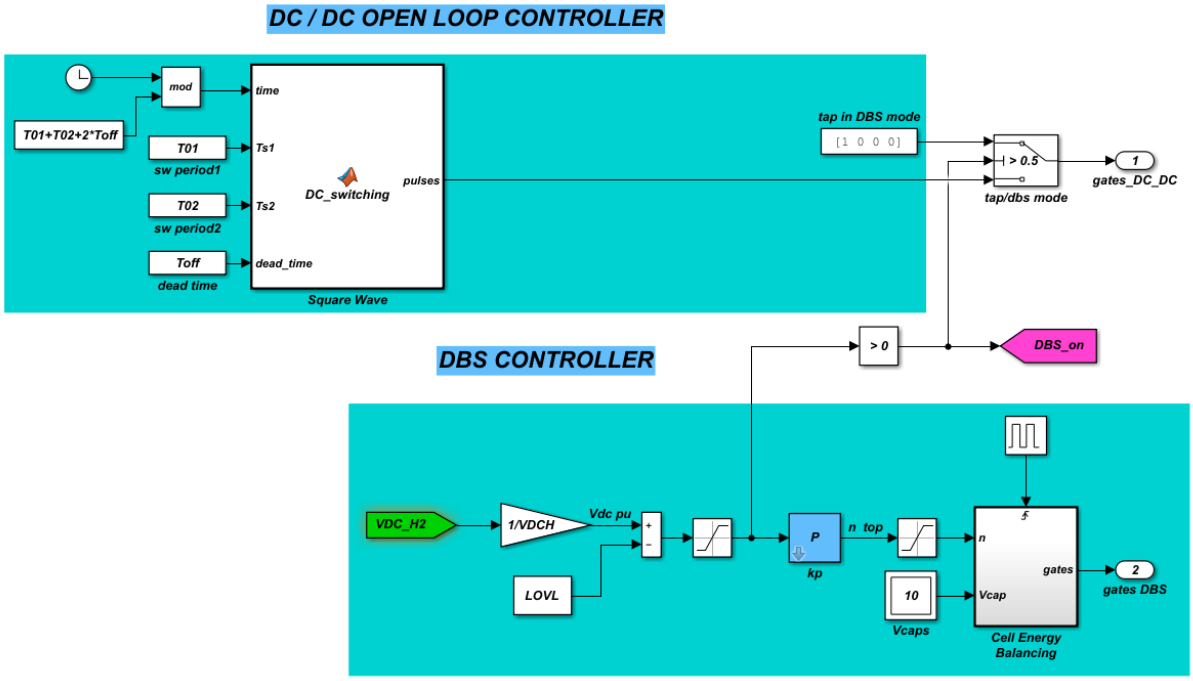


Fig. D.24 Controller detail for the DC-DC converter integrating DBS functionality.